STORAGE CAPACITANCE MINIMIZATION IN LED DRIVERS BASED ON PHOTOMETRICAL CONSTRAINTS AND CONVERTER INTEGRATION

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***Abstract* – This work proposes a novel combined approach for reducing the storage capacitances in off-line high power factor LED drivers. The proposal is to combine converter integration (power factor correction plus power control stages sharing a common switch) with photometrical constraints on the maximum allowable LED current ripple. An experimental setup was used to assess the upper limit for current ripple on the LEDs based on luminous flux drop, efficacy drop and chromaticity coordinate change. By combining the ripple design constraint obtained from photometrical measurements with the design methodology of an integrated converter, the largest storage capacitances (bus and output capacitors) were greatly reduced, allowing the use of small film capacitors of long lifespan, rather than relying on large short-lived electrolytic capacitors. As a design example, an integration between a SEPIC power factor preregulator and a buck-boost power control stage was chosen and a prototype was built, fed from 220 V / 60 Hz mains voltage and feeding 56 series-associated LEDs (ca. 70 W). The driver imposed a 50% current ripple on the LEDs, value for which it was found to yield only 0.2% decrement in luminous flux, while preserving color stability.**

***Keywords* - Converter Integration, Electrolytic Capacitor Avoidance, LED Current Ripple, LED Off-line Drivers, Photometrical Constraint on LED Ripple.**

I. INTRODUCTION

Light-emitting diodes (LEDs) are increasingly becoming a reality for lighting applications. Recent developments allowed high-power white LEDs to achieve luminous efficacies as high as 150 lm/W, already surpassing high-pressure sodium (HPS) lamps [1]. Road lighting is thus an application for which LEDs promise energy consumption reduction, mostly due to increased luminaire efficiency (that in the case of discharge lamp-based luminaires stands at ca. 75%, while for LED-based luminaires can be as high as 90%) [2] and also due to the spectrum of LED light. LEDs have far more of its spectral power on short wavelengths than HPS and thus yield increased effective illuminance at low-mesopic illumination levels [2], [3]. Medical treatments [4] and integration with photovoltaic systems [5] are also topics being currently investigated for LED application.

However, LED fixtures are still costly, and the driving of LEDs has several peculiarities. Devices must be driven by current sources, i.e., there must be a control scheme to limit current, and heat dissipation must be provided to maintain color stability of the LEDs and prevent early aging. InGaN-based high-power white LEDs are expected to have a lifetime of 100,000 hours or more [6], but this can only be attained when LEDs are properly heatsinked and junction temperature stays within safe margins. Plus, heatsinking plays an important role on the luminous flux output of the devices [7].

In theory, the long lifespan of the LEDs alone could counter the high initial cost of an LED luminaire, since expenditures with system maintenance and lamp replacement would be severely reduced. But since the weakest point in a properly designed LED luminaire is the electronic driver, increasing the reliability of these power converters becomes an important topic of research. Therefore, many recent works have been focused in reducing the number of active switches [8]-[15] as well as eliminating the need for electrolytic capacitors [9]-[17], components which are known to have an expected lifespan much shorter than the lifetime of the LEDs.

Using two conversion stages has been one of the most popular ways to reduce storage capacitance in high power factor (HPF) LED drivers [9]-[12]. In some of these cases, a two-stage driver comprising two separate individual converters in cascade connection (converter 1: power factor correction (PFC) stage; converter 2: power control (PC) stage) has both of them integrated to share a common power switch. This yields a single-stage integrated power converter (SSIPC) with all the characteristics of the cascade connection, and with a common bus voltage node, where a bus capacitor sits. This bus capacitor is usually the bulkiest within the circuit. The reprocessing of energy by both stages allows for a bus capacitance reduction proportional to the bus voltage and inversely proportional to output power [12]. A conceptual schematic of a SSIPC is given in Figure 1.

In this paper, a HPF off-line integrated LED driver is proposed, following an experimental approach to constraint the maximum allowable current ripple on the LEDs stemming from photometrical measurements. The combination of converter integration and photometrical constraints allows for additional reduction on the bus

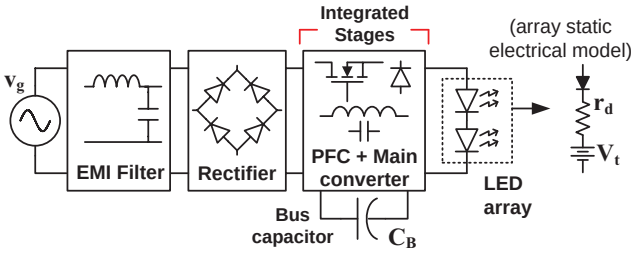

Fig. 1. Single-stage integrated power converter for LED driving.

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capacitance, while still ensuring that little impairment results to the LED photometrical performance (i.e., luminous flux, efficacy and color are well conserved). Experimental results with a prototype show the feasibility of the combined approach, which yielded capacitances smaller than those usually found in LED drivers designed with an integration-only or single converter approaches. This reduces overall cost and volume of the LED driver, while also increasing efficiency, given that less AC current will circulate through the energy storage elements (thus reducing losses in the equivalent series resistance (ESR) of capacitors).

II. RIPPLE PROPAGATION AND FILTERING REQUIREMENTS IN OFF-LINE HPF LED DRIVERS

In HPF LED drivers, similarly to other off-line applications, the pulsating (single-phase) power on the input produces a low-frequency voltage ripple on its output. These instantaneous power fluctuations are usually filtered out by a large bus capacitor, sized for twice the line frequency, which is the frequency of the voltage ripple that appears on the bus. This voltage ripple is propagated all the way through the converter and reaches the load, producing a current ripple which is inversely proportional to the dynamic resistance (r_d) of the LED array. This principle is shown in Figure 2, for an LED driver composed of two stages/converters: PFC and PC. The same principle applies for any SSIPC, since both converters (PFC and PC) are still present, only integrated into a single-stage/switch solution.

Since LED arrays usually have low values of dynamic resistance, even small voltage ripples on the output can produce large current ripples on the LEDs. A single converter operating as a PFC and driving an LED array would require fairly large capacitances to yield a low enough ripple on the load, such as in [18]-[21]. Two cascaded converters, on the other hand, can reduce the amount of filtering needed, because power is reprocessed and an extra degree of freedom is added to the design – the bus voltage.

In case filtering requirements demand high capacitances, such as in some single-converter approaches [18]-[21], electrolytic capacitors might be needed. These components are known to fail much earlier than the LEDs own estimated useful life [8]-[11], [16], [17], making the lifespan of the driver much smaller than the lifespan of the devices being driven. One current approach to increase driver reliability is to reduce capacitances as much as possible, so as to fall within the smaller capacitance range of film capacitors, which may have lifespans in excess of 100,000 hours [22], thus compatible with the lifetime of LEDs.

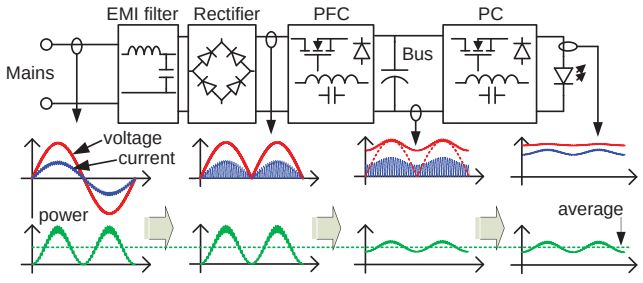

Fig. 2. Typical voltage, current and instantaneous power waveforms for a two-stage LED driver.

Reducing the size of the capacitors in LED drivers is therefore an important research topic, but this reduction might increase the LED current ripple. As much as the use of two cascaded converters and converter integration allows for capacitance reduction, the amount of ripple on the LEDs must be sized accordingly. Therefore, photometrical restrictions on current ripple are proposed in the next section, based on measurements with LEDs.

III. PHOTOMETRICAL CONSTRAINTS ON LED CURRENT RIPPLE

Some recent works address how the photometrical performance of LEDs is affected by the current waveform and by varying the amplitude of current ripple [23], [24]. It has been shown that the higher the amplitude of current ripple imposed to an LED array, the more luminous efficacy and luminous flux drop occurs due to the excursion of the current to very high peaks, where LEDs have lower efficacy. This leads to the fact that capacitances in LED drivers cannot be inadvertently reduced in an arbitrary manner, because this would increase the ripple to a point where the LEDs lose too much luminous flux and operate very inefficiently. Also, the larger the peak current for a given average value, the more chromaticity shift towards blue results [23], [24], therefore compromising the quality of the light emitted (correlated color temperature, color rendering index, chromaticity coordinates, etc.) Hence, it is of paramount importance to size the output current ripple adequately.

In this sense, a novel two-sided approach combining both integration and photometrical analysis seems quite adequate: the first implies in overall capacitance reduction, whereas the second limits the amount of ripple. Therefore a line must be drawn of how much low-frequency current ripple can be handled by the LEDs before sensible luminous flux decrease and color shifts result. For this purpose, an experimental set was assembled (Figure 3), in which the LED array intended to be driven, mounted on a heatsink, was subjected to various current ripples, ranging in peak-to-peak amplitude from 0% (stiff DC current, no ripple) to 200% (peak-to-peak value equals two times the average value), all with the same average current value of 350 mA (rated current of the LEDs).

The devices employed in this work are surface-mounted cool-white high-power white LEDs from Epileds, mounted on a well-sized aluminum heatsink. They were inserted inside an integrating sphere for flux and spectral measurements, with the LEDs fed by a DC current (350 mA) summed to an AC 120 Hz sinusoidal current, representing the current ripple in a similar manner to what is expected at the output of an off-line converter.

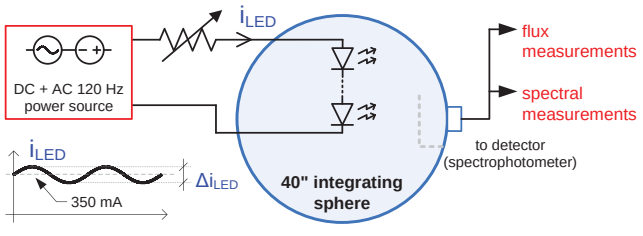

Fig. 3. Experimental setup for evaluating the impact of largely rippled currents on the LEDs photometrical performance.

Data gathered of luminous flux emitted and luminous efficacy of the LEDs at each tested ripple were all normalized to the DC value of flux and plotted against their respective percentage ripple with respect to the average value. The graphs obtained are shown in Figure 4.

Another relevant information assessed with the setup was how much color deviation resulted from the rippled currents. To take knowledge of this information, the chromaticity coordinates x and y were plotted against one another, for each one of the imposed ripple values, as shown in Figure 5. A trend line was drawn in the direction of increasing ripples.

In Figure 4, the data depicted falls within the small area marked by an arrow in the inset graph, close to the upper boundary of the 5000 K tolerance quadrangle defined by the ANSI C78.377 standard. Little drop on luminous flux and efficacy results from employing current ripples as high as 50% or 80% on the LED. In the case of a 50% current ripple, flux decrement was only 0.2%, whereas efficacy dropped by 1%. For 80% ripple, drops were 1% in flux and 2.7% in efficacy. Also, virtually no color shift is seen in Figure 5 for a 50% ripple, while only little chromaticity coordinate deviation is presented at 80% ripple, which is already fairly high (280 mA peak-to-peak, in this case). This means that ripples as high as 50-80% can be handled safely by the LEDs, without losing too much photometrical performance. This helps yielding an LED driver with smaller values of filtering capacitances if properly designed, to the point in which only long-lasting film capacitors could be employed.

It should also be noted that practically no difference in photometrical performance is perceived for the 5-30% ripple range when compared to the photometrical measurements

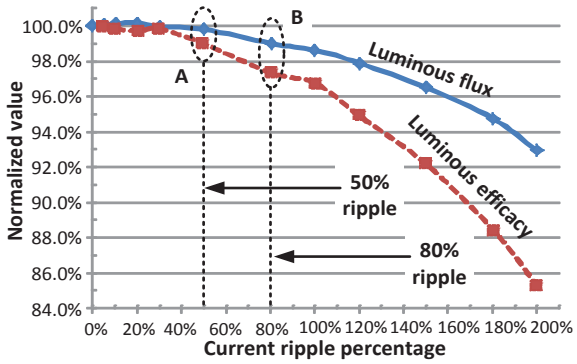

Fig. 4. Photometric measurements for the LED array when subjected to various current ripple amplitudes.

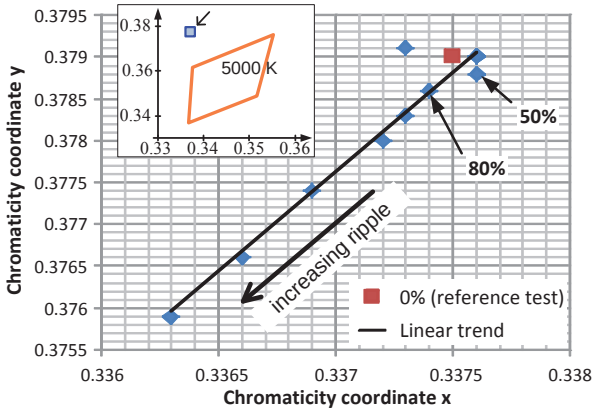

Fig. 5. Chromaticity coordinates for various tested ripples. The area analyzed by this graph is shown in the inset graph by an arrow.

obtained with a stiff DC current on the LEDs. Since current ripple is desired to be as high as possible – because it will lessen filtering requirements, the ripple constraint could be pushed farther from 30% in amplitude. From all the data gathered, it could be concluded that employing ca. 50% current ripple on the LEDs as a design constraint would suffice in terms of photometrical performance degradation (i.e., little degradation will result in this case): with 50% ripple, flux will drop minimally and efficacy will drop only by 1%, whereas chromaticity coordinates deviation will be $\Delta x = 0.0001$ (from 0.3375 at 0% to 0.3376 at 50%) and $\Delta y = -0.0002$ (from 0.3790 at 0% to 0.3788 at 50%). As such, color and luminous flux will be virtually unchanged, while luminous efficacy will lower almost unnoticeably. Also, 50% ripple marks the point on the curves from Figure 5 from which luminous efficacy will start to drop more steeply, making the 50% upper limit for current ripple a sensible choice for the design constraint.

IV. CONVERTER INTEGRATION AND MODES OF OPERATION

As already stated in this paper, using two cascaded converters to process the energy delivered to the LED load might help reducing the bus capacitance needed, mainly due to the extra degree of freedom introduced by this approach: one can choose a bus voltage such that the transmitted ripple from bus to the LED current will be minimum, or, at least, low enough. In general, the higher the bus voltage chosen, the smaller the capacitance needed for a given amount of ripple on the output [12], [14], making the adequate choice of bus voltage also of great design interest. In a single-converter approach, one cannot choose the bus voltage, since the LEDs will be connected directly to the bus capacitor, making the output voltage equals the bus voltage a design limitation. Furthermore, when using two cascaded converters, an integration between both of them can be proposed, in order to reduce the amount of controllable power switches, yielding fast dynamics and often simplifying the topology. The graft scheme integration technique developed in [25] is useful for such cases, and has been widely used for deriving new integrated topologies in which PFC and PC stages of power converters share a common power switch [8], [9], [11], [12], [14], [15], [25], [26], for various applications.

By applying the photometrical constraint for ripple drawn in the previous section plus the integration approach, the designer can achieve greater minimization in capacitance. This signals cost and volume reduction, since film capacitors are usually more expensive and more bulky than their electrolytic counterparts, for given capacitance.

Another important issue to be addressed regards the mode of operation of both converters of the SSIPC. Usually the first converter, the PFC stage, is operated in discontinuous conduction mode (DCM) to achieve power factor regulation without the need of current-mode control and two loops of compensation networks (one for bus voltage and one for input current). Because an integrated switching cell imposes that both conversion stages must now be operated at the same frequency and duty-cycle, one can greatly simplify and ease the converter design by only guaranteeing the PFC stage to

operate in DCM to achieve inherent power factor regulation (voltage follower method, [27] and [28]).

On the other hand, the second converter, the PC stage, could be operated either in DCM or continuous conduction mode (CCM). One of the advantages of operating the second converter also in DCM is that bus voltage in the SSIPC will be independent of duty-cycle, load and switching frequency [14], [26]. Being a previously defined and constant bus voltage of great design interest (since it directly relates to the ripple transmission to the output and size of the capacitor, as it will be shown), DCM-DCM operation might be preferable. Also, reference [10] reports significant reduction on the bus capacitance for the same SSIPC from [9] only by operating the PC stage also in DCM, for the same load – thus, in some cases, DCM-DCM might be more advantageous from the point of view of capacitance reduction and design freedom.

V. SEPIC BUCK-BOOST: A DESIGN EXAMPLE

So far, photometrical measurements were taken to size the amount of low-frequency ripple that the LEDs being driven by a certain converter could endure without losing their photometrical characteristics and performance. It was found that a 50% ripple would suffice as a design constraint. A discussion regarding the advantages in capacitance reduction arising from using two cascaded converters and integration was also done, concluding that SSIPCs are good choices for long-life LED drivers due to many of their peculiarities.

The design methodology based on the two-sided approach proposed – converter integration and photometrical constraining on current ripple – could be summarized by the following guidelines:

- Choosing an adequate PFC topology for the case (step up, step down or step up/down), given the desired power level and input/output characteristics: e.g., buck and boost converters as DCM PFCs present themselves with slightly distorted waveforms, depending on bus voltage [26]; others have it ideally sinusoidal, whereas some converters (buck-boost/Ćuk) lead to a negative bus voltage. DCM operation should be preferred due to ease in PFC realization (voltage follower PFC).
- Choosing a PC topology, also with the required characteristics, compatible with the power and voltage level of the load: e.g., a boost converter as a PC stage might not be desirable, since it would exceed the voltage level of the LED array if the bus voltage is chosen above LED array voltage.
- Choosing whether the PC stage will operate in DCM or not (assuming that PFC is in DCM). DCM could also be preferable, to achieve a bus voltage independent of load and duty-cycle. The designer can also compare the two modes of operation for the PC stage with respect to the ripple transmission to the LEDs, supposing the same bus capacitor for both possibilities; the one mode that transmits less ripple to the LEDs is the best choice.
- Choosing the bus voltage (assuming both PFC and PC in DCM) so as to minimize bus capacitance.
- Making sure that the 50% LED current ripple constraint is met for a given bus capacitor of the design, so as to conserve LED array photometrical performance.

Following the two-sided approach summarized, one design example is proposed. An integrated topology based on the SEPIC converter operating as PFC and the buck-boost converter operating as PC is chosen for this purpose. Such integrated SEPIC buck-boost (ISBB) converter is shown in Figure 6.

The SEPIC converter operating as a DCM PFC has several advantages: reducing or even removing the electromagnetic interference (EMI) filter commonly needed at the input (if $L_1 > L_2$), self PFC characteristics (voltage follower), active switch sharing same input and bus voltage reference, ideally sinusoidal current at input and the possibility to exchange the output inductor (L_2) for the magnetizing inductance of a transformer in an isolated application [26], [27]; the SEPIC converter alone has been employed in some single-converter off-line LED drivers, but with large and undesirable electrolytic capacitors [18]-[21].

The buck-boost operating as the PC stage was chosen so that bus voltage could be chosen above, equal or below the LED array voltage, giving the design more flexibility. The PC stage was also chosen to operate in DCM, given the aforementioned advantages; care will be taken to demonstrate that this mode of operation yields less ripple on the output given that the bus voltage is properly chosen.

The operating stages of the ISBB converter are given in Figure 7. The typical waveforms are given in Figure 8.

A simplified mathematical analysis for design purposes of the converter is given at following. A more complete analysis of this specific topology can be found in [24].

The input resistances emulated by each stage are given by (1) for the SEPIC and (2) for the buck-boost converters. The switching frequency is $f_s = 1/T_s$, L_e is an equivalent inductance for the SEPIC (L_1 parallel to L_2), L_{bb} is the buck-boost inductance, D is duty-cycle at operating point.

$$R_G = \frac{2L_e f_s}{D^2} \tag{1}$$

$$R_{bb} = \frac{2L_{bb} f_s}{D^2} \tag{2}$$

The load (LED array) can be represented by an equivalent resistance R_o and has an average voltage V_o at operating point, given by (3) and (4), respectively (I_o is the average output current).

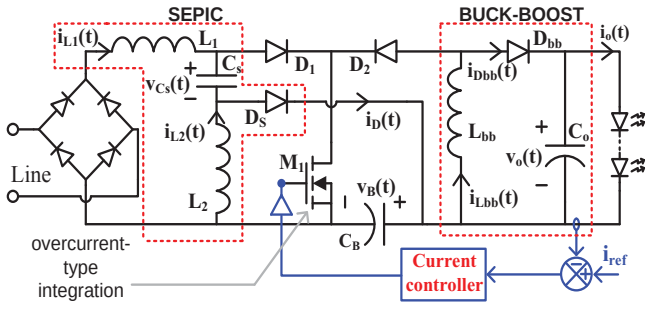

Fig. 6. The ISBB converter used as a design example for the two-sided approach to reduce storage capacitance.

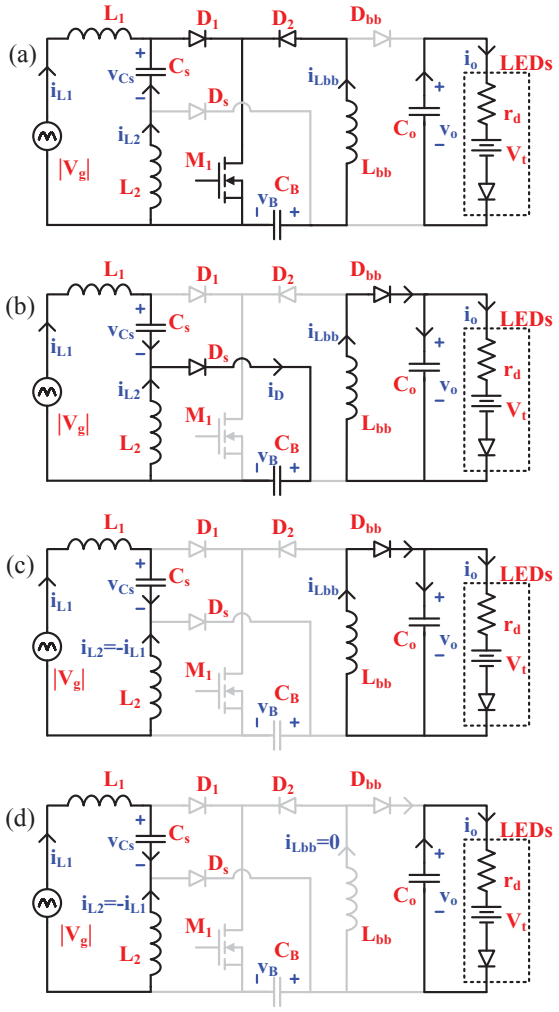

Fig. 7. Operating stages of the ISBB converter: (a) switch-on stage, (b) D_S conduction stage, (c) D_S turns off after i_D drops to zero (SEPIC DCM), (d) L_{bb} is discharged (buck-boost DCM).

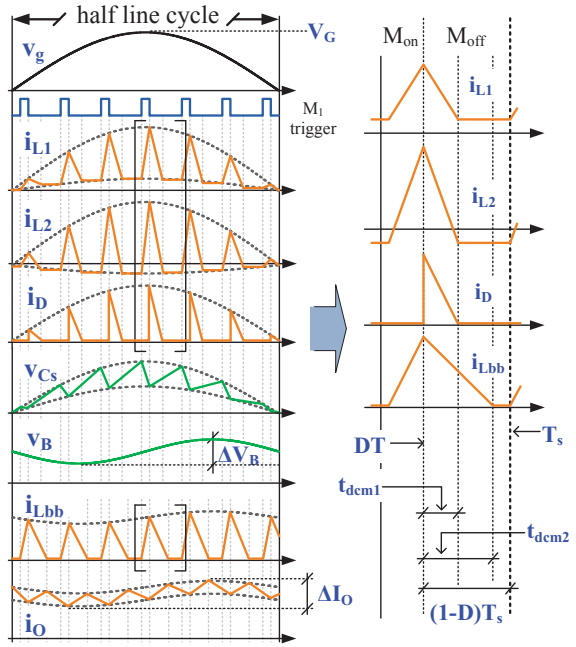

Fig. 8. Typical waveforms in the ISBB converter. Detail close to peak line voltage (V_G) is shown. All waveforms in time domain, t.

$$R_o = r_d + \frac{V_t}{I_o} \tag{3}$$

$$V_o = r_d I_o + V_t \tag{4}$$

Equaling input and output powers at the SEPIC stage only (neglecting voltage ripples) yields the relationship (5), which in turn establishes the ratio (6).

$$\frac{V_G^{\,2} D^2}{4 L_e f_s} = \frac{V_B^{\,2} D^2}{2 L_{bb} f_s} \tag{5}$$

$$\frac{V_G}{V_B} = \sqrt{\frac{2L_e}{L_{bb}}} \tag{6}$$

Equation (6) shows that the bus voltage V_B is indeed independent of load, only depending on peak line voltage V_G.

The current on the output of the first stage can be found averaging the diode D_S current from its waveform, for one switching cycle, which will yield a DC component (I_D) and an AC component ($\tilde{i}_D$), with twice line frequency. These are:

$$I_D = \frac{V_G^{\,2} D^2}{4 V_B L_e f_s} \tag{7}$$

$$\tilde{i}_D(t) = -\frac{V_G^{\,2} D^2}{4 V_B L_e f_s}\left[\cos(4\pi f_L t)\right] \tag{8}$$

Assuming that all the current flowing through bus capacitor C_B is $\tilde{i}_D$, the bus voltage ripple can be found by (9), where X_{CB} is the capacitor reactance and f_L is line frequency (60 Hz in this case).

$$\Delta V_B = 2\,|\tilde{i}_D|\,X_{CB} = \\ = \frac{V_G^{\,2}}{2\pi V_B f_L C_B} \times \frac{D^2}{4 L_e f_s} = \frac{V_o I_o}{2\pi V_B f_L C_B} \tag{9}$$

The RMS value of bus voltage will then be given by (10).

$$V_{B\_rms} = \sqrt{V_B^{\,2} + \frac{\Delta V_B^{\,2}}{8}} \tag{10}$$

Using (10) and (2) to find the power at the input of the buck-boost stage and equate it to the load power, the RMS value of output current (I_{o_rms}) can be found as in (11). In this equation, the RMS output current is defined similarly to (10) as a function of the output average current (I_o) and low-frequency current ripple (ΔI_{o_LF}), which appears due to transmission of the voltage ripple in the bus to the output, also with twice line frequency (as shown in Figures 2 and 8).

$$I_{o\_rms}{}^2 R_o = \frac{V_{B\_rms}{}^2}{R_{bb}}$$

$$\therefore I_{o\_rms} = \frac{D}{4}\sqrt{\frac{8V_B{}^2 + \Delta V_B{}^2}{L_{bb} f_s R_o}} = \sqrt{I_o{}^2 + \frac{\Delta I_{o\_LF}{}^2}{8}} \quad (11)$$

If current ripple at the output is neglected for one moment, the average output voltage V_o can be found solving second-order polynomial (12) and applying (4), which yields (13).

$$I_o V_t + r_d I_o{}^2 = \frac{V_{B\_rms}{}^2}{R_{bb}} \quad (12)$$

$$V_o = \frac{V_t}{2} + \sqrt{\frac{V_t^2}{4} + \frac{r_d}{R_{bb}} V_{B\_rms}{}^2} \quad (13)$$

Substituting (10) in (13) then taking its derivative with respect to V_B yields (14), which can be used as an approximation of the ratio bus voltage ripple to output ripple.

$$\frac{dV_o}{dV_B} = \frac{2V_B r_d}{R_{bb}\sqrt{V_t^2 + 4\frac{r_d}{R_{bb}} V_{B\_rms}{}^2}} \approx \frac{\Delta V_o}{\Delta V_B} \quad (14)$$

The output current ripple (low-frequency) will then be found by multiplying the ratio by ΔV_B and then dividing it by the dynamic resistance of the LED string ($r_d = \Delta V_o/\Delta I_o$), thus:

$$\Delta I_{o\_LF} = \frac{2V_B}{R_{bb}\sqrt{V_t^2 + 4\frac{r_d}{R_{bb}} V_{B\_rms}{}^2}} \times \Delta V_B \quad (15)$$

To find the total ripple on the output, the high-frequency current ripple must be considered. It is found by (16).

$$\Delta I_{o\_HF} = \frac{1}{f_s C_o r_d}\left(I_o + \frac{\Delta I_{o\_LF}}{2}\right)\left(1 - D\frac{V_B}{V_o}\right) \quad (16)$$

The total ripple on the output is the sum of both low and high-frequency components. This total ripple must meet the requirements derived from the photometrical analysis.

In order to operate in DCM, duty-cycle D must be below both of the critical duty-cycles (17) and (18), as in [28]:

$$D_{crit\_SEPIC} = \frac{V_B}{V_B + V_G} \quad (17)$$

$$D_{crit\_buck-boost} = \frac{V_o}{V_o + V_B} \quad (18)$$

The SEPIC capacitor C_S must also obey the constraint given in (19), as demonstrated in [27] to be necessary for low input current distortion for the SEPIC operating as a voltage-follower PFC.

$$f_L \ll \frac{1}{2\pi\sqrt{(L_1 + L_2)C_S}} \ll f_s \quad (19)$$

For this prototype, an LED array comprising 56 LEDs was used – these are the same LEDs used in the photometrical assessment from Section III. The equivalent electrical model has r_d = 98.4 Ω and V_t = 145 V, with a nominal current of I_o = 350 mA (V_o = 179.4 V). The LED driver is to be fed by 220 V / 60 Hz mains. The bus voltage was chosen V_B = 250 V, which showed good reduction in ripple transmission. Some other design parameters are summarized in Table I.

TABLE I
Input Parameters for the Prototype

Symbol	Description	Value
V_G	Input peak line voltage	311 V
V_B	Bus voltage (at V_G)	250 V
f_s	Switching frequency	50 kHz
f_L	Line frequency	60 Hz
I_o	Output current	350 mA
V_t	LED string threshold voltage	145 V
r_d	LED string dynamic resistance	98.4 Ω

The values of critical duty-cycle for each of the two stages of the converter are D_{crit_SEPIC} = 0.446 and $D_{crit\_buck\text{-}boost}$ = 0.418. Thus, D is chosen below these two: D = 0.35 (nominal). The ISBB converter design following the mathematical analysis returned the values from Table II.

TABLE II
ISBB Converter Prototype Components

Symbol	Description	Value
L_1	SEPIC input inductor	6.6 mH / E30 core
L_2	SEPIC output inductor	1.09 mH / E30 core
C_s	SEPIC main capacitor	33 nF / 630 V – polyester
C_B	Bus capacitor	10 µF / 350 V – polypropylene
L_{bb}	Buck-boost inductor	1.15 mH / E30 core
C_o	Output capacitor	3.3 µF / 250 V – polyester
M_1	Power MOSFET	SPP08N80C3
D_n	Power diodes	MUR460
L_f, C_f	Input EMI filter	2.2 mH / 220 nF

The bus capacitor C_B is a small 10 µF metallized polypropylene film capacitor of high reliability and rated life. These types of capacitors can have useful lives spanning up to 300,000 hours [22], outlasting even the LEDs. From (9), bus voltage ripple is calculated ΔV_B = 67.2 V (26.9%).

The theoretical output current ripples (low and high-frequency) are calculated from (15) and (16). Low-frequency ripple transmitted to output current is calculated ΔI_{o_LF} = 163 mA (46.5%) and with the output capacitor C_o = 3.3 µF (a long-life polyester film type), high-frequency ripple is ΔI_{o_HF} = 14 mA (3.9%). Thus, total ripple is summed up as being ΔI_o = 176 mA (50.4%), meeting the photometrical constraint

defined previously in this paper. It is possible to state that the small 10 µF polypropylene capacitor for C_B and the small 3.3 µF polyester capacitor for C_o suffice to respect photometric constraints on current ripple imposed by the design approach.

One could now compare both modes of operation of the PC stage (DCM and CCM) regarding ripple transmission to the LED load, for the same C_B = 10 µF. For such, the low-frequency output current ripple for the CCM case must be found. Were this converter operated with the PC stage in CCM, the output current ripple would be given by the buck-boost gain times the bus voltage ripple divided by r_d:

$$\Delta I_{o\_LF\_CCM} = \frac{I_o}{2\pi C_B f_L} \frac{D^2}{(1-D)^2} \frac{1}{r_d} \qquad (20)$$

It is possible to see that, different from the DCM case, the ripple in CCM does not depend on V_B, but depends on D. The opposite is true for the DCM case: it only depends on V_B and other converter parameters, but not on D. This is where the correct choice of V_B comes in handy: for some V_B, the ripple transmitted to the output by the PC conversion stage will be smaller in DCM, for a given operating point D. This result is more easily seen graphically: plotting (20) and (15) together as functions of D and having V_B as a parameter, both divided by I_o (normalized), returns the curves from Figure 9. This graph shows a hatched region for which the DCM operation will be more advantageous, because less low-frequency current ripple will result from the transmission of bus voltage ripple to the output. Given that the operating point of the ISBB converter design falls within the hatched region, DCM operation is indeed the best option in this case.

A prototype of the ISBB converter was built to validate the design methodology and the integration plus photometrical constraint approach to reduce storage capacitance. The prototype is shown in Figure 10. A glass passivated single-phase bridge rectifier (GBU4J) was used on the input, diodes are all fast-recovery MUR460 and power switch is an SPP08N80C3 MOSFET. The main waveforms obtained with the prototype follow in Figures 11 to 14.

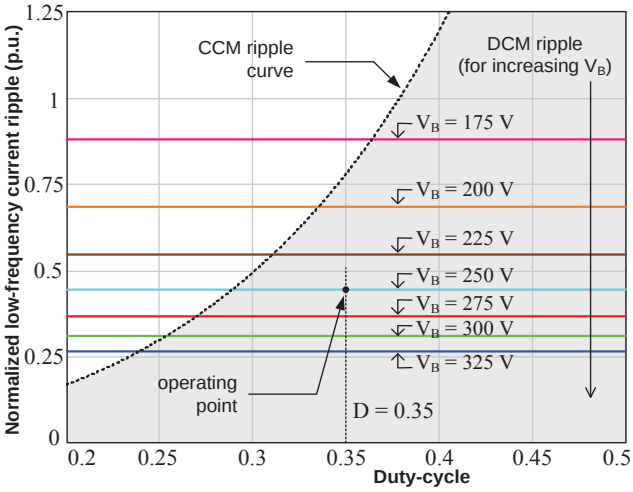

Fig. 9. Normalized current ripple at the output for the PC stage converter operated in DCM (solid lines, parameterized) compared to hypothetical CCM operation of the same stage (dotted line).

Fig. 10. Prototype of the ISBB LED driver. Polypropylene film bus capacitor is the cylindrical component in the middle of the picture.

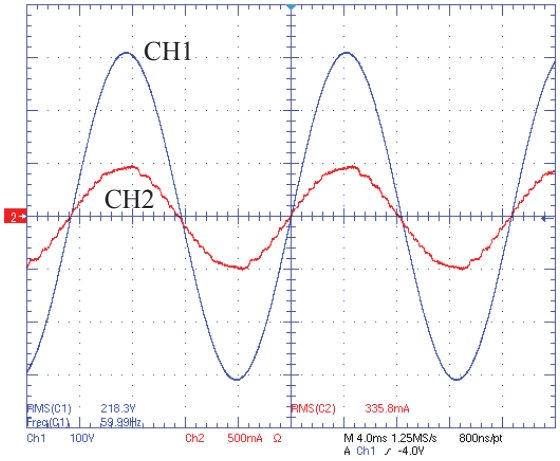

Fig. 11. Voltage (CH1 – 100 V/div) e current (CH2 – 500 mA/div) on the input of the converter. Time scale: 4 ms/div.

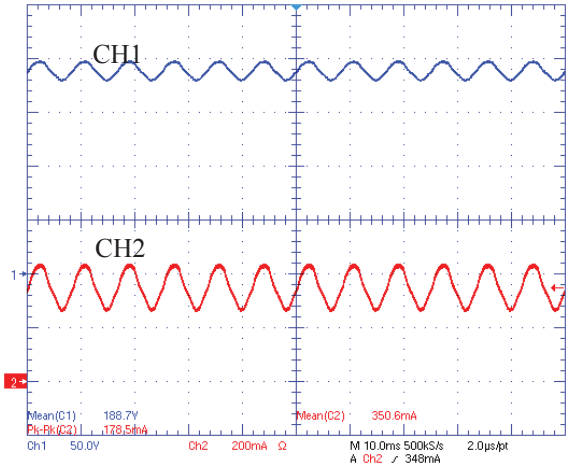

Fig. 12. Voltage (CH1 – 50 V/div) and current (CH2 – 200 mA/div) on the output of the converter. Time scale: 10 ms/div.

The experimental results are given in Table III, showing total output current ripple measured as 51%, meeting the photometrical requirement imposed by the methodology.

TABLE III
Experimental Results

Description	Value
Input power	70.4 W
Output power	63.5 W
Input power factor	0.998
Input current distortion (THD)	3.2%
Overall efficiency	90.2%
Total output current ripple	178 mA (51%)
DC bus voltage	255 V
DC bus voltage ripple	71.8 V (28%)

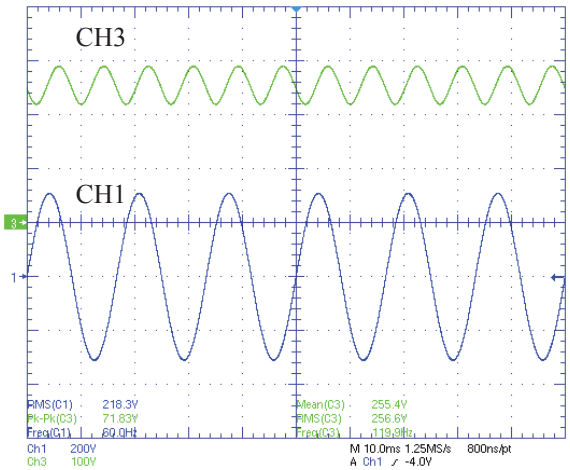

Fig. 13. Input voltage (CH1 – 200 V/div) and bus voltage (CH3 – 100 V/div). Time scale: 10 ms/div.

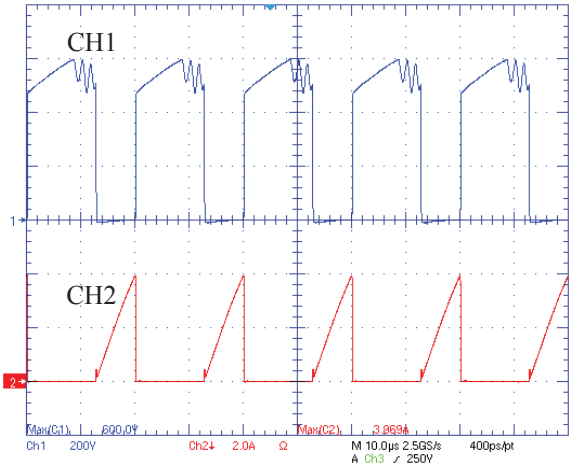

Fig. 14. Shared switch voltage (CH1 – 200V/div) and current (CH2 – 2A/div) at peak line voltage, showing DCM operation. Time scale: 10 µs/div.

Power factor was close to unitary, as expected for a SEPIC PFC. Total harmonic distortion (THD) of input current was very low and harmonic content of input current complies with the IEC 61000-3-2 class C restrictions.

The efficiency of the converter (90%) was fairly high for a SSIPC. Losses in the circuit were detected mainly in the magnetics (5%). Shared switch losses were 2 W (3%), mostly during turn-off, inherent to DCM operation (high peak current, zero current on turn-on).

VI. CONCLUSION

A two-sided approach for reducing storage capacitance for HPF off-line LED drivers was proposed, combining the already popular integration of converter stages of cascaded topologies with the novel proposal of a photometrical constraining on the maximum allowable current ripple on the LEDs. The combination of both techniques allowed for an extreme reduction in the capacitances needed for proper circuit operation, without degrading the photometrical performance of the LEDs being driven. This fact is supported by photometrical evidence of luminous efficacy, luminous flux and chromaticity coordinates, which were shown to decrease (or shift, in the case of the coordinates) negligibly when a current ripple as high as 50% was imposed on the LED array being driven.

Following the upper limit constrained by this methodology, design guidelines for integrated converters were derived, based on many of their inherent characteristics when driving LEDs and also based on the photometric data.

A design example employing a SEPIC PFC stage integrated in a buck-boost PC stage was then done. The main design equations were given, and it was demonstrated that, for this particular design, given that the bus voltage is properly selected (250 V, in this case), DCM-DCM operation yields less ripple on the output, comparatively; DCM-DCM also allows for V_B to be constant and an input design parameter, as desired. Therefore this mode of operation was chosen, because it allowed for a reduced bus capacitance (10 µF) and a large bus voltage ripple (around 28%) without surpassing the upper limit in the LED current ripple imposed by the photometrical constraint.

A prototype was built employing the design methodology outlined. Current ripple on the output was maintained within desired amplitude for the implemented prototype (51%), without the need to employ unreliable and short-lived electrolytic capacitors and also without the need for very high switching frequency (100 kHz and above), as in many works addressing capacitance reduction [15]-[17]. High power factor, high efficiency and low input current harmonic content were attained, along with the removal of electrolytic capacitors, which is expected to largely increase the life expectancy of the driver, to match that of the LEDs. Several advantages were explored in the ISBB design example: self-PFC characteristics, lower EMI filtering required compared to most DCM PFCs, grounded switch facilitating triggering and control. One disadvantage is the floating output, but current measurements can be made differentially without much difficulty, employing an operational amplifier.

Though this particular converter employs 4 capacitors and 4 inductors (including EMI filter), the prototype is not bulky, as seen in Figure 10, mainly due to the small values of capacitances needed. Furthermore, all 4 capacitors are long-life metalized film type, which unfortunately are inherently more expensive than electrolytic counterparts, however, since film capacitor cost and volume are usually proportional to capacitance and voltage rating, employing small capacitances such as the ones from this prototype also results in overall cost, volume and weight reduction of the LED driver. This is also one of the main achievements of the storage capacitance reduction approach proposed.

Cost and volume is estimated to be further reduced due to the presence of only one active power switch, as a result of integration, although efficiency may be penalized in these cases due to redundant power processing by both cascaded conversion stages (PFC and PC) and by the increase in current/voltage stresses on these components. Though efficiency might be an issue in integrated converters, the storage capacitance reduction methodology is also helpful in increasing efficiency, because film capacitors of very small capacitance will always have ESR much smaller than common electrolytics or even large-sized film capacitors.

In this paper, controller design was not addressed, as focus was on the novel approach for reducing storage capacitance.

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