ANALYSIS OF A SOFT-SINGLE-SWITCHED QUADRATIC BOOST CONVERTER

Lúcio R. Barbosa
Universidade Estadual de Londrina
Campus Universitário – Caixa Postal: 6001
Cep: 86051-990 – Londrina – PR – Brasil
lbarbosa@uel.br

Leandro S. Vilefort, Fábio V. Silva, Ernane A. Coelho, Luiz G. Freitas, Luiz C. Freitas and João B. Vieira Jr.
Universidade Federal de Uberlândia
Faculdade de Engenharia Elétrica
Cep: 38400-902 – Uberlândia – MG –Brasil
batista@ufu.br

***Abstract* – In recent years, the development of new technologies is requiring power supplies with wide dc conversion range. In this paper an alternative solution is presented, the properties of the new soft-single-switched (SSS) Boost converter with voltage ratio that are quadratically dependent on duty cycle are discussed. The converter is a zero-current-switching (ZCS) during the turn-on period and a zero-voltage-switching (ZVS) during the turn-off period. The operating principle of the proposed converter is explained; its operating modes along with key waveforms are shown. Moreover, a complete simulation and experimental results have verified the feasibility of its applications in renewable energy systems.**

***Keywords* – Quadratic Boost, Soft-Single-Switched.**

I. INTRODUCTION

The demand of efficient step-up dc-dc converters has been rising due to the increase of battery powered applications and low voltage storage elements. Typical applications are embedded systems, renewable energy systems, fuel cells, mobility applications and uninterrupted power supply (UPS) [1], [2] and [3]. These applications demand high step-up static gain, high efficiency and reduced weight, volume and cost.

There are six basic single-switch topologies that can be used in non-isolated, high-frequency, switch-mode converters: buck, boost, buck-boost, cuk, sepic, and zeta. They are used mainly in dc-dc converters [4], but sometimes in ac-dc converters, and are effective in converting the supplied input voltage to the required output voltage. There are, however, applications where none of the basic converter topologies are suitable and alternative topologies need to be considered.

New technological developments require for such alternative topologies systems, in which the converter output voltage to input voltage conversion ratio G(D) is a function of the converter duty cycle D. For most applications, one of the basic converter topologies can be used, but for other applications that require power supplies with significant step-up and/or step-down voltages, for example in portable applications and photovoltaic arrays [5], none of the basic converters has a suitable value of G(D).

Topologies with different values of G(D) can be produced if basic converters are cascaded with each other. It was shown in [6] that such cascaded converters can be implemented with only a single switch and thus single switch converters with non-standard conversion ratios can be synthesized. These converters are frequently referred to as quadratic converters as G(D) is related to the square of D. Additional quadratic boost converter topologies have been proposed in [7] and [8].

Quadratic converters can also be considered in fuel cell systems, where the range of the output voltage is between 24 V and 60 V. These values are low when compared to the voltage needed at the input of an inverter when dc-ac conversion is required. This results in the need of another conversion stage – a boost converter – between the fuel cell and the inverter to boost the fuel cell voltage considerably. A standard boost converter is inadequate for this task and a quadratic converter can be used to avoid the use of more sophisticated topologies with transformers.

Although a quadratic boost converter is a single switch non-isolated converter, it is essentially a two-stage converter as it is made up of two cascaded converters as shown in Figure 1. This means that power must be processed twice as opposed to being processed only once in a basic converter. Consequently, a quadratic converter can never be as efficient as one based on one of the basic topologies and thus should only be use in applications where standard basic converter is inadequate.

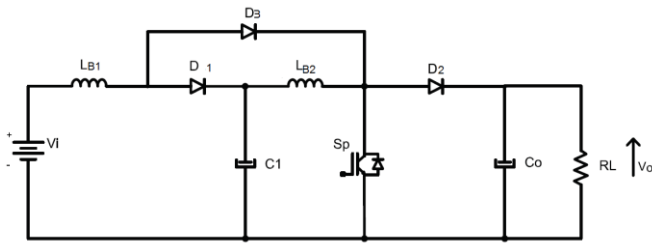


Fig. 1. Quadratic boost converter.

Manuscript received on 27/02/2013, revised 30/06/2013 and acceptance for publication issued on 04/08/2013, upon recommendation of Regular Section Editor Henrique A. C. Braga.

One type of application for which a quadratic converter is well-suited is for applications where low cost, low power is required. Power electronics researchers have therefore been motivated to develop simpler, less expensive such as single-switch converters for low power applications [9]. It was presented in [10] a quadratic converter used to drive a LED string for photodynamic therapy purpose. It can be used in hybrid electrical systems supplied by photovoltaic systems or 110/220 V_{AC} from the utility power grid [11].

In above mentioned converters, however, switching losses are still inevitable. A number of quadratic converters have been proposed in the power electronics literature [12-15]. In order to maintain high switching frequency operation while maximizing the converter efficiency, soft switching cells are introduced to the converters. Several kinds of soft switching converters, such as series and parallel resonant converters, quasi-resonant converters (QRCs), and multi-resonant converters (MRCs) [16], have been proposed to alleviate these problems.

One type of development in high frequency converter configuration is a hybrid of resonant soft switching and pulse-width-modulation (PWM) control. This group of converters is called soft switching PWM converters; an example of these converters is presented in [17]. In the soft switching PWM converters, the switches operate in resonant mode only during switching transitions and then, return to PWM operation for the rest of a switching period.

A comparison of soft switching methods for PWM converters had shown that passive method has better efficiency in the high power operation region, while active method outperforms the passive method in the low power regions [18]. However, this small improvement in efficiency is partially countered by higher gate drive losses, higher control complexity, and lower reliability compared to the passive method.

This paper provides an interesting Quadratic Boost topology based on the soft switching method presented in [19]. It has several advantages: (a) high efficiency in a large operation area, (b) reduction in the driver circuits and the main advantage, (c) less complex, which results from the use of only one single active switch, two diodes and three resonant components (two inductors and a capacitor) to achieve soft switching. The operation, key waveforms corresponding to each operating mode are shown, experimental and simulations results are presented.

II. PRINCIPLE OF THE PROPOSED CONVERTER

The power stage diagram of the proposed quadratic boost Soft-Single-Switched (SSS) PWM converter is shown in Figure 2. The circuit can be divided in two sections. The first is the pulse-width modulation continuous conduction mode (CCM) step-up converter, composed by L_{b1}, L_{b2}, S_1, D_1, D_2, D_3, C_1 and C_o. This section operates as two boost converters in cascade, each one being processed by the active switch. The second section is a SSS-PWM auxiliary circuit to provide soft-switching. It is composed by the auxiliary diodes D_4, D_5, the resonant inductors L_{r1}, L_{r2} and the resonant capacitor C_r.

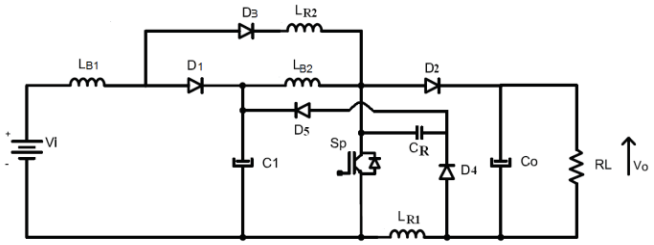


Fig. 2. SSS-PWM Quadratic boost converter.

A. Topological states and mathematical analysis

For convenience in analysis, it is assumed that the proposed quadratic boost SSS-PWM converter is operating in steady-state and the following assumptions are made during one switching cycle: all components and devices are ideal; the filter inductances L_{b1} and L_{b2} are large enough to assume that I_{Lb1} and I_{Lb2} currents are constant in one switching period and is much greater than resonant inductors L_{r1} and L_{r2} ; the filter capacitors C_1 and C_o are large enough to assume that V_{C1} and output voltage V_o is constant and ripple free.

Based on these assumptions, circuit operation in one switching cycle can be divided into ten stages. The topological stages of the new quadratic boost SSS PWM converter during one switching period is shown in Figure 3, where switch S_1 starts conducting at $t=t_0$ and turns off at $t=t_4$.

In this section, the analytical expressions describing the operation of the proposed converter are presented. The following definitions are assumed:

$$\omega_{01} = 1/\sqrt{C_r.L_{r1}} \quad (1)$$

$$\omega_{02} = 1/\sqrt{C_r.L_{r2}} \quad (2)$$

$$\alpha_1 = \frac{I_{Lb2}}{V_0}\sqrt{\frac{L_{r1}}{C_r}} \quad (3)$$

$$\alpha_2 = \frac{I_i}{V_{C1}}\sqrt{\frac{L_{r2}}{C_r}} \quad (4)$$

$$G_1 = V_o / V_{C1} \quad (4)$$

$$G_2 = V_{C1} / V_i \quad (6)$$

$$G = V_o / V_i \quad (7)$$

1) First Stage - [$t_0 t_1$], Figure 3(a) – Before $t=t_0$, the main switch S_1 maintains turn-off state, the current I_i flows through D_1 and I_{Lb2} through D_2. This stage begins when S_1 turns on with ZCS at $t=t_0$. The resonant inductor L_{r1} discharges linearly due to output voltage V_o from I_{Lb2} to zero. The stage ends when diode D_2 turns off at $t=t_1$. The current $i_{Lr2}(t)$ remains zero because the output voltage is greater than that of the capacitor C_1. The resonant $i_{Lr1}(t)$ and $v_{Cr}(t)$ can be respectively described as:

$$i_{Lr1}(t) = I_{Lb2} - (V_o / L_{r1})t \quad (8)$$

$$v_{Cr}(t) = V_o \quad (9)$$

$$\Delta t_1 = \alpha_1 / \omega_{o1} \quad (10)$$

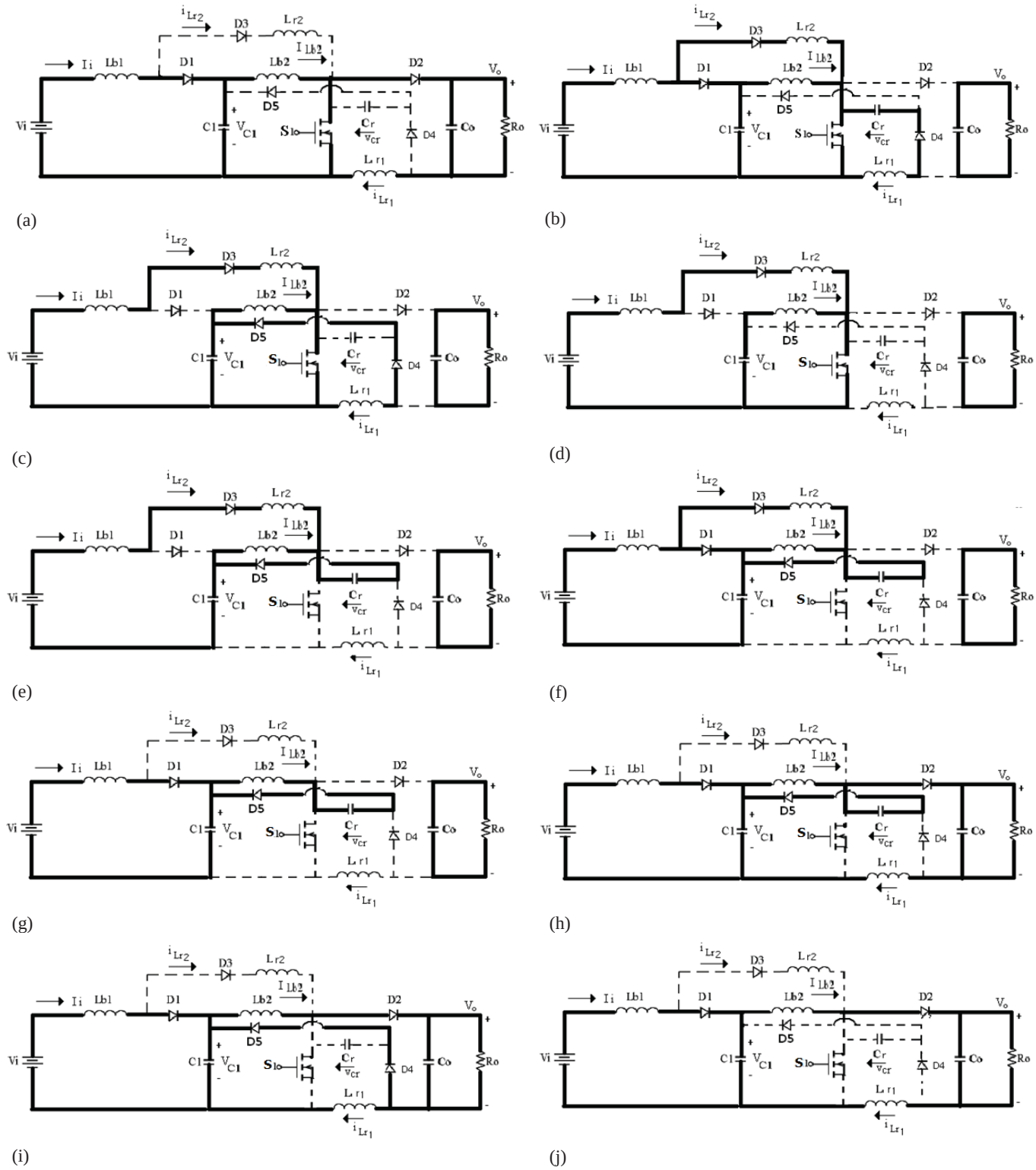


Fig. 3. Topology Modes

2) Second Stage - [t_1.t_2], Figure 3(b) – In this stage, the resonance begins when D_4 turns on at t=t_1'. The resonant loop proceeds by way of L_{r1}, C_r, S_1 and D_4. The resonant current $i_{Lr1}(t)$ decreases and the resonant voltage $v_{Cr}(t)$ also decreases via the resonance of L_{r1} and C_r. The resonant inductor L_{r2} charges linearly from zero to I_i. This state ends when the voltage $v_{Cr}(t)$ reaches capacitor C_1 voltage V_{C1} at t=t_2. The resonant behavior of $i_{Lr1}(t)$ and $v_{Cr}(t)$ can be respectively described as:

$$i_{Lr2}(t) = (V_{C1} / L_{r2})t \tag{11}$$

$$\Delta t_2^{'} = \alpha_2 / \omega_{o2} \tag{12}$$

$$i_{Lr1}(t) = -V_0 \sqrt{\frac{C_r}{L_{r1}}} \sin(\omega_{01} t) \tag{13}$$

$$v_{Cr}(t) = V_0 \cos(\omega_{01} t) \quad (14)$$

$$\Delta t_2 = \frac{\pi - \arccos\left(-\frac{V_{C1}}{V_0}\right)}{\omega_{01}} \quad (15)$$

At the end of this stage i_{Lr1} is equal to:

$$i_{Lr1}(t_2) = -\frac{I_{Lb2}}{\alpha_1}\sqrt{1-\frac{1}{G_1^2}} \quad (16)$$

3) Third Stage - [t_2, t_3], Figure 3(c) – The diode D_5 turning on clamps resonant capacitor voltage at $V_{C1.}$ In this mode $i_{Lr1}(t)$ decreases linearly until it reaches zero, delivering all its stored energy to the capacitor C_1. The expressions for $i_{Lr1}(t)$ and $v_{Cr}(t)$ are:

$$i_{Lr1}(t) = \frac{V_{C1}}{L_{r1}} t - \frac{I_{Lb2}}{\alpha_1}\sqrt{1-\frac{1}{G_1^2}} \quad (17)$$

$$v_{Cr}(t) = -V_{C1} \quad (18)$$

$$\Delta t_3 = \frac{\pi - \cos^{-1}\left(-\frac{V_{C1}}{V_0}\right)}{\omega_{01}} \quad (19)$$

4) Fourth Stage - [t_3, t_4], Figure 3(d) – The main switch is conducting and the input current I_i and I_{Lb2} flow through the power switch. All diodes are blocked, excepting diode D_3, and the input inductor stores energy. The equations that describe this mode are:

$$i_{Lr1}(t) = 0 \quad (20)$$

$$v_{Cr}(t) = V_{C1} \quad (21)$$

$$\Delta t_4 = t_5 - t_4 \quad (22)$$

5) Fifth Stage5- [t_4, t_5], Figure 3(e) – At the instant t_4, switch S_1 is turned-off in a ZVS way and the energy stored in the inductors L_{b1} and L_{b2} is transferred to the resonant capacitor C_r through the diode D_5. In this time interval, C_r linearly discharges to zero voltage. The resonant behavior of $i_{Lr1}(t)$, $i_{Lr2}(t)$ and $v_{Cr}(t)$ can be respectively described as:

$$i_{Lr1}(t) = 0 \quad (23)$$

$$i_{Lr2}(t) = I_i \quad (24)$$

$$v_{Cr}(t) = -V_{C1} + \frac{I_i + I_{Lb2}}{C_r} t \quad (25)$$

$$\Delta t_5 = \frac{1}{\alpha_2 \omega_{02} + \alpha_1 \omega_{01} G_1} \quad (26)$$

6) Sixth Stage - [t_5, t_6], Figure 3(f) – In this stage, the resonance begins when D_1 turns on at $t=t_5$. The resonant loop proceeds by way of L_{r2}, C_r, D_5, D_3 and D_1. The resonant current $i_{Lr2}(t)$ decreases and the resonant voltage $v_{Cr}(t)$ increases. This state ends when the current $i_{Lr2}(t)$ reaches zero at $t=t_6$.

$$i_{Lr2}(t) = I_i \cos(\omega_{02} t) \quad (27)$$

$$v_{Cr}(t) = I_i \sqrt{\frac{L_{r2}}{C_r}} \sin(\omega_{02} t) \quad (28)$$

$$\Delta t_6 = \frac{\pi}{2\omega_{02}} \quad (29)$$

7) Seventh Stage - [t_6, t_7], Figure 3(g) – At the instant t_7, switch D_3 is turned-off and the energy stored in the inductor L_{b2} is transferred to the resonant capacitor C_r through the diode D_5. In this time interval, C_r linearly charges to V_o-V_{C1}.

$$i_{Lr2}(t) = i_{Lr1} = 0 \quad (30)$$

$$v_{Cr}(t) = \alpha_2 V_{C1} + \frac{I_{Lb2}}{C_r} t \quad (31)$$

$$\Delta t_7 = \frac{G_1 - 1 - \alpha_2}{\alpha_1 \omega_{01} G_1} \quad (32)$$

8) Eight Stage - [t_7, t_8], Figure 3(h) – In this stage, the resonance begins when D_2 turns on at $t=t_7$. The resonant loop proceeds by way of L_{r1}, C_1, D_5, C_r, D_2 and C_o. The resonant current $i_{Lr1}(t)$ increases and the resonant voltage $v_{Cr}(t)$ also increases via the resonance of L_{r1} and C_r. This state ends when the voltage $v_{Cr}(t)$ reaches output voltage V_o at $t=t_8$. The resonant behavior of $i_{Lr1}(t)$ and $v_{Cr}(t)$ can be respectively described as

$$i_{Lr1}(t) = I_{Lb2}(1 - \cos(\omega_{01} t)) \quad (33)$$

$$v_{Cr}(t) = V_o - V_{C1} + I_{Lb2}\sqrt{\frac{L_{r1}}{C_r}} \sin(\omega_{01} t) \quad (34)$$

$$\Delta t_8 = \frac{1}{\omega_{01}} \arcsin\left(\frac{1}{\alpha_1 G_1}\right) \quad (35)$$

At the end of this stage i_{Lr1} is equal to

$$i_{Lr1}(t_8) = I_{Lb2}\left(1 - \sqrt{1 - \left(\frac{1}{\alpha_1 G_1}\right)^2}\right) \quad (36)$$

9) Ninth Stage - [t_8 t_9], Figure 3(i)- – When capacitor C_r voltage becomes V_o diode D_4 is turned on and L_{r1} current increases linearly. This stage finishes when the L_{r1} current becomes equal to inductor L_{b2} current.

$$i_{Lr1}(t) = i_{Lr1}(t_8) + \frac{V_{C1}}{L_{r1}} t \quad (37)$$

$$\Delta t_9 = \frac{1}{\omega_{01}}\sqrt{(\alpha_1 G_1)^2 - 1} \quad (38)$$

10) Tenth Stage - [t_9, t_0], Figure 3(j)- – During this stage transference of energy from source to load occurs through diode D_2, starting another switching cycle.

$$i_{Lr1}(t) = I_{Lb2} \quad (39)$$

$$\Delta t_9 = \frac{1}{\omega_{01}}\sqrt{(\alpha_1 G_1)^2 - 1} \quad (40)$$

B. Main waveforms and static gain

Figure 4 shows three different region of the plane (α_1xG_1). In the region 3, the converter operates with hard switching and in the other two regions it works with soft switching. In the regions 2 and 3 the L_{r1} current becomes equal to I_{Lb2} preventing v_{Cr} reaches V_o, as indicated at t_8 in Figure 5. Despite of this, the converter operates with soft switching in the region 2.

The ideal relevant waveforms are shown in Figure 5. It is only valid for $\alpha_1 > 1/G_1$ (region 1), physically, for low values of load current, the energy stored in resonant inductor would not be sufficient to charge resonant capacitor to capacitor C_1 voltage, which results in hard switching. Equation (36) define region 2 upper limit, it can be reached by $i_{Lr1}(t_8) \leq I_{Lb2}$. Equation (33) define region 3 upper limit, it can be accomplished by $i_{Lr1}(t_8) = I_{Lb2}$. The new Δt_8 prevents v_{Cr} to reach V_o.

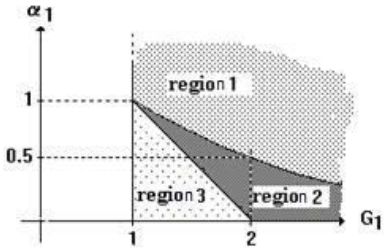


Fig. 4. Converter operating regions.

The static gain is a function of the duty cycle and normalized input current.

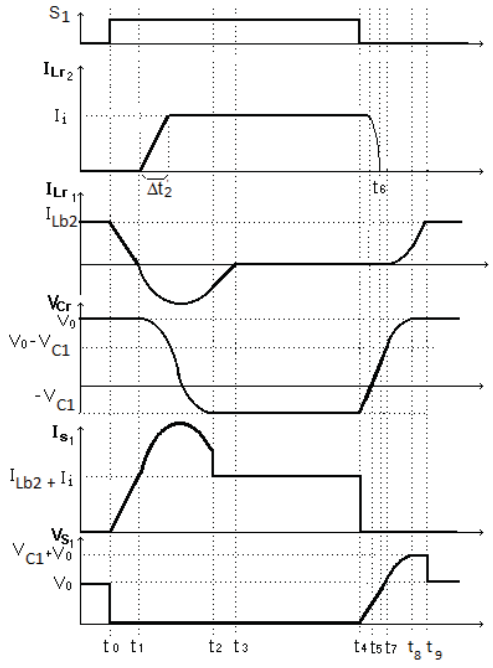


Fig. 5. Main theoretical waveforms.

After the mathematical analyses, the expression of the static gain can be obtained.

$$G_1 = \frac{V_0}{V_{C1}} = \frac{1}{1 - D - \frac{1}{T_s \omega_{01}}\left(-\alpha_1 + \frac{1}{2\alpha_1}\right)} \quad (41)$$

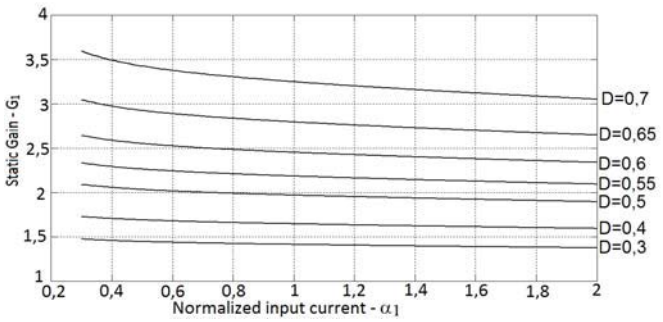
$$G_2 = \frac{V_{C1}}{V_i} = \frac{1}{1 - D - \frac{1}{T_s \omega_{02}}\left(-\alpha_2 + \frac{1}{2\alpha_2(1+G_1)}\right)} \quad (42)$$

$$G = \frac{V_0}{V_i} = G_1 G_2 \quad (43)$$

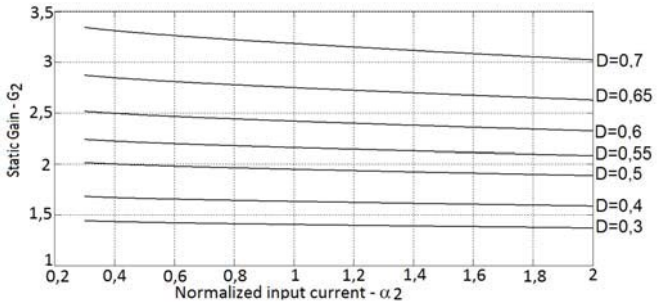
T_s - Switching period.

D - Duty cycle.

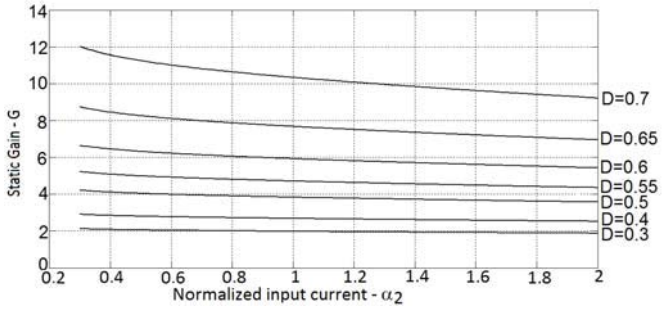
The expressions of the static gain are illustrated in Figure 6.



(a) Static gain G_1 as a function of normalized input current α_1 when duty cycle D varied.



(b) Static gain G_2 as a function of normalized input current α_2 when duty cycle D varied.



(c) Static gain G as a function of normalized input current α_2 when duty cycle D varied.

Fig. 6. Static gain curves.

According to the expressions, it appears clearly that total static gain G (Figure 6) is always higher compared to the conventional boost converter. Thus it seems more appropriate to develop the new quadratic converter which has high conversion ratio in a large range of duty cycle.

III. DESIGN PROCEDURE

Design of conventional quadratic PWM converters has been well presented in [17]. Thus, it is more significant to focus on design procedures of the auxiliary circuit. First, specify the converter choosing: switching frequency (f_s), output power (P_o), output voltage (V_o), input voltage (V_i), resonant frequency (f_o). Determine I_o ($I_o=P_o/V_o$), α_1, α_2 and D from Figure 6, and observing the operating region according to Figure 4. The resonant inductors and resonant capacitor are the most important components when designing the auxiliary circuit. The proposed auxiliary resonant circuit provides soft-switching conditions for the main switch. The following design procedure is developed considering procedures such as those presented previously in [9-12].

Snubber inductor L_{r1} is selected to allow its current to decrease from the maximum L_{b2} current to zero within t_r time, during the turn-on of the main switch. In this case, from (9), it can be written. Here t_r is the rise time of the transistor.

$$L_{r1}(t) \geq (V_o / I_{Lb2mac})t_r \quad (44)$$

Snubber inductor L_{r2} is selected to permit its current to rise up to at most the maximum input current within t_r time, during the turn-on of the main switch. In this case, from (11), it can be written.

$$L_{r2} \geq (V_{C1} / I_{i\max})t_r \quad (45)$$

Snubber capacitor C_r is selected to be discharged from V_{c1} to zero with the maximum input and L_{b2} currents over at least the time period t_f during the turn-off of the transistor. For this state, according to (25) it is obttained: Here, t_f is the fall time of the transistor.

$$C_r \geq [(I_{i\max} + I_{Lb2\max}) / V_{C1}]t_f \quad (46)$$

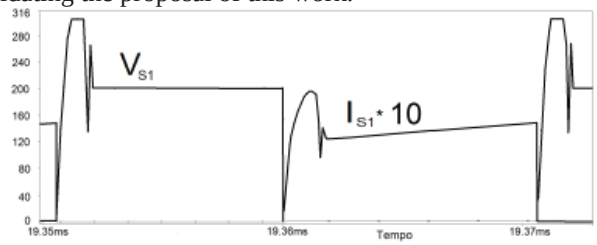
IV. SIMULATION AND EXPERIMENTAL RESULTS

The converter is simulated using simulation software ORCAD®. Figure 7 (a-b) shows the simulation results of the proposed converter. A prototype of the proposed converter, as shown in Figure 2, has been built in the laboratory. The experimental waveforms obtained in laboratory are shown in Figure 8 (a-e), and were acquired using a THS720 Tektronix® oscilloscope and a Tm 502A Tektronix® current gauge. Due to limitation of the power supply and laboratory equipment, the newly proposed converter operates with an input voltage V_i=50V, output voltage V_o=200V, output power of 400W and a switching frequency of 50kHz. The major parameters and components are given in Table 1.

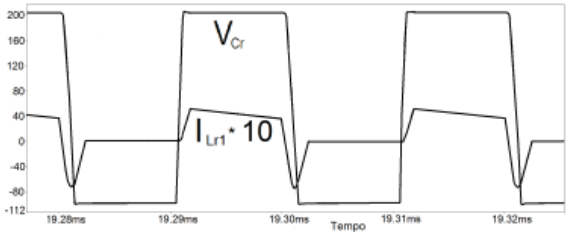
TABLE I
Components used in the proposed converter

Components	Simulation	Experiment
Main Switch (S)	Ideal	SK 60 GAL 125
Diodes (d_1,d_3,d_5)	Ideal	APT 30D100B
Diodes (d_4, d_2)	Ideal	APT 30D100B
Resonant inductor (L_{r1})	15 nH	15 nH
Resonant inductor (L_{r2})	3.5 nH	3.5 nH
Resonant capacitor (C_r)	20.4 nF	3x6.8nF
Filter inductor (L_{b1})	450 µH	450 µH
Filter inductor (L_{b2})	545 µH	545 µH
Filter capacitor (C_1)	330 µH	330 µH
Output capacitor (C_o)	330 µF	330 µF

It is noted from Figures 7(a) and 8(a) that the main switch S_1 is turned on under ZCS. The main switch takes the load current and the charging current of the resonant capacitor. The capacitor starts to transfer its stored energy to resonant inductor L_{r1} during the turn-on period of main switch. The converter has not exceeded the voltage limits; however, the current stress is slightly higher for a very short period of time. The main switch also switches off under ZVS. The current and voltage wave shapes are similar to theoretical waveforms. At the time of switching, voltage is induced across the stray inductance of the power circuit because of di/dt from the main current. This can be minimized with designs to reduce stray inductance and stray resistance such as making patterns appropriate to minimize oscillations. Unfortunately, it was not possible to eliminate completely the discrepancy between theoretical and practical values due to parasitic oscillation. After the commutation transient it is possible to see that the switch's voltages are clamped, validating the proposal of this work.



(a) Main switch voltage V_{S1} and current I_{S1}.

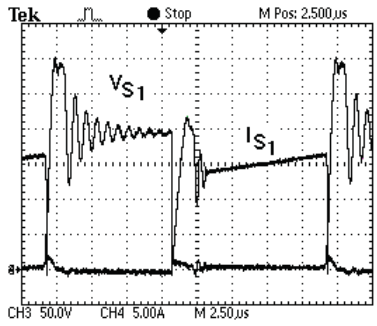


(b) Resonant voltage V_{CR} and current I_{Lr1}.

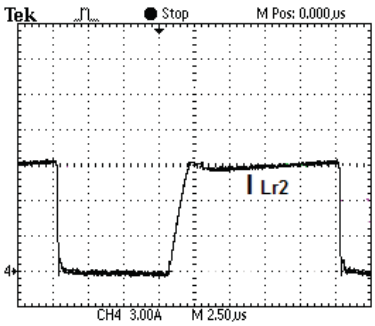
Fig. 7. Simulation results.

An Insulated Gate Bipolar Transistor (IGBT) is a more attractive device for high power and high voltage applications. The major problem of IGBT for operation at high frequency is the "current tailing". At turn-off the device current does not fall rapidly but a considerable portion of the current lingers or tails for a longer time. The co-existence of tail current and high collector-to-emitter voltage of IGBT cause high turn-off switching losses. This sets the upper limit on the switching frequency of an IGBT. On the other hand, IGBT can achieve smaller turn-on losses by using a better freewheeling diode (FWD). When di/dt increases, over-current of IGBT and over-voltage stress of FWD increases [20], this way the proposed soft switching technique could be an advantage because minimizes the di/dt.

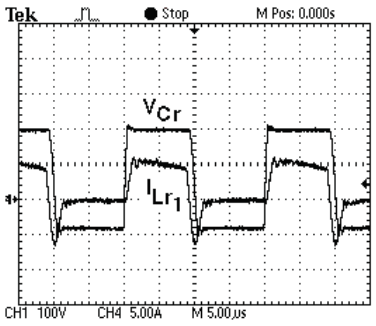
It can be seen in Figures 7(b) and 8(c) that after switch is turned off under ZVS, capacitor C_r is charged. As soon v_{cr} reaches (V_o-V_{c1}), the resonance starts between C_r and L_{r1}. Figure 8(b) shows that inductor current i_{Lr2} charges linearly providing ZCS. Figure 8(d) shows the current in filter inductors L_{b1} and L_{b2}. The small oscillation is due to the inductance value.



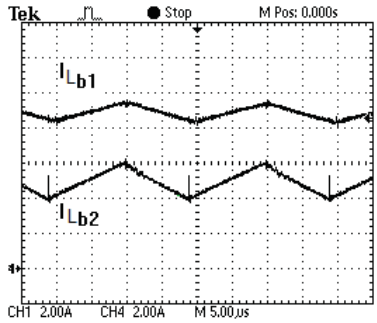
(a) Main switch voltage V_{S1} and current I_{S1}.



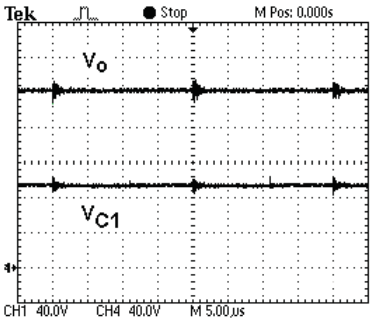
(b) Resonant current I_{Lr2}.



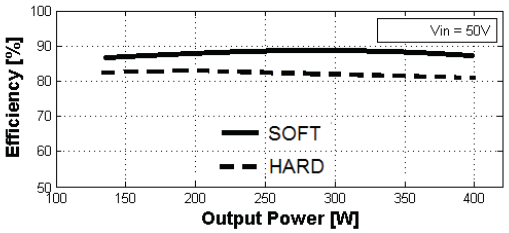
(c) Resonant voltage V_{CR} and current I_{Lr1}.



(d) Current in inductors L_{b1} and L_{b2}



(e) Output voltage (V_o) and Capacitor C_1 voltage (V_{C1})



(f) Curve of efficiency versus output power.

Fig. 8. Experimental results

Figure 8(e) shows the voltage step up obtained with the proposed circuit. As expected, one can see that output voltage increases in the converter. The efficiency of the power circuit reached at nominal load is equal to 86%, as shown in Figure 8(f). These values were obtained using a Yokogawa® WT230 Digital Power Meter. To provide a comparative analysis about the efficiency levels achieved with the laboratory prototype, a converter without the proposed soft-commutation cell was also built in the laboratory using the same layout and the same components. Thus, in this situation, one can conclude that significant efficiency improvements can be achieved with the application of the proposed soft commutation cell.

V. CONCLUSION

In this study, a new DC-to-DC converter topology with quadratic conversion ratio using a single active switch to achieve soft switching is investigated. This solution permits to reach high conversion ratio without duty cycle too close to one and with better efficiency than the classical quadratic boost converter.

In addition, the possibility of increasing the switching frequency due to soft switching characteristics makes it possible to reduce the reactive elements of these structures. The presented converter can be interesting for higher power and higher output voltage. It can be also interesting for applications where a high voltage ratio is necessary, what can be the case of fuel cell applications, but only when transformer isolation is not required.

ACKNOWLEDGEMENT

The authors gratefully acknowledge the CNPq (National Council of Scientific and Technological Development) by the Postdoctoral study grant provided to Lúcio dos Reis Barbosa (Process number 150627/2010-6).

REFERENCES

[1] Q. Zhao and F. Lee, "High-efficiency, high step-up dc-dc converters,", *IEEE Trans. on Power Electron..*, vol. 18, no. 1, pp. 65-73, Jan. 2003

[2] R. Wai and R. Duan, "High step-up converter with coupled-inductor" *IEEE Trans. on Power Electron.,* vol. 20, no. 5, pp. 1025-1035, Sep. 2005.

[3] R. Wai and R. Duan, "High-efficiency power conversion for low power fuel cell generation system." *IEEE Trans. on Power Electron.*, vol. 20, pp. 847-856, Jul. 2005.

[4] D. Maksimovic, S. Cuk, "General properties and synthesis of PWM dc-dc converters," in *IEEE 1989 Power Electronics Spec. Conf.*, 1989, pp. 515-525, 1989.

[5] M. Lopez, J. Ramos, E. Gutierrez, L Saldierna, J. Ibarra, "Current-Mode control for a quadratic boost converter with a single switch", in *IEEE 2007 Power Electronics Specialists Conference*, pp. 2652-2657, June 2007.

[6] D. Maksimovic, S. Cuk, "Switching converters with wide DC conversion range", *IEEE Transactions on Power Electronics*, vol. 6, no. 1, pp. 151-157, Jan. 1991.
[7] Y. Novaes, A. Rufer, I. Barbi, "A new quadratic, three-level, dc/dc converter suitable for fuel cell applications", *Power Conversion Conference*, pp. 601–607, 2007.
[8] R. Kadri, J. Glaubert, G. Champenois, M. Mostefai, "Performance, analysis of transformless single switch quadratic boost converter for grid connected photovoltaic systems", *ICEM'2010*, pp. 1–7, 2010.
[9] S. Bassan, G. Moschopoulos, "Properties and applications of quadratic converters," in *IEEE 2007 Canada Electrical Power Conf.*, pp. 123-127, 2007.
[10] W. Silva, D. Rodovalho, F. Silva, J. Morais, L. Freitas, E. Coelho, J. Vieira Jr "Conversor boost quadrático-buck utilizado no acionamento de um vetor de LED empregado no tratamento de disfunções celulares," *Eletrônica de Potência*, vol. 16, pp. 204-211, Jun. 2011.
[11] J. Britto, F. Silva, E. Coelho, L. Freitas, V. Farias, J. Vieira Jr, "Proposta de um conversor cc-cc utilizado em sistemas fotovoltaicos e rede de energia elétrica para faixa de tensão universal," *Eletrônica de Potência*, vol. 14, pp. 165-172, Agosto 2009.
[12] L. Barbosa, J. Vieira, L. Freitas, M. Vilela, V. Farias, "A buck quadratic PWM sof-switching converter using a single active switch," *IEEE Transactions on Power Electronics*, vol. 14, pp. 445-453, May 1999.
[13] V. Pacheco, A. Nascimento, V. Farias, J. Vieira, L. Freitas, "A quadratic buck converter with lossless commutation," *IEEE Transactions on Industrial Electronics*, vol. 47, pp. 264-272, April 2000.
[14] A. Pereira, C. Treviso, L. Barbosa, J. Rossi, M. Almeida, "A stressless buck quadratic PWM soft-switched converter," in *IEEE 2002 International Telecommunications Energy Conf.*, pp. 150-155, 2002.
[15] L. Barreto, E. Coelho, V. Farias, L. Freitas, J. B. Vieira, "A quasi-resonant quadratic boost converter using a single resonant network", *IEEE Transactions on Power Electronics*, vol. 52, pp. 552–557, 2005.
[16] T. Wu, S. Liang, "A systematic approach to developing single-stage soft switching PWM converters," *IEEE Transactions on Power Electronics,* vol. 16, pp. 581-593, no. 5, September 2001.
[17] L. Barbosa, "A zero-voltage-transition interleaved boost converter and its application to PFC," *Advances in Power Electronics*, vol. 2011, pp. 1-10, Dec. 2011.
[18] I. Matsuura, K. Smith, K. Smedley, "A comparison of active and passive soft switching methods for PWM converters," in *IEEE 1998 Power Electronics Specialists Conference*, pp. 94-100, 1998.
[19] L. Barbosa, J. Vieira Jr., L. Freitas, V. Farias, "Um conversor boost PWM com comutação não dissipativa com uma única chave ativa", *SBA*, vol. 11, nº 1, 2000.
[20] K. J. Um, "Application note 9020: IGBT Basic II" Fairchild Semiconductor, 2002.

BIOGRAPHIES

Lúcio dos Reis Barbosa received the B.S., M.S. and the Ph.D. degrees in electrical engineering from Federal University of Uberlândia, Brazil, in 1992, 1996 and 1999, respectively. In 2011 he conducted Postdoctoral study at the Nucleus of Research in Power Electronics, Federal University of Uberlândia. Since 1999, he has been with the Electrical Engineering Department, State University of Londrina, Brazil, where he is currently an Associate Professor. His research interests include converter topologies and soft switching techniques. Dr. Barbosa is a member of the Brazilian Society of Power Electronics (SOBRAEP).

Leandro Sousa Vilefort received the B.S. and the M.S. degrees in electrical engineering from Federal University of Uberlândia, Brazil, in 2008 and 2011, respectively. Currently, he is conducting the Ph.D. in electrical engineering at the Federal University of Uberlândia. His research interests include developing and modeling of power converters and soft switching techniques. Mr. Vilefort is a member of the Audio Engineering Society (AES).

Fábio Vincenzi Romualdo da Silva received the B.S., M.S. and the Ph.D. degrees in electrical engineering from Federal University of Uberlândia, in 2000, 2003 and 2007, respectively. He is currently with the Nucleus of Research in Power Electronics, Federal University of Uberlândia. His research interests are power electronics, in particular, new converter topologies. Dr. Vincenzi is a member of the Brazilian Society of Power Electronics (SOBRAEP).

Ernane Antonio Alves Coelho received the B.S degree in electrical engineering from Federal University of Minas Gerais, in 1987, the M.S. degree from Federal University of Santa Catarina, in 1989 and Ph.D. degree from Federal University of Minas Gerais in 2000. He is currently with the Nucleus of Research in Power Electronics, Federal University of Uberlândia. His research interests are PWM inverters and digital control. Dr. Coelho is a member of the Brazilian Society of Power Electronics (SOBRAEP).

Luiz Carlos Gomes de Freitas received the B.S., M.S. and the Ph.D. degrees in electrical engineering from Federal University of Uberlândia, Brazil, in 2001, 2003 and 2006, respectively. He is currently with the Nucleus of Research in Power Electronics, Federal University of Uberlândia. His research interests include power-factor-correction and new topologies. Prof. Gomes de Freitas is a member of the Brazilian Society of Power Electronics (SOBRAEP).

Luiz Carlos de Freitas, received the M.S. and Ph.D. degrees from the Federal University of Santa Catarina, Brazil, in 1985 and 1992, respectively. He is currently with the Nucleus of Research in Power Electronics, Federal University of Uberlândia. He has published in IEEE (Jan. 1995), the evolution of a zero-voltage-transition commutation cell that has been largely applied in power electronics research. Dr. de Freitas is a member of the Brazilian Society of Power Electronics (SOBRAEP).

João Batista Vieira Jr. received the B.S degree in electrical engineering from Federal University of Uberlândia, Brazil, in 1980, the M.S. and Ph.D. degrees from the Federal University of Santa Catarina, Brazil, in 1984 and 1991, respectively. He is currently with the Nucleus of Research in Power Electronics, Federal University of Uberlândia. His research interests include high-frequency power conversion and new converter topologies. Prof. Vieira is a member of the Brazilian Automatic Society (SBA) and the Brazilian Society of Power Electronics (SOBRAEP).