AC–DC SERIAL-INTERLEAVED BOOST CONVERTER APPLIED IN A SINGLE-STAGE PFC

Cícero S. Postiglione, André L. Fuerback, Claudinor B. Nascimento, Denizar C. Martins, Arnaldo J. Perin
Federal University of Santa Catarina
Department of Electrical Engineering – Power Electronics Institute
P. O. Box 5119, Zip Code: 88040-970 – Florianopolis, SC – Brazil
denizar@inep.ufsc.br

***Abstract* – This paper presents single-stage power factor corrected (PFC) AC–DC converters based on a modified serial-interleaved boost converter. The topologies are a composition of a modified interleaved boost converter with a DC–DC converter. The interleaving allows each boost converter to operate in discontinuous conduction mode (DCM) while still having continuous conduction mode (CCM) input current. High power factor and reduced current ripple are obtained, meeting IEC 61000-3-2 regulations for wide load range. The converters also operate with zero voltage switching (ZVS) resulting in high efficiency. The steady-state analysis of the converter is performed along with the description of the converter operation stages. Finally, a simplified design procedure is proposed, from where a prototype is designed and built. Finally experimental results from a laboratory prototype are presented.**

***Keywords* – AC–DC Power Conversion, Power Quality, Switched Mode Power Supplies.**

I. INTRODUCTION

When the IEC 61000-3-2 came into effect in 2001, high PF with low Total Harmonic Distortion (THD) became a requirement for electronic equipments sold in most of Europe. Soon, Britain, Japan and China adopted similar standards, developing a worldwide market. In 2006, the power factor correction (PFC) market (both passive and active) was of about 1.3 billion units and a compound annual growth rate of 11.4% is expected, increasing to 2.2 billion units in 2011 [1]. This market motivated the study and development of low-cost PFC solutions. Despite a global economic slowdown, the outlook for the worldwide embedded AC–DC power supply market is expected to remain strong. Evolving powering architectures, packaging trends, and global standards for improvements in energy efficiency are being combined with developments in advanced components and new markets for AC–DC power and to create new opportunities for manufacturers of AC–DC power supplies [2].

Passive PFC is not recommended for applications above 100 W owing to size and weight constrains [3]. For such cases, high-frequency switch-mode PFC converters are more suitable. The most common active PFC technique is the two-stage approach, which consists of the addition of a front-end converter for PFC, typically a boost converter, to the DC–DC converter. However, the overall efficiency is reduced, since the input power is processed twice. Also, the additional converter and its control circuitry lead to high cost for low-power applications [4]. Over the past years, single-stage PFC solutions have been developed [3]-[20] as an attempt to overcome these drawbacks.

Single-stage techniques integrate the PFC stage with the DC–DC converter, producing a single AC–DC converter. Unfortunately, most of the proposed single-stage topologies, especially those based on a single-power switch and/or operating in discontinuous conduction mode (DCM), suffer from low efficiency owing to switching losses, high current stress, high voltage on the DC-link capacitor and high electromagnetic interference (EMI) noise[5]. The search for more efficient topologies led to complex converters. Some authors have even suggested the use of full-bridge and LCC resonant converters, which could cost as much as a two-stage solution, owing to the large number of components and auxiliary circuits required. Therefore, the advantages over the two-stage approach in these cases are minimal [19].

In this work, single-stage PFC converters suitable for low power (75–600 W) SMPS are presented. The main advantages of the proposed converters are high PF and high efficiency. The converter topology is based on a modified serial interleaved boost converter. This technique is also known as charge-pump power-factor-correction (CPPFC) technique, typically used in electronic ballasts and known for its high PF with the addition of few passive elements[6]–[15], thus presenting low cost and high power density.

II. PROPOSED CONVERTER

In this paper, a modified series interleaved boost converter is used to perform PFC, and different DC–DC converters can be integrated to perform the voltage step-down and provide galvanic isolation. The proposed PFC converter is based on those proposed by [13] in 1994 and [14]. The advantage of these topologies over most single-stage techniques is the interleaving effect of the input current, signifying that the current through inductors L_1 and L_2 can be discontinuous, but the input current will be continuous, thus reducing or in some cases, eliminating the additional input filter. Also, these serial interleaved topologies benefit from zero-voltage switching (ZVS) naturally, resulting in higher efficiency.

Topologies proposed in [13], [14] and [15] suffer from high-voltage spikes across the bridge diodes, sometimes leading to component failure. This problem is eliminated in the proposed converter by moving the inductors from the DC to the AC side. Nevertheless, the bridge diodes operate at the switching frequency, requiring fast-recovery devices, but the bridge diodes are naturally blocked each switching cycle.

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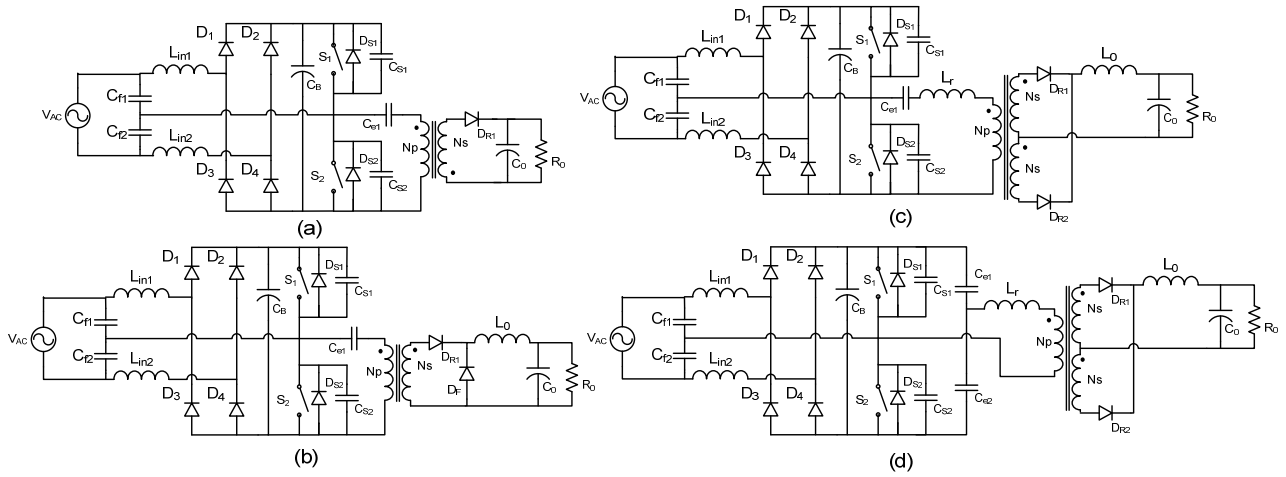

Fig. 1. Proposed AC–DC converters: (a) PFC integrated with a flyback converter, (b) PFC integrated with a forward converter, (c) PFC integrated with an AHB converter, and (d) PFC integrated with a SHB converter.

Figure 1 shows the integration of the modified serial interleaved boost with different ZVS DC–DC converters resulting in four different single-stage converters. The first is integrated with a Flyback, the second with a Forward, and the third and fourth with asymmetrical half-bridge (AHB) and symmetrical half-bridge (SHB) converter, respectively. Both the PFC and DC–DC converters share the same power switches, which is a characteristic of single-stage topologies. In 2005, Do et al. [16], [17] presented a similar topology to the one proposed in Figure 1 (a), but with a different approach for the input inductors, which were coupled. The problem with using coupled inductors is the necessity of a large leakage inductance with the same magnitude as the magnetizing inductance, which results in difficult practical implementation without the addition of external inductors. The converters presented in Figure 1 (a) and (b) have been proposed in this work. The SHB was proposed in [12], and the only difference with the AHB is the combination of the SHB capacitors into one capacitor with double capacitance, which is more attractive for practical implementation.

For the sake of brevity, this paper only presents the study of the PFC converter integrated with the SHB pulse width modulated with ZVS (HB-PWM-ZVS). To simplify the analysis, the PFC stage and the DC–DC converter are studied separately. This is made possible by the presence of the DC-link capacitor, which decouples both the stages. The only elements common to both the stages are the power switches, which handle the sum of the currents of both the stages.

III. PFC STAGE – CONVERTER OPERATION

In the present analysis, the input voltage is considered to be in its positive half-cycle, and the circuit is in steady-state operation with a constant switching frequency, fs. The switching frequency is considered high enough to assume that the input voltage $V_i(t)$ is constant during one switching period. The input capacitors C_{f1} and C_{f2} have the same capacitance values and are large enough to consider the voltage across them constant during one switching period. Inductors L_{in1} and L_{in2} and capacitors C_{S1} and C_{S2} have the same values of inductance and capacitance, respectively. The DC-link voltage is higher than the mains peak voltage, and the ripple is negligible because the DC-link capacitor, C_B, has a large value. All the components are assumed to be ideal.

The operation stages are subsequently summarized and shown in Figure 2. The main waveforms for each time interval are presented in Figure 3.

Interval 1 – (t_0, $t_{0'}$): At the instant before t_0, switch S_2 was conducting and the current through L_{in2} was increasing. At t_0, S_2 is turned off and C_{s1} subsequently starts to discharge and C_{s2} begins to charge. Thus, the voltage across S_1 decreases and across S_2 increases. At $t_{0'}$, the switch voltage V_{S1} is zero and V_{S2} is equal to the DC-link voltage V_B.

Interval 2 – ($t_{0'}$, $t_{0''}$): At $t_{0'}$, when voltage V_{S1} reaches zero, S_1's anti-parallel diode starts to conduct. The current through L_{in2} decreases linearly, charging the DC-link capacitor C_B. The current through L_{in1} starts to increase linearly owing to the voltage imposed by C_{f1}. During this time interval, switch S_1 is commanded to conduct.

Interval 3 – ($t_{0''}$, t_1): At $t_{0''}$, the increasing current through inductor L_{in1} reaches the same value of the current through L_{in2}, dropping the diode current to zero. From this moment, S_1 takes on the current. At t_1, the current through inductor L_{in2} reaches zero.

Interval 4 – (t_1, t_2): At t_1, when the current trough L_{in2} reaches zero, D_4 turns off. The input current flows through capacitor C_{f2} and the current through the inductor L_{in1} continues to increase linearly.

Interval 5 – (t_2, $t_{2'}$): At t_2, S_1 is turned off under zero voltage. Owing to the current imposed by inductor L_{in1}, C_{s2} starts to discharge and C_{s1} begins to charge, and the opposite of Interval 1 occurs.

Interval 6 – ($t_{2'}$, $t_{2''}$): This interval is similar to Interval 2, but now the body diode of S_2 is turned on.

Interval 7 – ($t_{2''}$, t_3): At $t_{2''}$, S_2 is turned on, taking on all of the currents. At t_3, the current through inductor L_{in1} reaches zero.

Interval 8 – (t_3, t_4): At t_3, when the current through L_{in1} reaches zero, D_1 turns off. The input current flows through capacitor C_{f1} and the current through inductor L_{in2} continues to increase linearly. In this interval, S_2 is turned off.

From Figure 3, the interleaving effect becomes clear, showing the input current i_{in} in CCM, even though the current through each inductor is in DCM.

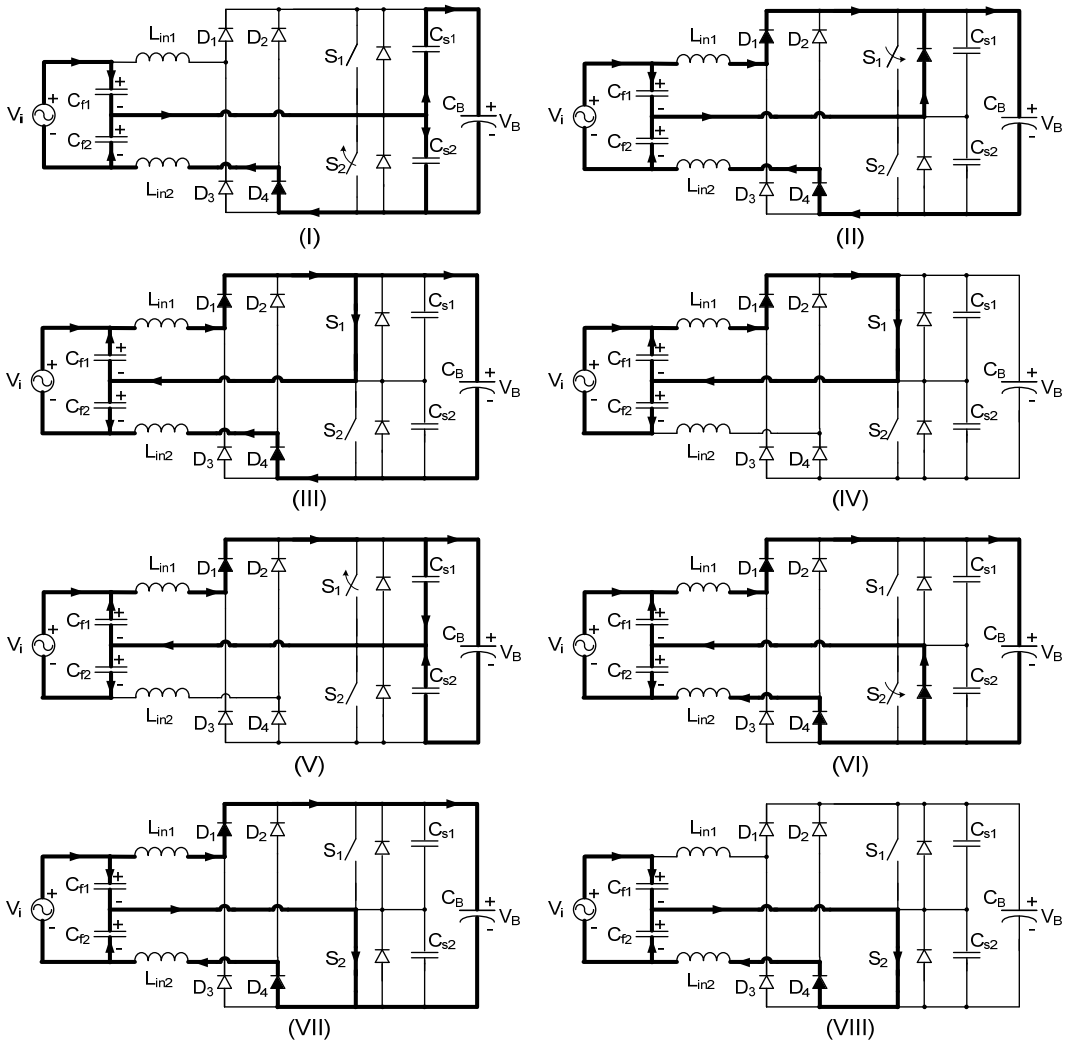

Fig. 2. Operation stages for each time interval.

A. Analysis and Design Equations

To simplify the study, the operation modes were reduced to only four, disregarding those involved in the ZVS, considering only the transitions of current through the inductors.

1) Voltage Across Input Capacitors

To obtain the current rates through L_{in1} and L_{in2}, it is necessary to obtain the voltage across capacitors C_{f1} and C_{f2}. Unlike the AHB-PWM, in this converter the ratio between the input capacitors voltage is not (1−D)/D. The following study analyzes the boundary condition for DCM of the current through the input inductors to guarantee DCM operation. In this particular condition, the time intervals t_2−t_1 and t_4−t_3 tend to zero. For this study, the currents were considered linear, which is true if the input capacitors are large enough (but not bulky – less than a microfarad). Further, a condition will be given to validate this statement.

The voltage ratios across the input capacitors are defined in (1).

$$\alpha_1 = \frac{V_{Cf1_{pk}}}{V_B} \quad , \quad \alpha_2 = \frac{V_{Cf2_{pk}}}{V_B} \tag{1}$$

where

$$\alpha = \alpha_1 + \alpha_2 \tag{2}$$

and α is defined as

$$\alpha = \frac{V_{in_{pk}}}{V_B} . \tag{3}$$

The peak current through inductors L_{in1} and L_{in2} can be obtained using (4).

$$I_{Lin1_{pk}} = \frac{V_{Cf1}}{L_{in}} \Delta t_1 \quad , \quad I_{Lin2_{pk}} = \frac{V_{Cf2}}{L_{in}} \Delta t_3 \tag{4}$$

And the peak current during the grid voltage half-cycle is

$$I_{Lin1_{pk}}(t) = \frac{V_{Cf1_{pk}} \sin(\omega t)}{L_{in}} \Delta t_1 \ , \ I_{Lin2_{pk}} = \frac{V_{Cf2_{pk}} \sin(\omega t)}{L_{in}} \Delta t_3 \tag{5}$$

The time intervals Δt_1 and Δt_3 are known and given by (7), and the time intervals Δt_2 and Δt_4 are unknown. However, the current variation is the same during magnetizing and de-magnetizing of the inductors, and thus, the following relation can be written:

$$\Delta t_1 \Delta i_{Lin1} = \Delta t_2 \Delta i_{Lin1} \ , \ \Delta t_3 \Delta i_{Lin2} = \Delta t_4 \Delta i_{Lin2} \tag{6}$$

$$\Delta t_1 = DT_s \ , \ \Delta t_3 = (1-D)T_s = D'T_s \tag{7}$$

Writing the equations for the magnetizing and de-magnetizing inductor L_{in1}, and making them equal results in

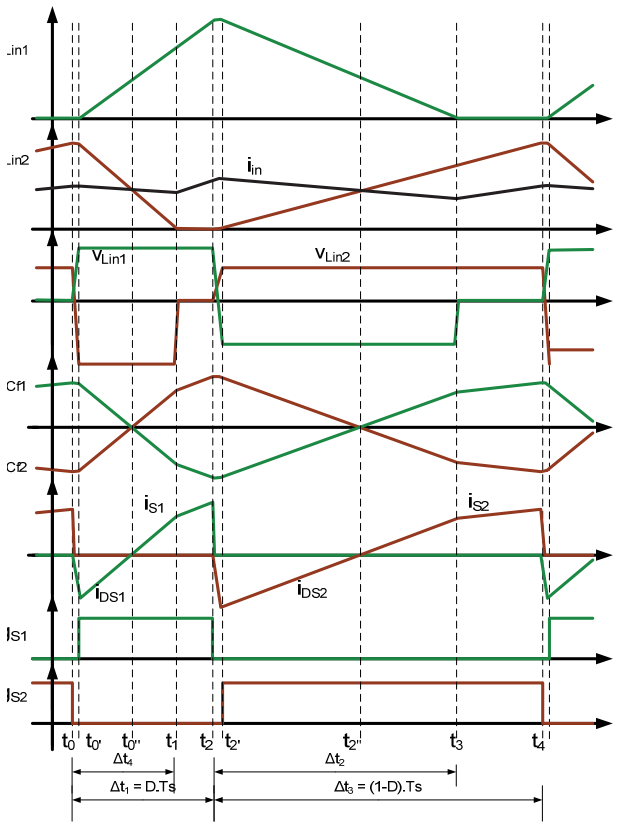

Fig. 3. Main waveforms of the PFC converter for one switching cycle.

$$\frac{V_{Cf1_{pk}}\sin(\omega t)}{L_{in}}\Delta t_1 = \frac{V_B - \left(V_{Cf1_{pk}}\sin(\omega t)\right)}{L_{in}}\Delta t_2 . \quad (8)$$

Isolating Δt_2 and using the voltage in terms of α leads to (9)

$$\Delta t_2 = \frac{\alpha_1 \sin(\omega t)}{1-\alpha_1 \sin(\omega t)} DT_s . \quad (9)$$

Repeating the same equations for inductor L_{in2} leads to

$$\Delta t_4 = \frac{\alpha_2 \sin(\omega t)}{1-\alpha_2 \sin(\omega t)}(1-D)T_s . \quad (10)$$

As only one inductor can operate in critical conduction mode, it is necessary to determinate what happens to Δt_4 and Δt_2 when L_{in1} is in the critical conduction mode and the current through L_{in2} is critical, respectively.

By assuming that inductor L_{in1} operates in critical conduction mode and knowing that the maximum value for Δt_2 occurs at the input voltage peak, from (9),

$$\Delta t_{2\max} = \frac{\alpha_1}{1-\alpha_1} DT_s . \quad (11)$$

When in critical conduction mode, the time interval Δt_2 tends to Δt_3, therefore substituting these relation in (11) leads to a restriction for D

$$(1-D)T_s = \frac{\alpha_1}{1-\alpha_1} DT_s . \quad (12)$$

Solving (12) leads to (13), which is the condition for critical conduction mode of inductor L_{in1}. Given this condition, it is possible to calculate the time interval of Δt_4, as shown in (14).

$$\alpha_1 = 1-D \quad (13)$$

$$\Delta t_{4\max} = \frac{\alpha_2}{1-\alpha_2}(1-D)T_s \quad (14)$$

From (2) a second restriction is obtained and expressed by (15).

$$\alpha_2 = \alpha - (1-D) \quad (15)$$

The next step is to determine Δt_2 for the critical conduction mode of L_{in2}. In this case, Δt_4 tends to D, therefore repeating the same procedure leads to two conditions for the boundary conduction of L_{in2}. These conditions are presented in (16)

$$\alpha_1 = \alpha - D \quad \& \quad \alpha_2 = D . \quad (16)$$

As the conduction interval has to be divided between both the inductors, the energy balance forces the voltage across the capacitors to the mean value between both the conditions, which is mathematically represented in (17) and (18)

$$\alpha_1 = \frac{(1-D)+(\alpha-D)}{2} = \frac{\alpha-(2D-1)}{2}, \quad (17)$$

$$\alpha_2 = \frac{\alpha-(1-D)+D}{2} = \frac{\alpha+(2D-1)}{2} . \quad (18)$$

By substituting (17) and (18) in (1), the peak voltages across the input capacitors C_{f1} and C_{f2} are given by (19) and (20), respectively

$$V_{Cf1_{pk}} = \frac{V_{in_{pk}} - V_B(2D-1)}{2}, \quad (19)$$

$$V_{Cf2_{pk}} = \frac{V_{in_{pk}} + V_B(2D-1)}{2} . \quad (20)$$

Equations (19) and (20) demonstrate the dependence of the voltage across the capacitors with parameter α. In addition, there is a limit for α at each duty-cycle D that guaranties voltages higher than zero across the capacitors, given by (21)

$$\frac{\alpha-(2D-1)}{2} \geq 0 \quad \& \quad \frac{\alpha+(2D-1)}{2} \geq 0 , \quad (21)$$

or, isolating D in (21) gives:

$$\frac{1+\alpha}{2} \geq D \geq \frac{1-\alpha}{2} . \quad (22)$$

Once the voltages across the input capacitors are known, the conduction intervals of the input inductors Δt_2 and Δt_4 can also be calculated.

2) Input Current

The input current can be obtained by using Kirchhoff's current Law, which yields

$$i_{in} = i_{Lin1} + i_{Cf1} = i_{Lin2} + i_{Cf2} . \quad (23)$$

Another expression for the input current can be obtained by expressing the average current during one switching period

$$i_{in} = \frac{\left(i_{Lin1}+i_{Cf1}\right)+\left(i_{Lin2}+i_{Cf2}\right)}{2} . \quad (24)$$

By applying the Kirchhoff's current law to the input nodes, current through C_{f1} is equal to minus the current through C_{f2}; therefore, (24) becomes (25)

$$i_i = \frac{i_{Lin1}+i_{Lin2}}{2} . \quad (25)$$

If the input current ripple is disregarded, the average input current can be obtained as the sum of the average current through the input inductors. The average value of the current through inductor L_{in1} during one switching period is given by:

$$\hat{I}_{Lin1} = \frac{1}{T_s}\frac{i_{Lin1_{pk}}}{2}\Delta t_1 + \frac{1}{T_s}\frac{i_{Lin1_{pk}}}{2}\Delta t_2 . \quad (26)$$

The peak current is given in (5), where Δt_1 is equal to D and Δt_2 is given in (9). However, in this case, the instantaneous average value is used [21], and substituting in (26) and solving leads to (27), which is the value of the current through inductor L_{in1} averaged over one switching cycle [21]

$$\hat{I}_{Lin1} = \frac{D^2 V_B V_{Cf1}}{2L_{in} f_s \left(V_B - V_{Cf1}\right)} . \quad (27)$$

Following the same procedure, the averaged current through inductor L_{in2} over one switching cycle is given by (28)

$$\hat{I}_{Lin2} = \frac{\left(1-D\right)^2 V_B V_{Cf2}}{2L_{in} f_s \left(V_B - V_{Cf2}\right)} . \quad (28)$$

The averaged value of the input current is given by

$$\hat{I}_{in} = \frac{\hat{I}_{Lin1} + \hat{I}_{Lin2}}{2} . \quad (29)$$

Substituting (27) and (28) in (29) as well as the approximations for the voltage across the capacitors C_{f1} and C_{f2} given by (19) and (20), results in (30).

$$\hat{I}_{in} = \frac{D^2 V_B \left[\frac{V_{in} - V_B(2D-1)}{2}\right]}{4L_{in} f_s \left\{V_B - \left[\frac{V_{in} - V_B(2D-1)}{2}\right]\right\}} + \cdots + \frac{\left(1-D\right)^2 V_B \left[\frac{V_{in} + V_B(2D-1)}{2}\right]}{4L_{in} f_s \left\{V_B - \left[\frac{V_{in} + V_B(2D-1)}{2}\right]\right\}} \quad (30)$$

Substituting the equation for the input voltage and the definition of α gives the input current over the line voltage half-cycle.

$$i_{in}(t) = \frac{V_{in_{pk}}}{4L_{in} f_s \alpha}\frac{D^2 \sin(\omega t)\left[\frac{\alpha - (2D-1)}{2}\right]}{1 - \sin(\omega t)\left[\frac{\alpha - (2D-1)}{2}\right]} + \cdots + \frac{V_{in_{pk}}}{4L_{in} f_s \alpha}\frac{\left(1-D\right)^2 \sin(\omega t)\left[\frac{\alpha + (2D-1)}{2}\right]}{1 - \sin(\omega t)\left[\frac{\alpha + (2D-1)}{2}\right]} \quad (31)$$

Equation (31) describes the input current behavior over one half-cycle of the input voltage. However, as the converter's operation is symmetrical, the waveform is the same for the second half, except being inverted. Figure 4 shows the normalized input current waveform for one half-cycle of the input voltage and the normalized currents through inductors L_{in1} and L_{in2}. Owing the duty-cycle, the different voltage across the input capacitors is reflected on the current through the inductors. However, owing to the input voltage symmetry, the current through the inductors are interchanged every half-cycle.

3) Power Factor

With the input current and the input voltage, the active power drained from the grid can be obtained as:

$$P_{in} = \frac{1}{\pi}\int_0^{\pi}\left(V_{in}(t) i_{in}(t)\right)\partial\left(\omega t\right) = \frac{{V_{in_{pk}}}^2}{4L_{in} f_s}\Psi_2 \quad (32)$$

where

$$\Psi_2 = \frac{1}{\pi}\int_0^{\pi}\frac{D^2}{\alpha}\frac{\sin(\omega t)\left[\frac{\alpha - (2D-1)}{2}\right]}{1 - \sin(\omega t)\frac{\alpha - (2D-1)}{2}}\sin(\omega t)d\omega t + \cdots + \frac{1}{\pi}\int_0^{\pi}\frac{(1-D)^2}{\alpha}\frac{\sin(\omega t)\left[\frac{\alpha + (2D-1)}{2}\right]}{1 - \sin(\omega t)\frac{\alpha + (2D-1)}{2}}\sin(\omega t)d\omega t \quad (33)$$

The PF, given by the ratio between the active power and the apparent power, can be written as:

$$PF = \frac{P_{in}}{V_{in_{ef}} I_{in_{ef}}} = \frac{\sqrt{2}}{\sqrt{\Psi_1}}\Psi_2 . \quad (34)$$

where

$$\Psi_1 = \frac{1}{\pi}\int_0^{\pi}\left\{\frac{\sin(\omega t)}{\alpha}\left[\begin{array}{c} D^2 \dfrac{\frac{\alpha - (2D-1)}{2}}{1 - \sin(\omega t)\cdot\frac{\alpha - (2D-1)}{2}} + \\ (1-D)^2 \dfrac{\frac{\alpha + (2D-1)}{2}}{1 - \sin(\omega t)\cdot\frac{\alpha + (2D-1)}{2}} \end{array}\right]\right\}^2 d\omega t \quad (35)$$

Figure 4 (d) represents the PF as a function of α with the duty-cycle as a parameter. The limitations of α become evident for a given duty-cycle, because the voltage across the input capacitors C_{f1} and C_{f2} cannot be negative during the positive half-cycle of the line input voltage, thus respecting the limits of inequality (22). However, simulation and experimental results show the voltage across the capacitors is reflected regarding the voltage axis, never becoming negative during the positive cycle and vice-versa. This behavior is not covered by the presented design equations.

4) Static Gain Characteristic

Owing to the complexity of the converter operation, it is difficult to obtain an equation to describe the output voltage V_B as a function of the input voltage and output current. However, the output current can be expressed as a function of α, because it is the sum of the de-magnetizing current of inductors L_{in1} and L_{in2}. The average value of the current through these inductors during one switching period is given in (36).

$$\hat{I}_{Lin1} = \frac{1}{T_s}\frac{I_{Lin1_{pk}}\Delta t_2}{2} \quad , \quad \hat{I}_{Lin2} = \frac{1}{T_s}\frac{I_{Lin2_{pk}}\Delta t_4}{2} \quad (36)$$

By substituting the peak values given in (5) and the time intervals Δt_2 and Δt_4 presented in (9) and (10), respectively, in (36), (37) can be obtained.

$$I_{Lin1} = \frac{V_{Cf1_{pk}} \sin(\omega t) D^2}{2 f_s L_{in}} \frac{\alpha_1 \sin(\omega t)}{1-\alpha_1 \sin(\omega t)}$$
$$I_{Lin2} = \frac{V_{Cf2_{pk}} \sin(\omega t)(1-D)^2}{2 f_s L_{in}} \frac{\alpha_2 \sin(\omega t)}{1-\alpha_2 \sin(\omega t)} \quad (37)$$

By substituting the voltage across the capacitor and solving the equations, the output current instantaneous value can be written as given in (38).

$$I_{0\,CFP}'(t) = \frac{V_{in_{pk}} \alpha_1 D^2}{2 f_s L_{in} \alpha} \frac{\alpha_1 [\sin(\omega t)]^2}{1-\alpha_1 \sin(\omega t)} + \cdots + \frac{V_{in_{pk}} \alpha_2 \cdot (1-D)^2}{2 f_s L_{in} \alpha} \frac{\alpha_2 [\sin(\omega t)]^2}{1-\alpha_2 \sin(\omega t)} \quad (38)$$

The mean value over the grid period is given in (39).

$$I_{0\,CFP}' = \frac{1}{\pi} \int_0^{\pi} I_{0\,CFP}'(t) \partial \omega t \quad (39)$$

By solving (39) for (38) and making the pertinent approximations results in (40).

$$I_{0\,CFP}' = \frac{V_{in_{pk}}}{2\pi\alpha f_s L_{in}} D^2 \left(\frac{\alpha - (2D-1)}{2} \right) \Psi_3 + \cdots + \frac{V_{in_{pk}}}{2\pi\alpha f_s L_{in}} (1-D)^2 \left(\frac{\alpha + (2D-1)}{2} \right) \Psi_4 \quad (40)$$

where

$$\Psi_3 = -2 - \frac{\pi}{\alpha_1} + \frac{2}{\alpha_1 \sqrt{1-\alpha_1^2}} \left[\frac{\pi}{2} + \tan^{-1} \left(\frac{\alpha_1}{\sqrt{1-\alpha_1^2}} \right) \right] \quad (41)$$

$$\Psi_4 = -2 - \frac{\pi}{\alpha_2} + \frac{2}{\alpha_2 \sqrt{1-\alpha_2^2}} \left[\frac{\pi}{2} + \tan^{-1} \left(\frac{\alpha_2}{\sqrt{1-\alpha_2^2}} \right) \right]. \quad (42)$$

Normalizing the output current leads to (43).

$$\overline{I_{0\,CFP}'} = \frac{D^2}{\alpha} \left(\frac{\alpha - (2D-1)}{2} \right) \Psi_3 + \cdots + \frac{(1-D)^2}{\alpha} \left(\frac{\alpha + (2D-1)}{2} \right) \Psi_4 \quad (43)$$

where

$$\overline{I_{0\,CFP}'} = \frac{2\pi f_s L_{in}}{V_{in_{pk}}} I_{0\,CFP}'. \quad (44)$$

From (43), one can plot the output current as a function of α for different duty-cycles. Subsequently, the static gain q, which is $1/\alpha$, can be plotted as a function of the output current by rotating the graphic and mirroring it (Figure 5).

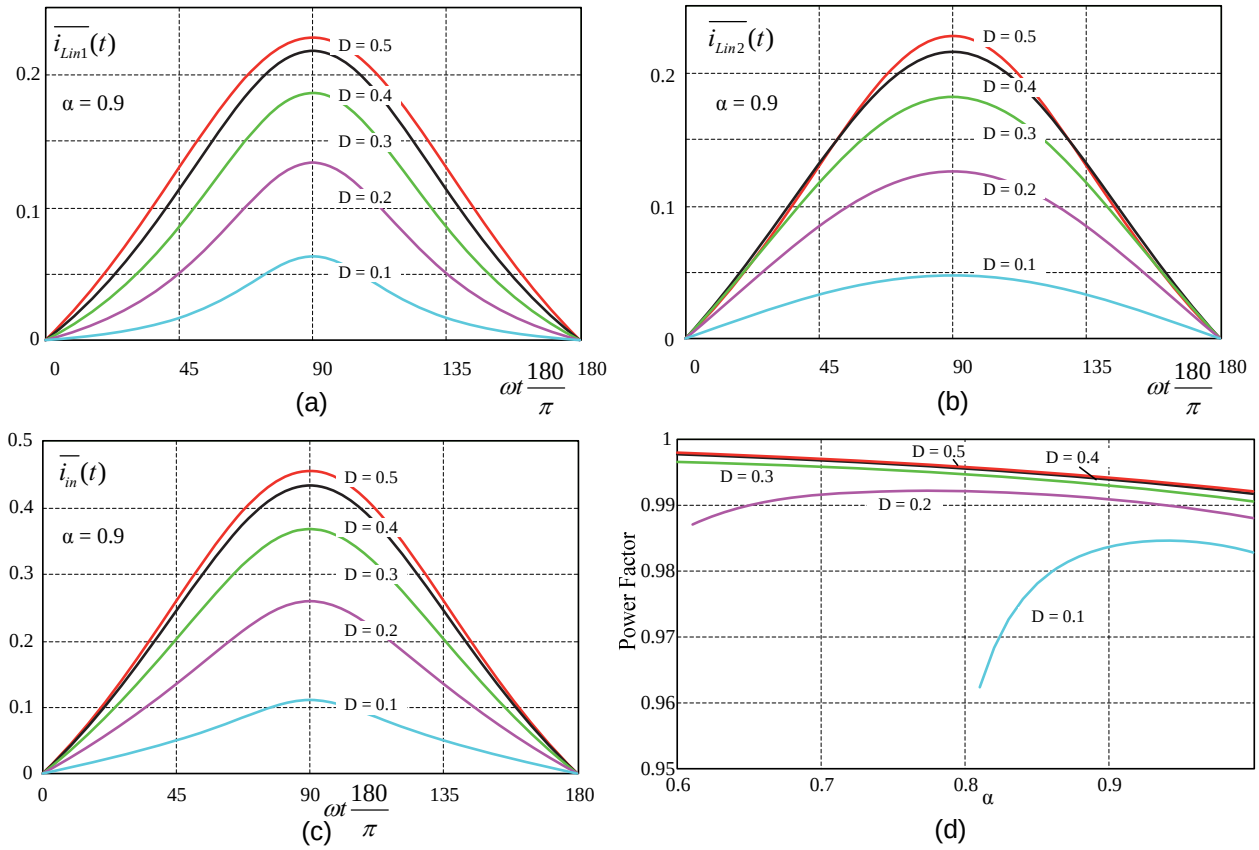

Fig. 4. Normalized current through input inductors during the positive half-cycle of input voltage: (a) Current through L_{in1}, (b) Current through L_{in2}, (c) Normalized input current with α = 0.9 for different values of duty-cycle D, and (d) Power Factor as a function of parameter α for different values of duty-cycle.

5) Parameter μ

The presented analysis was developed by assuming that the voltage across the input capacitors C_{f1} and C_{f2} is constant during one switching period. However, voltage ripple is present and is a function of the natural frequency of the elements C_f and L_{in}, and the switching frequency given in (45). The voltage ripple can be obtained through a detailed analysis of the operation stages, which is not presented here.

$$\mu = \frac{\omega_0}{\omega_s} = \frac{1}{2\pi f_s \sqrt{L_{in} C_f}} \tag{45}$$

Simulations demonstrated that if the switching frequency is 3 times higher than the natural frequency of the input circuit ($\mu_0 < 0.33$), then the current through the inductors can be approximated by ramps, and the presented analysis is valid.

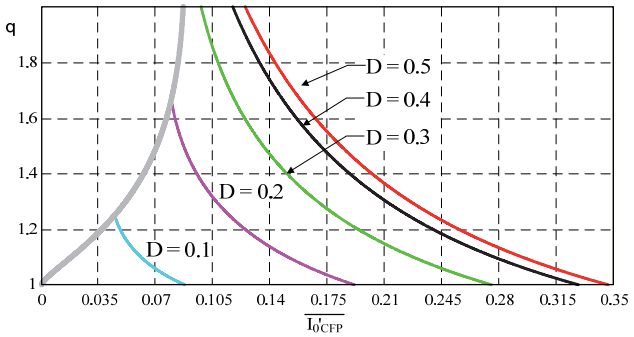

Fig. 5. Static gain as a function of the normalized averaged output current.

From (32) and (40), it is clear that the power of the circuit depends on L_{in}. Therefore, its value is determined by the design parameters, and the input capacitance is determined by parameter μ. Small values of μ leads to higher C_f capacitances, allowing the circuit to be adequately approximated by the analysis presented here. However, capacitors C_f must not have capacitances large enough to create a significant displacement between the input voltage and current. Thus, there exists a tradeoff.

IV. DC–DC STAGE

The DC–DC stage is a SHB converter with pulse-width-modulation and zero-voltage switching (SHB-PWM-ZVS).

As the SHB-PWM-ZVS is a well-known converter [22], the operation modes are not presented in this paper, and only the main design equations are summarized.

A. Design Equations

The SHB-PWM-ZVS output characteristic is presented in (46).

$$q = \frac{V'_0}{V_B} = \left[2D(1-D) - \frac{4I'_0 L_r f_s}{V_B} \right] \tag{46}$$

Owing to the presence of the resonant inductor there is a duty-cycle loss, which is proportional to the output current, as shown in (47).

$$\overline{I'_0} = \frac{4I'_0 L_r f_s}{V_B} \tag{47}$$

Substituting (47) in (46) leads to (48).

$$q = \left[2D(1-D) - \overline{I'_0} \right] \tag{48}$$

The turns ratio of the transformer can be written as shown in (49), where V'_0 represents the output voltage referred to the primary side of the transformer [12].

$$n_T = \frac{V'_0}{V_0} = \frac{V_B}{V_0} \left[2D(1-D) - \overline{I'_0} \right] \tag{49}$$

The DC-link voltage V_B is obtained through the parameter α, from the PFC stage at the rated power.

V. CONTROL

There are at least three different ways to implement the control for the proposed topology. The first one consists of driving the switches complementarily with a fixed switching frequency and the use of duty-cycle D to regulate the output voltage for load variations (47). However, as any other PFC boost operating in DCM, the DC-link voltages increase with the reduction in duty-cycle The second alternative is to use variable switching frequency by keeping the duty-cycle constant, typically at 50% [12]. The advantage is that the DC-link voltage is kept constant, but the control dynamic must be slow, and the load range is limited [12]. The third alternative consists of mixing variable switching frequency with variable duty-cycle. The idea is to use variable switching frequency to maintain the DC-link voltage under a certain value, when the output power is reduced [20], while the duty-cycle is responsible for regulating the output voltage with the desired dynamic. The use of both the techniques is possible owing to the different dynamic responses of the PFC and the DC–DC stages.

VI. SIMULATION AND EXPERIMENTAL RESULTS

To validate the presented study, simulation and experimental results for the converter, shown in Figure 1 (d), are presented. The specifications are summarized in Table I. The converter component values obtained for the given specifications are shown in Table II.

TABLE I
Prototype Specifications

Parameter	Value
Line Input Voltage – Vi	220 Vef ± 10% / 60 Hz
Output Voltage – V0	24 Vdc ± 5 %
Output Rated Power – P0	200 W
Nominal Switching frequency – fs	110 kHz
Standard	IEC 61000-3-2 Class D

TABLE II
Component Values

Parameter	Component Value
L_{in1}, L_{in2}	200 μH (E 25/06)
C_{f1}, C_{f2}	220 nF
L_f	500 μH (Fe-si, a=1 cm)
L_r	25 μH (E 20)
T_1	n_T = 6.25 (E 30/14)
C_B	100 μF
C_{e1}, C_{e2}	220 nF
L_0	20 μH (E 30/07)
C_0	4,700 μF

It is important to note that parameters α, μ, and nominal duty-cycle D must be assigned. From the presented study, the ideal values for α and D are found to be 1 and 0.5, respectively. However, unitary α is a theoretical value and cannot be achieved in practical applications. In addition, grid voltage tolerance must be taken into account in the design. The authors found that a good initial value for the α parameter was 0.92, to guarantee that the converter can deliver the rated power with reduced line input voltage, as low as 190 V. The nominal duty-cycle was observed to be 0.4 to allow compensation of load and input voltage variations. Parameter μ was chosen as 0.22, which is slightly under 0.3, and resulted in a commercial value for capacitors C_{f1} and C_{f2}. The maximum switching frequency for this prototype was 180 kHz.

The laboratory prototype was built using MOSFETs FCP11N60F for the power switches and Schottky diodes MBR20200CT as the output diodes. For the input rectifier, MUR460 diodes were used and the magnetic components are from a local company: Thornton. Higher efficiency can be

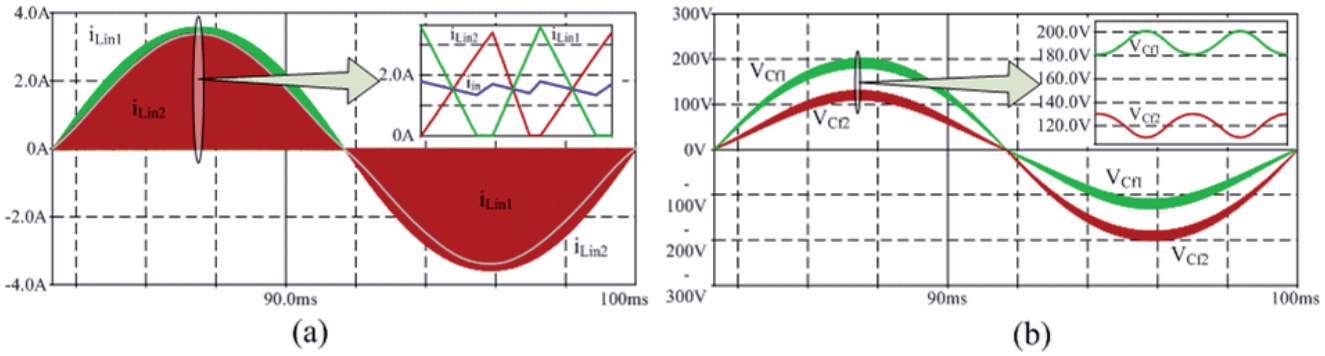

Fig. 6. Simulation results: (a) Current through inductors L_{in1} and L_{in2} and input current and (b) Voltage across input capacitors C_{f1} and C_{f2}.

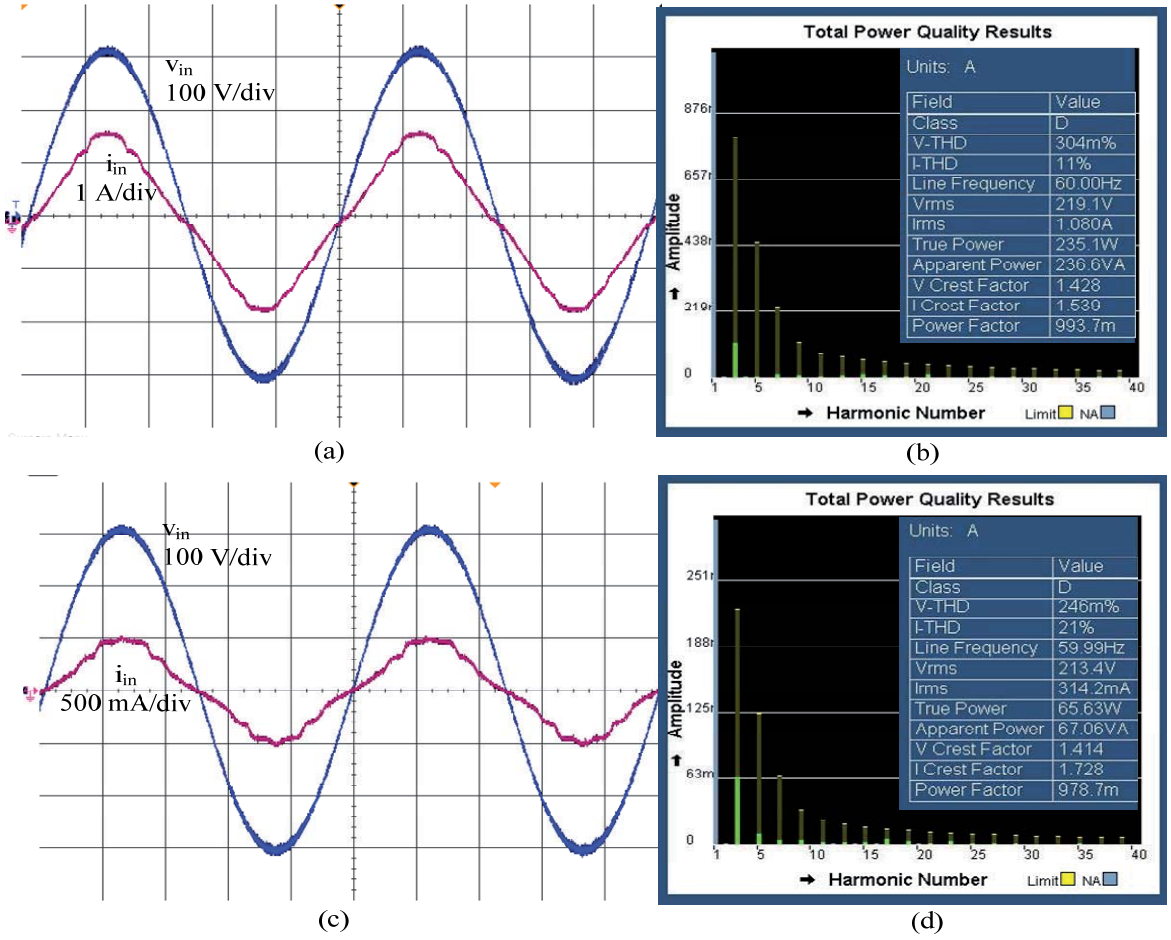

Fig. 7. Experimental results: (a) Line input voltage and current at rated power, (b) Harmonic content of line input current at rated power, (c) Line input voltage and current at 25 % of rated power, and (d) Harmonic content of line input current at 25 % of rated power.

obtained using new Silicon Carbide (SIC) diodes.

Simulation results at the rated power for the circuit operating in open loop are presented in Figure 6. The current through input inductors L_{in1} and L_{in2} during one period of the grid voltage, with a zoom on the switching period scale at the line input peak are shown in Figure 6 (a). The clear envelope delineates the peak values for currents through L_{in1} and L_{in2}. During the positive half-cycle of the grid voltage, the peak current of L_{in1} is higher than that of L_{in2} and the opposite occurs during the negative half-cycle. This is more evident when the voltage across the capacitors C_{f1} and C_{f2} is observed during the same period (Figure 6 (b)).

Figure 7 (a) and (c) present the experimental results for the line input voltage and current at 100 and 25 % of the rated power, respectively. As can be seen, PFC is achieved in both the situations. At 25 % of full load, the input current is more distorted with a THD of 22%, but the PF is still high at 0.977. The high-frequency line input voltage ripple is owing to the use of an inverter to supply power with very low voltage distortion of around 0.3 %. Figure 7 (b) and (d) show the line input power quality analysis for both the situations. The first column represents the fundamental current. The darker columns represent the IEC limits for each measurement and the brighter area at each column represents the measured values. The input current THD is 11 % and the PF obtained is 0.994 at nominal power. In both the cases, considering only the first 40 harmonics, the measurements comply with the limits of IEC 61000-3-2 Class D and Class A [23]. All the measurements for the PF were made in open-loop operation. Closed loop may influence PF and THD results, because it is meant to reduce the 120-Hz output voltage ripple. The final results will depend on the DC–DC stage dynamic response, and this topic has not been covered in this paper.

The experimental results for PF and efficiency trend curves as the functions of the output power are depicted in Figure 8. High PF, always above 97%, has been achieved for the tested range. Two efficiency curves were obtained. The highest one with constant switching frequency of 110 kHz, and increasing the switching frequency at low power to reduce the DC link voltage. When the output power goes under 50 %, the converter starts to work with hard switching during the zero crossing of the line input voltage and increasing the switching frequency has its toll. As the output power is reduced, the time interval in which the converter works with hard switching grows from the zero crossing region towards the peak, reducing the efficiency.

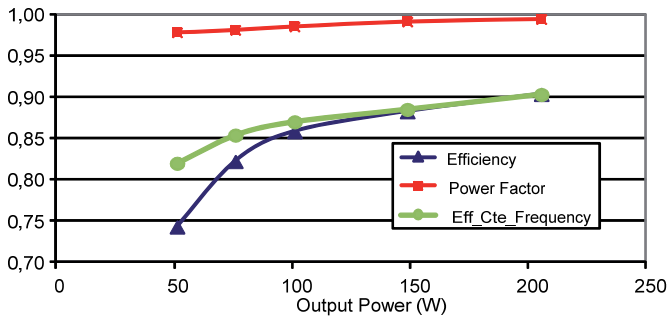

Fig. 8. Power factor and efficiency vs. output power.

VII. CONCLUSION

A single-stage SMPS with PFC, suitable for low-power applications (under 600 W) has been presented. Experimental results for a 200 W–110 kHz prototype presented PF close to unity, high efficiency, and a small number of components, when compared with the two-stage approach. The obtained efficiency trend curve has shown that the presented converter is more suitable for applications with load variations from 50 to 100 % of the rated power when powered by a 220-V utility line. Therefore, it is probably more useful for equipment with a dedicated load. Wide load range applications are possible, but the efficiency is reduced at light load conditions and extra care is necessary to properly design the converter to avoid DC-link voltage stress, optimizing the ZVS range.

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REFERENCES

[1] L. Brush, *Power Factor Correction Market Driven by Regulations*, Bodo's Power, 2006.

[2] Darnell Group Inc., "*AC-DC Power Supplies: Economic Factors, Application Drivers, Architecture/Packaging Trends, Regulatory and Technology Developments*", Ninth Edition, January 2009

[3] B.Sharifipour, J. S. Huang, P.Liao, L. Huber, M.M. Jovanovic, "Manufacturing and Cost Analysis of Power-Factor-Correction Circuits", *IEEE Applied Power Electronics Conference and Exposition, APEC '98*, pp. 490-494, 1998.

[4] Z. Jindong, M.M. Jovanovic and F.C. Lee, "Comparison between CCM single-stage and two-stage boost PFC converters". *Proc. of IEEE APEC 1999*, pp. 335-341, 1999.

[5] J.-Y. Lee, G.-W. Moon, M.-J. Youn, "Design of a Power-Factor-Correction Converter Based on Half-Bridge Topology," *IEEE Transactions on Industrial Electronics*, Vol. 46, no. 4, August 1999.

[6] J.Qian, F.C. Lee, "Charge Pump Power-Factor-Correction Technologies Part I: Concept and Principle", *IEEE Transactions on Power Electronics*, Vol. 15, no 1, pp.121-129, January 2000.

[7] J.Qian, F.C. Lee, "Charge Pump Power-Factor-Correction Technologies Part II: Ballast Applications", *IEEE Transactions on Power Electronics*, Vol. 15, no 1, pp.130-139, January 2000.

[8] D. L. O'Sullivan, M. G. Egan, M. J. Willers, "A Family of Single-Stage Resonant AC/DC Converters With PFC", *IEEE Transactions on Power Electronics*, Vol. 24, no 2, pp.398-408, February 2009.

[9] P. Das, S. Li, G. Moschopoulos, "An Improved AC–DC Single-Stage Full-Bridge Converter With Reduced DC Bus Voltage", *IEEE Transactions on Industrial Electronics*, Vol. 24, no 12, pp. 4882-4893, December 2009.

[10] C. B. Nascimento, A. J. Perin, "High Power Factor Electronic Ballast for Fluorescent Lamps with Reduced

Input Filter and Low Cost Implementation". *IEEE Transactions on Industrial Electronics*, Vol. 55, pp. 711-721, 2008.
[11] C.B. Nascimento, E.I. Pereira, A.J. Perin, "Low Cost High Power Factor Electronic Ballast with No Input Filter", *IEEE 36th Power Electronics Specialists Conference, 2005. PESC '05*, pp.1100-1106, 2005.
[12] C. S. Postiglione, A. J. Perin, C. B. Nascimento, "Single-Stage Power Factor Correction Switched Power Supply", *IEEE IECON'06 32nd Annual Conference of the IEEE Industrial Electronics Society*, pp. 2402-2407, November 2006.
[13] A. Nabae, H. Nakano, S. Arai, "Novel Sinusoidal Converters With High Power Factor", *IEEE Industrial Applications Society Annual Meeting, IAS 1994*, vol. 2, pp. 775-780, 1994.
[14] R. Teodorescu, S. B. Kjær, S. M. Nielsen, F. Blaabjerg, J.K. Pedersen, "Comparative Analysis of Three Interleaved Boost Power Factor Corrected Topologies in DCM", *IEEE Power Electronics Specialists Conference, PESC 2001*, vol. 1, pp. 3-7, June 2001.
[15] F. Tao, F. C. Lee, "An Interleaved Single-Stage Power-Factor-Correction Electronic Ballast", *IEEE Applied Power Electronics Conference and Exposition, APEC 2000*, vol.1, pp. 617-623, 2000.
[16] H.-L. Do, B.-H. Kwon, "Single-Stage Line-Coupled Half-Bridge Ballast with Unity Power Factor and Ripple-Free Input Current Using a Coupled Inductor", *IEEE Transactions on Industrial Electronics*, Vol. 50, no. 6, pp 1259-1266, 2003.
[17] J.-M Kwon, W.-Y. Choi, H.-L. Do and B.-H. Kwon, "Single-stage half-bridge converter using a coupled-inductor", *IEE Proc. Electr. Power Appl.*, Vol 152, no. 3, pp. 748-756, May 2005.
[18] T.-F. Wu, J.-C. Hung, S.-Y. Tseng, Y.-M. Chen, "A Single-Stage Fast Regulator with PFC Based on an Asymmetrical Half-Bridge Topology", *IEEE Transactions on Industrial Electronics*, vol. 52, No.1, February 2005.
[19] G. Moschopoulos, P. Jain, "Single-Phase Single-Stage Power-Factor-Corrected Converter Topology", *IEEE Transactions on Industrial Electronics*, Vol. 52, no 1, pp. 23-35, February 2005.
[20] C. S. Postiglione, A. J. Perin, C. B. Nascimento, "A Single-Stage Power Factor Correction Switched Mode Power Supply", *12th European Conference on Power Electronics and Applications, EPE 2007*, pp. 1-9. September 2007.
[21] R. W. Erickson, "*Fundamentals of Power Electronics*", ISBN 0-412-08541-0 Chapman and Hall, 1997.
[22] I. Barbi, F. P. Souza.: *High Frequency soft-switched Isolated dc/dc Converters* (in portuguese), Authors Ed. INEP – UFSC, 1999.
[23] IEC 61000-3-2, "*Limits for Harmonic Current Emission (equipment input current ≤ 16 A per phase)*", International Electrotechnical Commission, Switzerland, 2000.

BIOGRAPHIES

Cícero da S. Postiglione was born in Porto Alegre, Brazil, in November 1979. He received the B.S, M.S. and the Ph.D degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 2004, 2006 and 2011, respectively, where he is currently working as a Consultant Eng. at Huaweii Technologies Sweden AB. and has been engaged in the advanced development of switching power converters.

André L. Fuerback was born in Florianópolis, SC, Brazil, in 1977. He received the B.S und M.S. and the Ph.D degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 2004 and 2006, respectively, where he is currently working as R&D Engineer in the Power Electronics Institute.

Claudinor B. Nascimento was born in Tubarão, SC, Brazil, in 1971. He received the B.S, M.S., and Ph.D. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1994, 1996 and 2005, respectively. He was with the Electronic Coordination, Federal Technological University of Paraná, Ponta Grossa, Brazil, in 1997, where he is currently a Professor of power electronics and automation and control. His research interests include electronic ballasts for discharge lamps, power-factor-correction circuits, and new converter topologies.

Denizar C. Martins was born in São Paulo, Brazil, on April 24, 1955. He received the B.S. and M.S. degrees in electrical engineering from Federal University of Santa Catarina (UFSC), Florianópolis, SC, Brazil, in 1978 and 1981, respectively, and the Ph.D. degree in electrical engineering from the Polytechnic National Institute of Toulouse, Toulouse, France, in 1986. He is currently a Titular Professor in the Department of Electrical Engineering at Federal University of Santa Catarina. He is a member of the Brazilian Power Electronics Society. His interest research areas include dc-dc and dc-ac converters, high frequency, soft commutation, power factor correction and grid-connected PV systems.

Arnaldo J. Perin received the B.E. degree in electronic engineering from Pontificia Universidade Católica do Rio Grande do Sul, Porto Alegre, Brazil in 1977, the M.S. degrees in electrical engineering from Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 1980 and Dr.Ing degree from Institut National Polytechnique de Toulouse, Toulouse, France, in 1984.

He was with the Electrical Engineering Department (EEL), UFSC, in 1980, where was engaged in education and research on power electronics until 2009. After that, he assumed a volunteer professorship with the EEL Graduation Program at the UFSC. Research interests include power electronics, modulation, ac converters, and power factor.