SINGLE-PHASE ACTIVE POWER FILTERS WITH REDUCED NUMBER OF POWER SWITCHES AND OPTIMUM VOLTAGE CONTROL ANGLE

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***Abstract* - This paper proposes some topologies of universal active power filter for single-phase applications with reduced number of components. Some configurations are proposed: two with both series and parallel converters connected in half-bridge, sharing the same d.c.-bus mid-point connection; and the others with the series and parallel converters sharing one leg. It will be demonstrated the existence of a coupling law between the two converters (S_e and S_h) related to the voltage capabilities. All configurations compensate for current and voltage harmonic and provide power factor control close to one. Comparisons between the structures are made and the steady-state analysis are also presented to demonstrate that it is possible to obtain an optimum voltage angle in order to reduce the amplitudes of the converters' currents and, consequently, the total losses of the systems. Simulated and experimental results validate the theoretical considerations.**

***Keywords* – Active Power Filter, Optimum Voltage Angle, Reduced Number of Components, Two-leg Converter.**

I. INTRODUCTION

The continuous proliferation of electronic equipment either for home appliances or industrials uses have the drawback of increasing the non-sinusoidal current into power network. Different mitigation solutions are currently proposed and used in practical applications to work out the problems of harmonics in electric grids. In the last decades, the use of active filtering techniques has became more attractive due to the technological progress in power electronic switching devices, enhanced numerical methods and more efficient control algorithms.

The Series Active Power Filter (SAPF) [1], [2], [3] provides load voltage control, eliminating voltage disturbances, such as unbalance, sags, notches, flickers and voltage harmonics, so that a regulated fundamental load voltage with constant magnitude is provided to the load. The purpose of a Parallel Active Power Filter (PAPF) also knowing as shunt, [4], [5], [6], [7], [8] is to absorb harmonics current, compensate for reactive power and regulate the d.c.-bus voltage. The Universal Active Power Filter (UAPF) [9], [10], [11], [12] [13], [14], which is combination of both ones, is a versatile device that operates as series and parallel active power filter. Then, it can simultaneously fulfill different objectives like maintaining a balanced sinusoidal (harmonic free) nominal voltage at the load bus, source current harmonics elimination, load balance and power factor correction.

UAPF is appeared to be a strong tool to improve power quality in many applications and it has been attracting the attention of many researchers in order to reduce cost, size and weight. Generally, the largest cost reduction is achieved by reducing the number of switches employed in a converter power circuit or developing topologies that employ switches with lower voltage stresses [15], [16], [17], [18], [19]. In this field, the challenge is to choice between full-bridge and half-bridge topologies. The main attributes for the sake of comparison are: the number of bi-directional switches (two for the half-bridge and four for the full-bridge); the voltages of the switches (rated line voltage for the full-bridge and half of the rated line voltage for the half-bridge) and capacitor current in the case of the half-bridge.

A conventional UAPF topology, Figure 1, consists of two full-bridge bi-directional converters connected to a common d.c.-bus. The series bi-directional converter consists of four

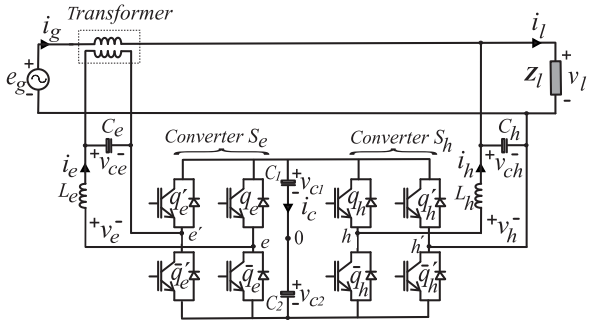

Fig. 1. Conventional topology of single-phase Universal Active Power Filter (UAPF).

switches connected via transformer in series with the a.c line. The parallel bi-directional converter also consists of four switches. As the number of electronic power switches is reduced to achieve low cost and high performance at the same time the d.c.-bus voltage must increase. For the controllability of the conventional UAPF system, the voltage of the d.c-bus must be $\frac{3}{2}$ times of the peak voltage of the a.c. line. In configurations with two-leg converters, the voltage of both capacitors C_1 and C_2 must be $\frac{3}{2}$ times of the peak voltage of the line voltage. Therefore, the voltage of the capacitor bank must be three times of the a.c. line peak voltage [11], [18].

This paper proposes some configurations of UAPF with reduced number of components for single-phase applications. Configurations have only two-leg and use a capacitor bank with d.c.-bus mid-point connection. In Figure 2 are presented

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some conventional structures of UAPF with transformer connected in series side. The configurations presented in Figure 3 are directly connected to the distribution system without a series injection transformer, the transformer is used in parallel to the load [20]. This configurations may be feasible when the transformer turns ratio *n*, of the transformer winding connected to the parallel converter, is varied in order to reduce the d.c.-bus voltage. The operation principle, control strategy, steady-state analysis and experimental results are presented to validate the theoretical considerations.

II. FREQUENCY MODULATION

Configurations presented in Figure 2 have a transformer in the series side connection and the presented in Figure 3 are connected to the distribution system without series injection transformer, which may struggles with core saturation and voltage drop [21]. However, the magnetic flux in iron core of series transformer may change in a large range depending on the close angle of injecting voltage, at the same time iron core easily get over saturated. Over saturation in transformer iron core leads to produce large field inrush current and distortion on compensating voltage waveform [22]. These configurations use the transformer in parallel to the load.

The active power filters configurations for single-phase applications can be composed by two-leg converters [23]. They can be classified into $2L$, $2L_e$ and $2L_h$. The converters, Figure 2 and 3, can operate both sides in half-bridge (denoted as $2L$ configurations) or one side in full-bridge and the other one in half-bridge with a shared-leg (denoted as $2L_e$ and $2L_h$ configurations). In $2L_e$ the shared-leg is h and for $2L_h$ is the leg e.

The configurations $2L_e$ and $2L_h$ can operate in half-bridge and full-bridge, but there is a coupling law between the two converters. Half-bridge converters voltages are limited by $v_e < \left(\frac{E}{2}\right)$ (topologies $2L_h$) and $v_h < \left(\frac{E}{2}\right)$ (topologies $2L_e$). Full-bridge converters voltages are limited by $v_h < E$ (topologies $2L_h$) and $v_e < E$ (topologies $2L_e$). Both converters in half-bridge (topologies $2L$) are connected to a common d.c.-bus mid-point connection and have the converters voltages limited by $v_e = \left(\frac{E}{2}\right)$ and $v_h = \left(\frac{E}{2}\right)$, being $E = v_c = v_{c1} + v_{c2}$.

The conduction state of the switch-pairs is represented by homonymous binary variables q_e, $\bar{q}_e$, q_h and $\bar{q}_h$, where $q = 1$ indicates a closed switch while $q = 0$ indicates an open one. The pair of switches q_e or $\bar{q}_e$ and q_h or $\bar{q}_h$ are complementary, so

$$q_e = 1 - \bar{q}_e \quad (1)$$

$$q_h = 1 - \bar{q}_h \quad (2)$$

The pulse-widths of the gating signals are determined from the reference pole voltages v^*_{e0} and v^*_{h0}, as noted in

$$\tau_e = \frac{T}{2} + \frac{T}{E} v^*_{e0} \quad (3)$$

$$\tau_h = \frac{T}{2} + \frac{T}{E} v^*_{h0} \quad (4)$$

where T is the sample period for the pulse-width modulation (PWM). The reference signals for the pole voltages v^*_{e0} and

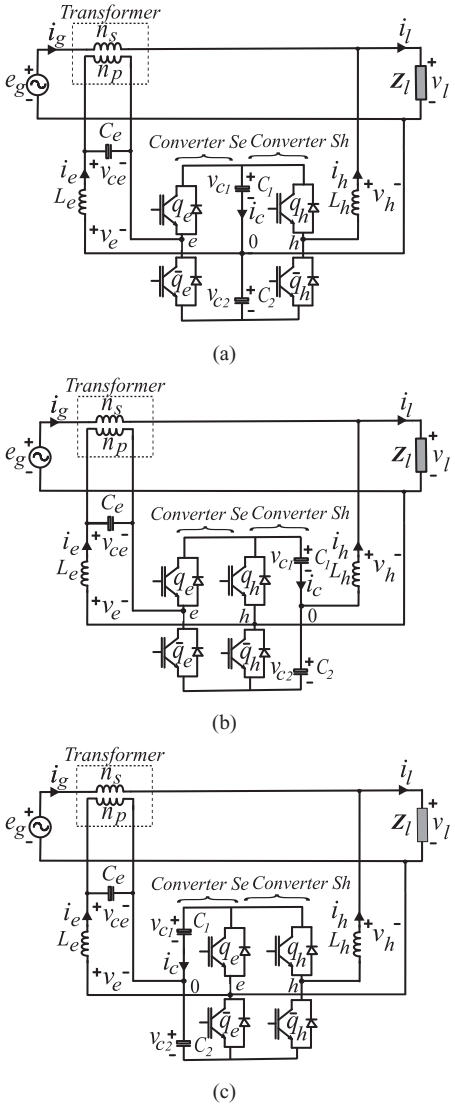


Fig. 2. Single-phase UAPF with transformer in series connection - configurations: (a) $2L$ (b) $2L_e$ and (c) $2L_h$.

v^*_{h0} are determined from the reference voltages v^*_e and v^*_h. The reference signals to the pole voltages of the UAPF converters are presented in the next subsections.

A. Configuration $2L$

Configurations $2L$ have both the converters in half-bridge topologies. Voltages v_e and v_h are in function of the converter pole voltages v_{e0} and v_{h0} which depend on the conduction states of the power switches and individual voltage of the capacitors v_{c1} and v_{c2}, then:

$$v_e = v_{e0} = q_e v_{c1} - (1 - q_e) v_{c2} \quad (5)$$

$$v_h = v_{h0} = q_h v_{c1} - (1 - q_h) v_{c2} \quad (6)$$

where v_{c1} and v_{c2} denote the capacitors voltages. The reference pole voltages can be expressed by:

$$v^*_{e0} = v^*_e \quad (7)$$

$$v^*_{h0} = v^*_h \quad (8)$$

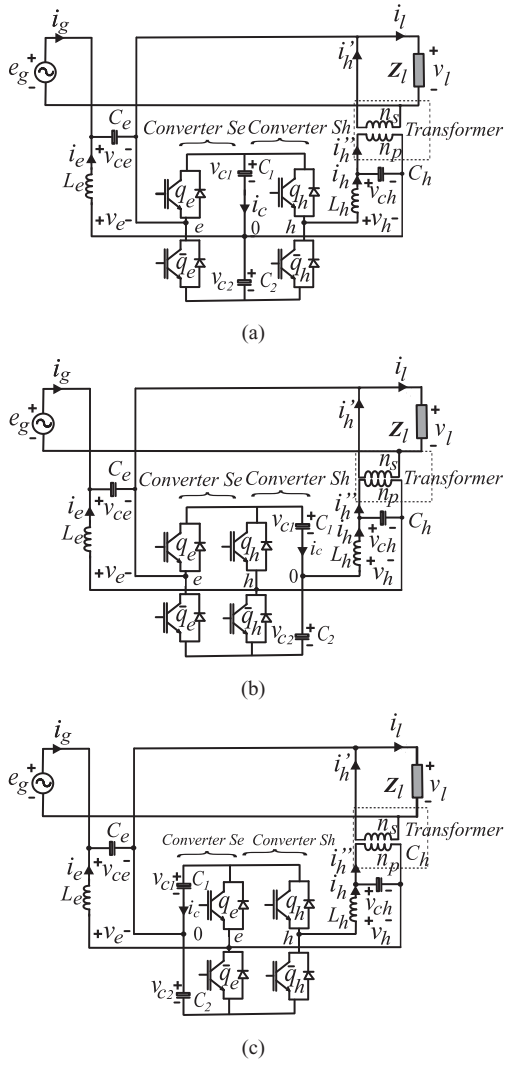


Fig. 3. Single-phase UAPF with transformer in parallel side - configurations: (a) $2L$ (b) $2L_e$ and (c) $2L_h$.

B. Configuration $2L_e$

Configurations $2L_e$ have the converter S_e in full-bridge and S_h in half-bride. Voltages v_e and v_h can be expressed as a function of the converter pole voltages v_{e0} and v_{h0} that depend on the conduction states of the power devices, so:

$$v_e = v_{e0} - v_{h0} = (q_e - q_h)E \tag{9}$$

$$v_h = v_{h0} = q_h v_{c1} - (1 - q_h)v_{c2} \tag{10}$$

It can be noted that the voltage v_e does not depend on the individual capacitors voltages v_{c1} and v_{c2}.

Considering that v_e^* and v_h^* denote the desired reference voltages, then the reference pole voltages can be expressed by:

$$v_{e0}^* = v_e^* + v_h^* \tag{11}$$

$$v_{h0}^* = v_h^* \tag{12}$$

Defining the reference pole voltages, pulse-widths τ_e and τ_h can be generated from (3) and (4).

C. Configuration $2L_h$

Configurations $2L_h$ have the converter S_h in full-bridge and S_e in half-bride. Voltages v_e and v_h can also be expressed as a function of the converter pole voltages v_{e0} and v_{h0}, so:

$$v_e = v_{e0} = q_e v_{c1} - (1 - q_e)v_{c2} \tag{13}$$

$$v_h = v_{h0} - v_{e0} = (q_h - q_e)E \tag{14}$$

In this case, the voltage v_e does not depend on the individual capacitor voltages v_{c1} and v_{c2}. The reference pole voltages can be expressed as:

$$v_{e0}^* = v_e^* \tag{15}$$

$$v_{h0}^* = v_h^* + v_e^* \tag{16}$$

Then, the pulse-widths can be calculated by using (3) and (4).

III. SHARED-LEG AND CAPACITOR CURRENTS

The currents flowing through the shared-leg, for configurations $2L_e$ and $2L_h$, and capacitor current for $2L$ depend on the currents i_e and i_h. The description of shared-leg and capacitor current are presented in the next subsections.

A. Configuration $2L$

Neglecting the frequency 2ω due to the single-phase power flow [24]. The capacitors average currents for configurations $2L$ are given by:

$$\bar{\imath}_{c1} = \frac{\bar{\imath}_e - \bar{\imath}_h}{2} \tag{17}$$

$$\bar{\imath}_{c2} = \frac{\bar{\imath}_h - \bar{\imath}_e}{2} \tag{18}$$

B. Configuration $2L_e$

In these configurations the shared-leg is h between converters S_e and S_h. Currents flow through the top and down switches q_h and $\bar{q_h}$ are:

- for $q_h = 1$ (during τ_h):

$$i_{qh} = (i_e + i_h) \tag{19}$$

$$\imath_{\bar{q}h} = 0 \tag{20}$$

- for $q_h = 0$ (during T - τ_h):

$$i_{qh} = 0 \tag{21}$$

$$\imath_{\bar{q}h} = -(i_e + i_h) \tag{22}$$

The equations can be rewritten as follows:

$$i_{qh} = q_h(i_e - i_h) \tag{23}$$

$$\imath_{\bar{q}h} = -(1 - q_h)(i_e - i_h) \tag{24}$$

It is possible to determine the average value of the current i_{qh} and $i_{\bar{q}h}$ within the period T:

$$\bar{\imath}_{qh} = \frac{1}{T}\int_{\tau} i_{qh}dt \tag{25}$$

$$\bar{\imath}_{\bar{q}h} = \frac{1}{T}\int_{\tau} i_{\bar{q}h}dt \tag{26}$$

Neglecting the high-frequency current components due to the switching and assuming that the interval T is too small, the average current flowing through each switch q_h and $\bar{q_h}$ of the shared-leg are given by:

$$\bar{i}_{qh} = \frac{\tau}{T}(\bar{i}_e - \bar{i}_h) \quad (27)$$

$$\bar{i}_{\bar{q}h} = \frac{T-\tau}{T}(\bar{i}_e - \bar{i}_h) \quad (28)$$

Substituting (4) in (27) and (28), the average current flowing through each switches of the shared-leg are given by:

$$\bar{i}_{qh} = \left(\frac{v^*_{h0}}{E} + \frac{1}{2}\right)(\bar{i}_e - \bar{i}_h) \quad (29)$$

$$\bar{i}_{\bar{q}h} = \left(\frac{v^*_{h0}}{E} - \frac{1}{2}\right)(\bar{i}_e - \bar{i}_h) \quad (30)$$

Capacitors currents of the dc-link for configurations $2L_e$ are:

$$i_{c1} = q_e i_e - q_h(i_e - i_h) \quad (31)$$

$$i_{c2} = i_{c1} - i_h \quad (32)$$

and average currents are given by:

$$\bar{i}_{c1} = \frac{1}{2}\bar{i}_h \quad (33)$$

$$\bar{i}_{c2} = -\frac{1}{2}\bar{i}_h \quad (34)$$

Ignoring the frequency due to the single-phase power flow.

C. *Configuration* $2L_h$

The procedure to determine the average currents for these configurations is similar to that presented in section III.B. Then, the average current flowing through each switch of the shared-leg q_e and $\bar{q_e}$ are given by:

$$\bar{i}_{qe} = -\left(\frac{v^*_{e0}}{E} + \frac{1}{2}\right)(\bar{i}_e - \bar{i}_h) \quad (35)$$

$$\bar{i}_{\bar{q}e} = -\left(\frac{v^*_{e0}}{E} - \frac{1}{2}\right)(\bar{i}_e - \bar{i}_h) \quad (36)$$

It is also observed that the current in the shared-leg is defined by the sum of currents i_e and i_h.

Capacitor currents of the d.c.-link for these configurations are given by:

$$i_{c1} = -q_h i_h + q_e(i_h - i_e) \quad (37)$$

$$i_{c2} = i_{c1} + i_e \quad (38)$$

and average currents are:

$$\bar{i}_{c1} = -\frac{1}{2}\bar{i}_e \quad (39)$$

$$\bar{i}_{c2} = \frac{1}{2}\bar{i}_e \quad (40)$$

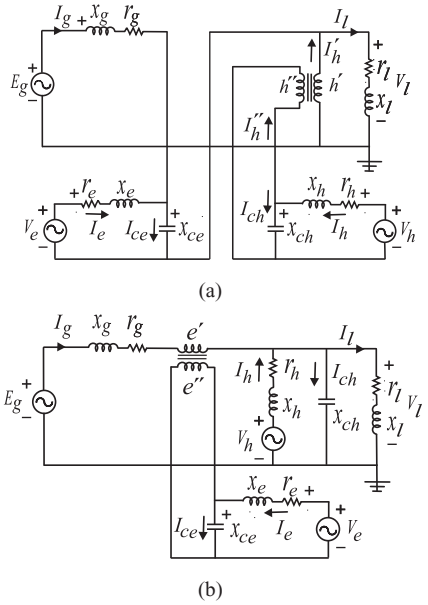


Fig. 4. Steady-state circuits: (a) transformer in parallel side and (b) transformer in series connection.

IV. STEADY-STATE CHARACTERISTICS

Steady-state analysis of the presented configurations with the transformer connected in parallel or in series side are based on the model shown, respectively, in Figure 4(a) and 4(b). The figures compromise the grid (E_g and I_g), internal grid impedance (r_g and x_g), series voltage (V_e), series impedance (r_e, x_e and x_{ce}), series current (I_e), parallel voltage (V_h), parallel impedance (r_h, x_h and x_{ch}), parallel current (I_h), series and parallel transformers, and load impedance (r_l, x_l).

Voltage sources V_e and V_h represent the converters generated voltages of converters S_e and S_h, respectively. The power load S_l presents a inductive power factor (PF) equal to 0.85. All results presented in this section are in function of load angle δ_l. This angle is the phase angle between the grid voltage e_g and load voltage v_l. Otherwise, the values of the parameters are represented in p.u. system.

In Figs. 5 and 6 are shown the results for the proposed UAPF with transformer connected in the parallel side using the following parameters: $|e_g| = 1.0$, $|v_l| = 1.0$, $r_g = 0.001$, $r_e = 0.005$, $r_h = 0.005$, $r'_h = 0.003$, $r''_h = 0.003$, $x_g = 0.01$, $x_e = 0.33$, $x'_h = 0.33$, $x''_h = 0.33$, $x_m = 0.9$, $x_h = 0.33$, $x_{ce} = 1.0$, $x_{ch} = 0.5$. The converter voltage amplitudes V_e and V_h are observed in Figure 5(a).

In this figure, the voltage amplitude of series converter V_e assume the lowest value at $\delta_l \approx -3.5°$. As δ_l moves away from $\delta_l \approx -3.5°$ the voltage V_e increases considerably. It is noted in Figure 5(b) that the converters' currents amplitude I_e and I_h assume the lowest values, respectively, at $\delta_l \approx -40°$ and $\delta_l \approx 36°$, while the amplitude of I_g remains practically constant on the δ_l variation. The current I'_h has the smallest amplitude value at $\delta_l \approx 32°$.

From Figure 6, it can be seen that the system has better performance for a load angle close to $\delta_l \approx -30°$. This operating point corresponds to the range in which the

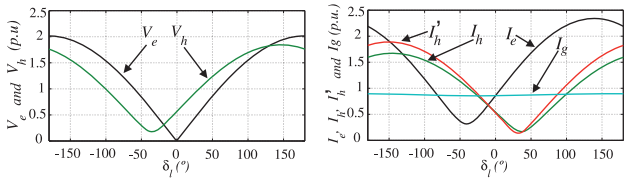


Fig. 5. Steady-state analysis of single-phase UAPF with transformer in parallel side: (a) converter voltages and (b) converters, transformer and grid currents.

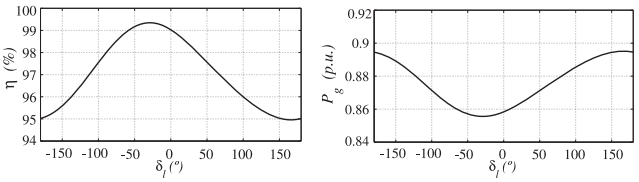


Fig. 6. Steady-state analysis of single-phase UAPF with transformer in parallel side: (a) efficiency and (b) a.c. power grid.

amplitudes of the converters' current I_e and I_h are smaller. In Figure 6(b) is observed that the point of maximum performance occurs when the power source has the lower amplitude.

In Figs. 7 and 8 are presented the results for the proposed UAPF with transformer connected in the series side, the results were obtained using the following parameters: $|e_g| = 1.0$, $|v_l| = 1.0$, $r_g = 0.001$, $r_e = 0.005$, $r_h = 0.005$, $r'_h = 0.003$, $r''_h = 0.003$, $x_g = 0.01$, $x_e = 0.33$, $x'_h = 0.33$, $x''_h = 0.33$, $x_m = 0.9$, $x_h = 0.33$, $x_{ce} = 1.0$, $x_{ch} = 1.0$.

Similar results are presented for the configuration with transformer in series side. The explanations of the presented simulated results are similar to the previous case. The steady-state analysis are shown in Figs. 7 and 8. Comparing the

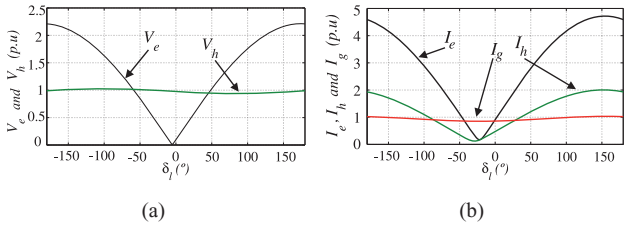


Fig. 7. Steady-state analysis of the proposed single-phase UAPF with transformer in series connection: (a) converter voltages and (b) converters, transformer and grid currents.

steady-state circuits analysis, it is clearly observed that the configuration with transformer in parallel side also presents the possibility to reduce the d.c.-bus voltage by varying the load angle instead of changing the transformer turns ratio $n = \left(\frac{n_p}{n_s}\right)$, as the voltage of the parallel converter V_h is reduced the capacitor d.c.-bus voltage can also be, see Figure 5(a). There are two options for reducing the d.c.-bus voltage: (1) varying the load angle and (2) changing the transformer turns ratio.

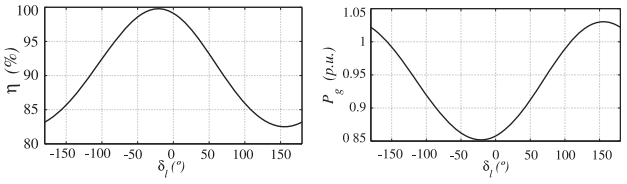


Fig. 8. Steady-state analysis of single-phase UAPF with transformer in series connection: (a) efficiency and (b) a.c. power grid.

From Figure 6(a) it is noted that the parallel converter voltage V_h remains practically constant with changes in the load angle δ_l. For both structures, as the currents of the converters are reduced the voltage amplitude of the series converter is increased. To obtain the point of minimum losses is necessary to have available d.c.-bus voltage at the capacitors. The voltage of the series converter (V_e) drastically increase as the load angle is varied, Figs. 5(a) and 7(a), then, the d.c.-bus capacitors needs to supply more energy for the series converter in order to provide the correct voltage compensation.

V. CONTROL STRATEGY

The block diagram of the proposed configurations can be seen in Figure 9. The d.c.-bus voltage is compared with the

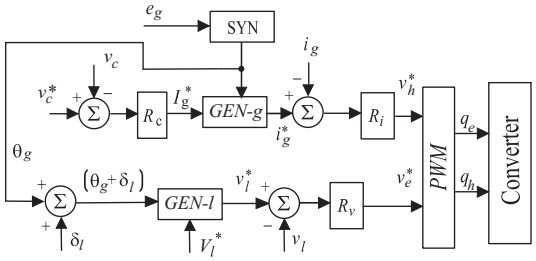


Fig. 9. Control block diagram for the proposed Universal Active Power Filter (UAPF).

reference voltage v_c^* and the error is applied to the input of a PI controller R_c.

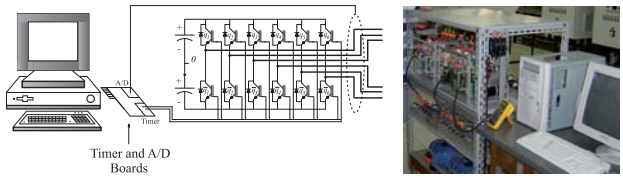
The output of R_c controller defines the current amplitude of reference signal I_g^* that is synchronized with the grid voltage e_g in order to control the power factor, this is done via block $GEN\text{-}g$. This block defines the current i_g^*. This synchronism is accomplished by PLL (Phase Locked Loop) to produce the reference voltage. The input of the PLL is the grid voltage. The output of the PLL is a $60Hz$ reference voltage, which is exactly in phase with the grid voltage. The current error $(i_g^* - i_g)$ is applied to current controller represented by R_i. The controller R_i is a double sequence digital current controller [25]. The output voltage v_h, of this controller, is used to determine the switches conduction state.

The voltage regulation applied to the load is determined from the instantaneous reference load voltage v_l^* which is obtained by the voltage amplitude V_l^* and by the angles θ_g and δ_l via block $GEN\text{-}l$. θ_g is the instantaneous angle of e_g and δ_l is used to determine the best operating point of the system. This information is applied to the block R_v which is also a

modified PI controller similar to presented R_i controller. The output of this controller generates the reference voltage for determining the PWM.

VI. EXPERIMENTAL RESULTS

Some topologies of UAPF, based on two bi-directional converters composed by two-leg connected to a common d.c.-link, have been proposed. The topology presented in Figure 3(c) was chosen to compose the experimental result because d.c.-bus voltage can be drastically reduced from the regulation of the transformer turn ratio n and/or the optimized load angle δ_l. The proposed single-phase UAPF system presented in Figure 3(c) has been tested by using a microcomputer-based system which is equipped with dedicated boards, in order to generate the control signals. The system have twelve sensors (six current and six voltage sensors), interface card and data acquisition boards, and two static converters each one with three-leg, see Figure 10. In experimental tests, d.c. capacitors



(a) (b)

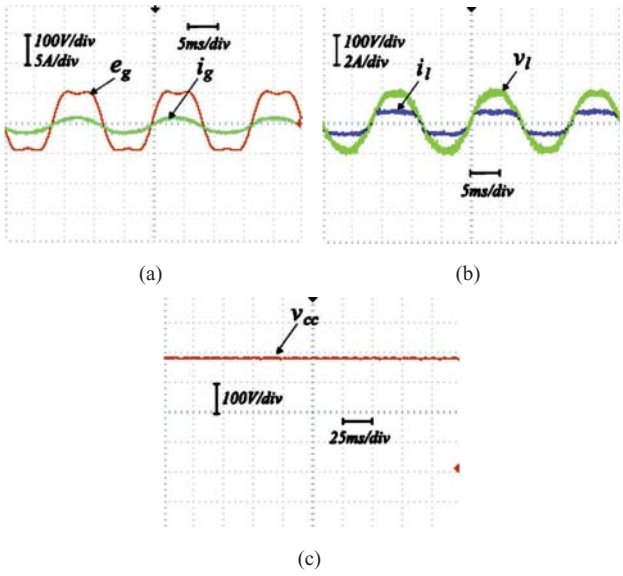
Fig. 10. Experimental platform in laboratory:(a) Schematic diagram of the converter via PC-based control, (b) Picture of the topology.

were selected as $C = 2200u$F, and the switching frequency was set at 10 kHz. The system parameters are given by

- Source frequency: 60 Hz;
- Harmonic frequency: 180 Hz;
- d.c.-bus voltage: 380 V_{cc} [see Figure 11(c)] and 80 V_{cc} [see Figure 13(c)];
- Inductors filters: 5 mH;
- Capacitor filter: 70 μF;
- Nonlinear load composed by diode bridge rectifier with $R = 10\ \Omega$ and $L = 62$ mH;
- Transformer turn ratio: $n = 1$ and $\delta_l = 0$ for Figure 11 and $n = 2$ and $\delta_l \approx -30°$ for Figure 13.

The parallel converter requires more energy for compensating harmonics current, provide power factor control close to unit and regulate the d.c.-bus voltage between both converters at desired level; the configurations $2L_e$, due to the shared-leg, need more d.c.-bus voltage compared to the others. According to the steady-state analysis, section IV, all configurations with transformer in parallel side allow to reduce the d.c.-bus voltage varying the load angle and/or the transformer turns ratio. The configurations $2L_h$ with transformer in parallel side was chosen because it requires less d.c.-bus voltage compared to the transformer in series side, and also by the capacitor current for $2L$ be greater compared to $2L_e$ or $2L_h$.

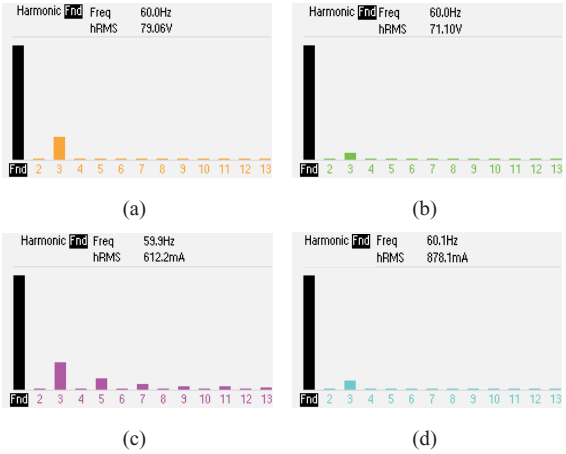
In the test, the load is supplied by a voltage source generator with 20% the $3rd$ harmonic. In Figure 11(a), it is noted that the grid current is compensated with the power factor control



(a) (b)

(c)

Fig. 11. Experimental results for proposed UAPF (Configuration $2L_h$) with load angle $\delta_l = 0°$ and $n = 1$: (a) grid voltage and current - e_g, i_g, (b) load voltage and current - v_l, i_l, (c) d.c-bus voltage - v_{cc}.



(a) (b)

(c) (d)

Fig. 12. Spectral analysis UAPF for proposed UAPF (Configuration $2L_h$): (a) grid voltage e_g, (b)load voltage v_l, (c) load current i_l, (d) grid current i_g.

closed to one and THD (Total Harmonic Distortion) of the current equal to 4.69%. The load presents nonlinear current characteristics with current THD equal to 29.74% and the load voltage is compensated with THD equal to 3.37%, Figure 11(b). The d.c.-bus voltage is observed in Figure 11(c). The spectral analysis of voltages and currents in the grid and load are also presented in Figure 12.

The set of experimental results presented in Figs. 13 and 14 were obtained considering the transformer turn ratio $n = 2$ and load angle $\delta_l \approx -30°$. The great contribution is related to the drastically reduction of the capacitor voltage in order to obtain the desirable results. The load voltage and grid current are also compensated, with power factor control close to one. The grid current THD is 4.36%, while the load current presents THD equal to 28.74%. The load voltage presents

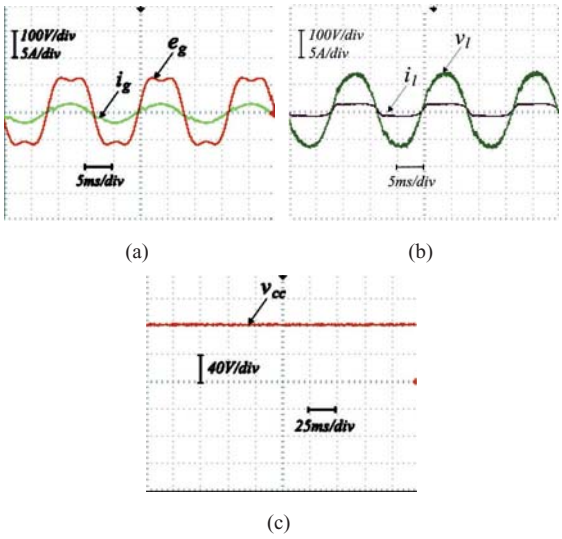


Fig. 13. Experimental results for proposed UAPF (Configuration $2L_h$) with load angle $\delta_l \approx -30^\circ$ and $n = 2$: (a) grid voltage and current - e_g, i_g, (b) load voltage and current - v_l, i_l, (c) d.c-bus voltage - v_{cc}.

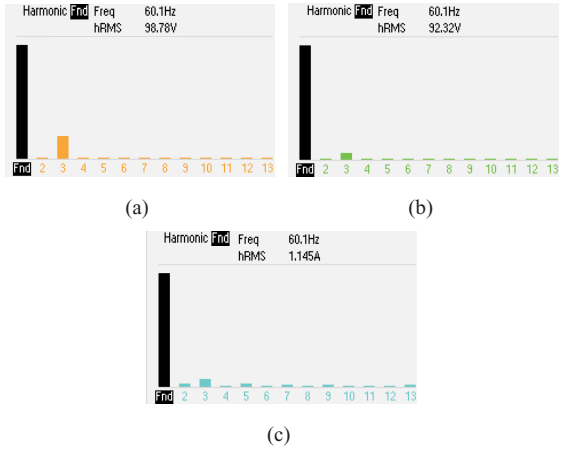


Fig. 14. Spectral analysis for proposed UAPF (Configuration $2L_h$): (a) grid voltage e_g, (b)load voltage v_l, (c) grid current i_l.

THD, for this case, equal to 2.98%.

It can be noted that despite of the distortion on the grid voltages, the load voltages present very low harmonic level, indicating that the filter operates properly.

VII. CONCLUSION

Some topologies of single-phase active power filter with isolation transformer in the series or parallel side for voltage and current harmonic compensation and power factor control have been presented in this paper. Such analysis showed that it is possible to operate with a load active voltage amplitude regulated at the rated reference value for some grid voltages and load conditions. The grid current compensation is also achieved with power factor control close to one. It was also observed that the capacitors average current for configurations denoted as $2L$ is higher than $2L_e$ or $2L_h$, but the total losses for $2L_e$ or $2L_h$ are greater than $2L$ - due to shared-leg current. Comparisons of steady-state analysis were presented and it was noted that the currents of the converters can be reduced from the load angle δ_l. Besides, the structures with the transformer in parallel to the load present the option to reduce the capacitors size and d.c.-bus voltages by varying the transformer turn ratio n and/or load angle δ_l.

The operation principle, control strategy, steady-state analysis, simulated and experimental results of the proposed single-phase active power filters with reduced number of power switches were presented under different conditions and demonstrated adequate harmonic correction and power factor close to one.

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