A FLICKER-FREE POWER LEDS DRIVER BASED ON THE NON-ISOLATED SEPIC RECTIFIER USING A REGENERATIVE SNUBBER

Ismael Burgardt, Eloi Agostini Jr., Carlos H. Illa Font, Claudinor B. Nascimento
Department of Electronic Engineering, Federal Technological University of Paraná
Ponta Grossa - PR
e-mails: eloiagostini@utfpr.edu.br, illafont@utfpr.edu.br, claudinor@utfpr.edu.br

***Abstract* – This paper presents an AC electronic lighting system using a non-isolated SEPIC PFC rectifier to drive and control power LEDs currents. One energy regenerative snubber for reducing the converter switching losses and improve the system efficiency is proposed. To reduce ripple current in the LEDs array a linear current regulator is placed in the SEPIC's output terminals. In order to reduce the efficiency impairment, the conditions for achieving minimum energy loss in the current regulator are also detailed. The operation stages as well as the theoretical waveforms and main equations at steady state of the proposed SEPIC rectifier using a regenerative snubber are detailed. To verify the theoretical analysis carried out, experimental results of a prototype operating in 127 and 220 V for 35 LEDs / 42 W are also presented. In this paper, the point of minimum energy loss in the linear regulator is adjusted in open loop to validate the converter operation.**

***Keywords* - Electronic Lighting System, Energy Regenerative Snubber, Linear Current Regulator, Non-isolated SEPIC, Power LEDs.**

I. INTRODUCTION

Solid-State Lighting (SSL) has revolutionized the lighting market. LEDs (Light Emitting Diodes) are versatile and incredibly energy-efficient, and as their color stability and lumen efficacy continue to increase, they are gradually replacing the conventional bulbs into an ever expanding range of general illumination applications.

An AC electronic lighting system for power LEDs applications needs performing some features as high power factor, flicker-free (continuous output current), high luminous efficacy, long lifespan, luminous flux dimming, high efficiency, universal input voltage (90 – 240 V) and low cost [1]-[3]. It is known that it is very difficult to achieve all these features in a single system. Then, when one LED driver system presents the majority of these features, it becomes a serious candidate to be used in some commercial applications.

LED driver systems having output power over 25 W generally require an AC/DC step-down converter operating in discontinuous conduction mode (DCM) to achieve power factor correction and satisfy the limits set by IEC 61000-3-2 Class C regulations [4], [5]. At DCM, the Buck, Buck-Boost, Boost and Zeta PFC (Power Factor Correction) rectifiers require LC input filters. The boost converter is an inadequate solution for several applications due to its inability to operate in step-down conditions. Regarding the other mentioned classical converters, they do not share a common switch and output reference terminal. It means that the switch driver or any output voltage/current sensor must be isolated, thus leading to a high component count and increased cost [6]. Therefore, the SEPIC converter becomes an attractive option since it addresses this whole list of drawbacks.

The SEPIC PFC rectifier does not need an LC input filter neither an isolated command circuit [7], [8]. Therefore, it has good characteristics for power LEDs applications, where the line current distortion must be low.

Although power electronics converters perform a low input current harmonic distortion due to the inherent property of DCM operation, the low frequency (twice the mains frequency) output voltage ripple is high. Being the LEDs directly connected to the DC bus voltage means that their current also have high ripple, thus reducing their lifespan [9]. In order to reduce the LEDs current ripple a linear regulator is often required [6], [10]-[12]. However, for the losses in the regulator not being very high, it is necessary that the difference between the input and output voltages of the regulator remains as low as possible, preferably on the threshold of regulation. Moreover, this threshold of regulation must be maintained for all DC bus and input voltage variation. Thus, through a programmed optimal point of a linear current regulation it is possible to outfit the system with universal input voltage capability.

It is well known that increasing the parasitic inductances in power converter circuits directly affects the semiconductor devices voltage stress and the system power loss [13], [14]. The employment of snubber circuits contributes for reducing the converter switching losses [15]-[17], since it provides the suppression of sharp rises of switch voltage and current during the commutation process. A resistor-capacitor-diode (RCD) turn-off snubber can be used. However, all snubber energy is dissipated on the resistor R. On adding regenerative capability to this circuit, the energy absorbed during commutation can be recovered to the converter, therefore allowing an improvement on the system efficiency. Regarding the SEPIC operating in DCM [18]-[20], it is possible to observe that it already has its turn-on current slew rate limited by one of its own inductances. Thus, a regenerative snubber acting only toward the reduction of the turn-off switch voltage is enough for minimizing the switching losses.

II. PROPOSED ELECTRONIC LIGHTING SYSTEM

In this paper, an electronic lighting system presenting the features of low input current THD (Total Harmonic

Manuscript received 08/08/2014. First revision 08/11/2014, second revision 12/01/2015. Accepted for publication 12/01/2015, by recommendation of the Regular Section Editor Cassiano Rech.

Distortion) and flicker-free operation is proposed. Moreover, as it is going to be clarified within the paper, this solution is able to operate under universal input voltage range and to perform dimming if a voltage control is proper designed. A regenerative snubber is proposed to harness most of the energy that would be wasted as heat during the switching interval. The efficiency improvement obtained from the use of the proposed snubber shall become more evident in applications where the switching frequency is increased to reduce the circuit size, such as in compact LED lamps.

Figure 1 shows the proposed AC electronic system. It can be observed that the non-isolated SEPIC PFC rectifier is feeding a transistorized linear current regulator with output LEDs load. It can also be observed that a regenerative snubber is used in the SEPIC converter for reducing its switching losses.

SEPIC rectifiers are capable of feeding loads that require low DC voltage level in systems that require high power factor [18]. This solution has the advantages of providing high power factor with low input filtering effort, as Boost rectifiers, and lower output voltage level, as Buck and Buck-Boost rectifiers. The disadvantage is the increase of component count, due to the need for additional capacitor and inductor.

SEPIC converter has important characteristics, which are suitable for LED lighting systems application [18]-[23]:

- step-down voltage operation: the SEPIC is able to operate as a step-down converter. Therefore, the converter can directly supply a LED array [22], [23];
- low input filtering effort: when operating as PFC, no additional input filters are required, even in CCM (Continuous Conduction Mode) or DCM operation;
- resistive mains behavior: when operating in DCM, SEPIC converter has a resistive behavior when observed from the mains. Thus, the converter does not need a current control loop for operating with high power factor [18];
- universal input voltage operation: since the converter has resistive mains behavior in DCM, universal input voltage operation is achieved by adjusting the duty cycle value without any input voltage sensor;
- ground-referred power transistor: the power transistor is referred to the same DC input voltage ground. Thus, the control and drive circuits do not need isolation [22].

For DCM operation, a value of constant k less than its critical value k_{CR} should be adopted.

The voltage gain is defined by:

$$M = \frac{V_o}{V_{in,pk}} \tag{1}$$

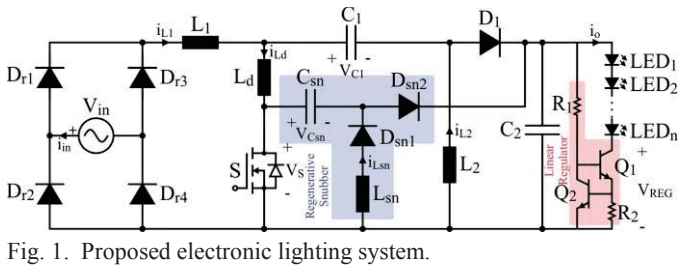

Fig. 1. Proposed electronic lighting system.

where M is the voltage gain, V_o is the output voltage and $V_{in,pk}$ is the input voltage peak value.

The critical value k_{CR} is defined as:

$$k_{CR} = \frac{1}{2(M+1)^2}. \tag{2}$$

Thus, the duty cycle value D is calculated by:

$$D = \sqrt{2}M\sqrt{k}. \tag{3}$$

The inductance of L_1 is calculated by:

$$L_1 = \frac{DV_{in,pk}}{f_s \Delta I_{L1}} \tag{4}$$

where ΔI_{L1} is the input current ripple and f_s is the switching frequency.

The equivalent inductor L_{eq} is given by:

$$L_{eq} = \frac{V_o k}{2I_o f_s} \tag{5}$$

where I_o is the output current.

Therefore, the inductance of L_2 is calculated by:

$$L_2 = \frac{L_1 L_{eq}}{L_1 - L_{eq}}. \tag{6}$$

The intermediate capacitor C_1 is designed for a desired voltage ripple, according to:

$$C_1 = \frac{\left(1-\sqrt{M\bar{I}_o}\right)M\bar{I}_o V_{in,pk}}{2 f_s L_2 \Delta V_{C1}} \tag{7}$$

where $\bar{I}_o$ is the parameterized output current and ΔV_{C1} is the capacitor C_1 voltage ripple;

The parameterized output current is defined as:

$$\bar{I}_o = \frac{2 f_s L_2 I_o}{V_{in}}. \tag{8}$$

Finally, the output capacitance C_2 necessary to maintain a specified value of output voltage ripple is given by:

$$C_2 = \frac{\bar{I}_o V_{in,pk}}{8\pi f_r f_s L_2 \Delta V_o} \tag{9}$$

where f_r: is the mains frequency and ΔV_o is the output voltage ripple.

III. ENERGY REGENERATIVE SNUBBER

In order to reduce the switching losses of the SEPIC rectifier operating in DCM a regenerative snubber is

proposed as depicted in Figure 1. It is composed of one capacitor (C_{sn}), one inductor (L_{sn}) and two diodes (D_{sn1} and D_{sn2}). It is important to observe that, in this case, inductance L_d is not considered to be part of the snubber circuit, since once the converter operates in DCM its switch turn-on current starts from zero and has slope limited by the SEPIC inductance L_2. Thus, there is no need to increase the L_d value and the snubber is only intended to limit voltage slope during the switch S turn-off process. Inductance L_d is here considered in the circuit to represent the stray inductances that are abruptly open by S. It is important to observe that these stray inductances might generate voltage spikes at the switch S terminals. However, these spikes are suppressed when using the proposed snubber, as detailed within this section.

A. Steady State Operation

Figure 2 depicts the sequence of nine operation stages of the proposed SEPIC converter employing the regenerative snubber, which are described as follows:

Stage 1 ($t_0 - t_1$): begins when the switch S is turned on. During this stage, energy is transferred from the input to inductor L_1 and from capacitor C_1 to inductor L_2. Regarding the regenerative snubber circuit, C_{sn} and L_{sn} form a resonant circuit and the energy previously stored in C_{sn} is transferred to L_{sn}. This stage ends at $t = t_1$, when v_{Csn} reaches the value of $-V_o$.

Stage 2 ($t_1 - t_2$): at $t = t_1$, diode D_{sn2} becomes forward biased and energy stored in L_{sn} starts being transferred to the converter's output. As soon as current i_{Lsn} is null this stage ends.

Stage 3 ($t_2 - t_3$): since the entire amount of energy stored in L_{sn} was transferred to the output during the previous stage, both diodes D_{sn1} and D_{sn2} become reverse biased. Thus, the circuit configuration during this stage is the same as the first stage of the conventional SEPIC converter in DCM. Stage 3 ends when the switch S is turned-off.

Stage 4 ($t_3 - t_4$): the consequence of switch S blocking is the bypass of current i_{Ld} to the capacitor C_{sn}, thus limiting the slew rate of voltage across S. At $t = t_4$, v_{Csn} reaches the value of V_{in} causing diode D_1 to become forward biased, and stage 4 is finished.

Stage 5 ($t_4 - t_5$): since diode D_1 started conducting, energy begins to be transferred to converter's output. During this stage, energy stored in L_d continues to be transferred to C_{sn}. At $t = t_5$, i_{Ld} becomes null and v_{Csn} assumes its highest value. It is important to observe that voltage across S also has its maximum value at this time instant, fact that characterizes the end of stage 5.

Stage 6 ($t_5 - t_6$): at $t = t_5$, diodes D_{sn1} and D_{sn2} become forward and reverse biased, respectively. During this stage, L_d, L_{sn} and C_{sn} form a resonant circuit and energy stored in C_{sn} is transferred to C_1 and converter's output. Stage 6 occurs until half of a resonant cycle has elapsed.

Stage 7 ($t_6 - t_7$): as the resonant transitions is over diode D_{sn1} blocks and the circuit configuration becomes the same as the second stage of the conventional DCM SEPIC converter. At $t = t_7$, inductor L_2 assumes all the current provided by L_1, thus blocking diode D_1 and implying the end of stage 7.

Stage 8 ($t_7 - t_8$): with the blocking of D_1, diode D_{sn1} becomes once again forward biased and L_d, L_{sn} and C_{sn} form a resonant circuit as occurred during stage 6. After half of a resonant cycle has elapsed, this stage ends.

Stage 9 ($t_8 - t_9$): at $t = t_8$, the circuit configuration

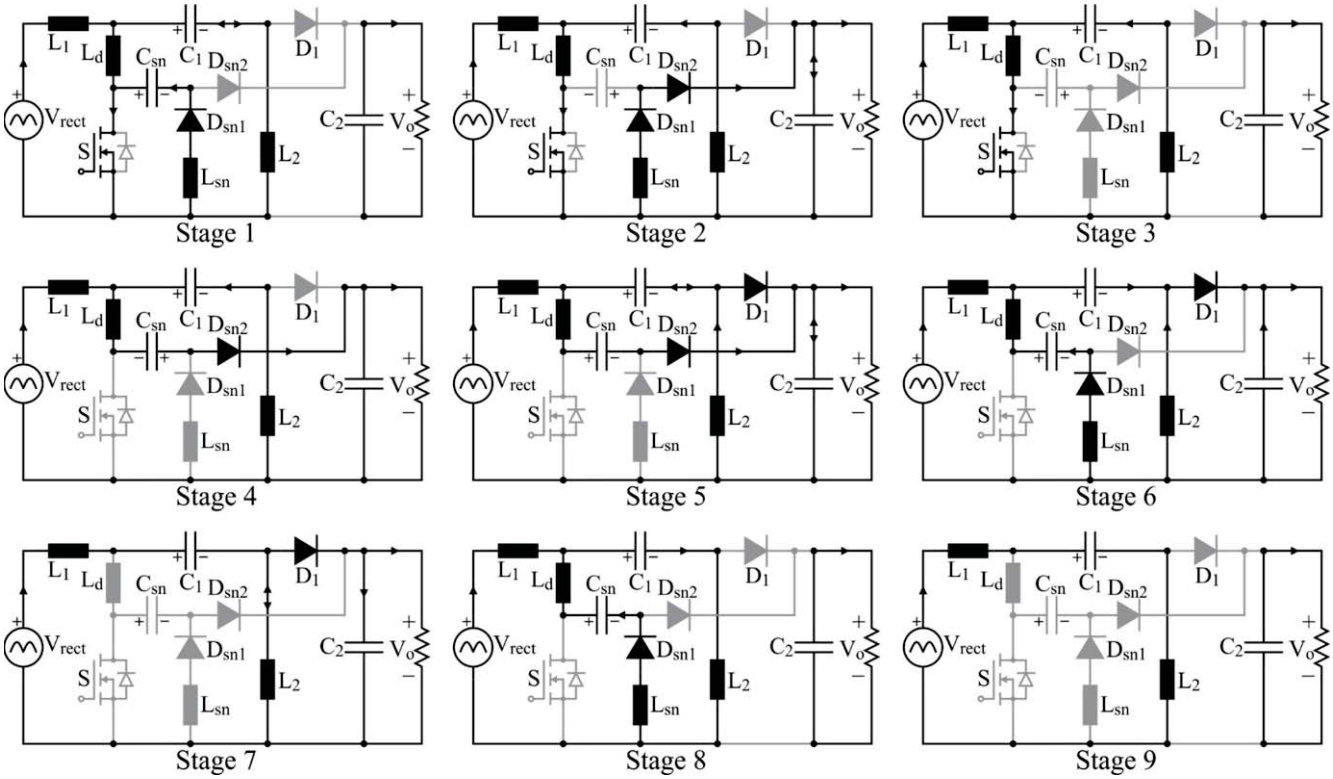

Fig. 2. Operation stages.

becomes the same as the third stage of the conventional DCM SEPIC. This stage persists until switch S is turned on.

Figure 3 shows the theoretical waveforms in steady state operation.

B. Mathematical Analysis

From the analysis of the SEPIC rectifier associated with the proposed regenerative snubber one can demonstrate that the maximum value of voltage across the switch S is given by:

$$V_{S,max} = \sqrt{\frac{L_d}{C_{sn}}}\frac{DV_{in}}{f_s L_2} + V_{in} + V_o. \quad (10)$$

It is important to remember that the maximum switch voltage stress considering the ideal SEPIC converter (no parasitic influence) is equal to V_{in}+V_o, term that appears in (10). Thus, the first term of this equation computes the influence of the stray inductance L_d on the voltage V_S, which maximum value is always higher than that of the ideal case. An interesting fact is that this deviation from the ideal conditions depends on the value of C_{sn} but does not on L_{sn}. Therefore, an adequate choice of capacitance C_{sn} might provide the conditions to keep the voltage stress on switch S limited to some predefined value.

The result given by (10) holds for every operating duty cycle, which is adjusted to maintain a minimum current regulator energy loss (see section IV). Rewriting (8) for the worst case (maximum input voltage) and considering the low frequency ripple on the output voltage, results in:

$$V_{S,max} = \sqrt{\frac{L_d}{C_{sn}}}\frac{\sqrt{M_{min}\bar{I}_{o,min}}V_{in,pk,max}}{f_s L_2} + V_{in,pk,max} + V_{o,avg}\left(1+\frac{\Delta V_{o\%}}{2}\right) \quad (11)$$

where M_{min} is the minimum operating voltage gain and $\bar{I}_{o,min}$ is the parameterized minimum operating output current, $V_{in,pk,max}$ is the maximum peak value of input voltage, $V_{o,avg}$ is the average value of output voltage and $\Delta V_{o\%}$ is the output voltage ripple as a percentage of $V_{o,avg}$.

During the switch S turn-off the slew rate of voltage across this element (SR_{VS}) is limited by the charging of capacitance C_{sn}. From the snubber analysis it is possible to demonstrate de validity of

$$SR_{VS} = \frac{DV_{in}}{f_s L_2 C_{sn}} = \frac{\sqrt{M\bar{I}_o}V_{in}}{f_s L_2 C_{sn}}. \quad (12)$$

Equation (12) provides the means for specifying C_{sn} in order to control the slew rate of voltage across S, thus allowing the reduction of the turn-off loss on this element.

Finally, inductor L_{sn} participates in the process of transferring the energy stored in C_{sn} during the switch turn-off to the output capacitor. Its value directly affects the time that this energy transfer process takes to be performed. Thus, L_{sn} is chosen in order to meet a trade-off between i_{Lsn} peak

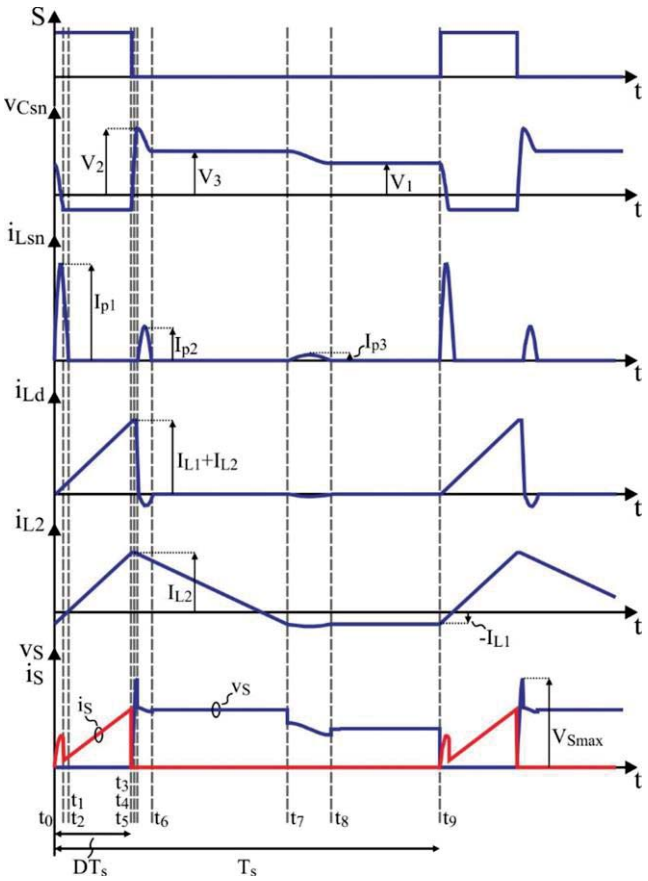

Fig. 3. Theoretical waveforms for steady state operation.

value and the duration of the snubber energy recovery. The snubber analysis provides that

$$I_{Lsn,max} = \sqrt{\frac{L_d}{L_{sn}}}\frac{DV_{in}}{f_s L_d} + \sqrt{\frac{C_{sn}}{L_{sn}}}\left(V_{in} - 2V_o\right). \quad (13)$$

When operating with universal input voltage, $I_{Lsn,pk}$ has an extreme value that occurs when the input voltage is maximum, as given by:

$$I_{Lsn,pk} = \sqrt{\frac{L_d}{L_{sn}}}\frac{\sqrt{M_{min}\bar{I}_{o,min}}V_{in,pk,max}}{f_s L_d} + \sqrt{\frac{C_{sn}}{L_{sn}}}\left(V_{in,pk,max} - 2V_o\right). \quad (14)$$

IV. LINEAR CURRENT REGULATOR WITH MINIMAL ENERGY LOSS

A linear current regulator is used to control the current in the LEDs array [21]-[23]. Being this circuit a linear regulator means that the bipolar transistors Q_1 and Q_2 operate in the active region, which is well known to have a considerable energy loss. The reason for employing such solution is that it simplifies the converter control, where high power factor and current regulation are achieved with a simple voltage controller even for universal input voltage range. This

solution is expected to be adequate for several lighting applications where this extra energy loss is acceptable when considering the benefits of control simplicity, flicker-free, inherent LED overcurrent protection and dimming capability. Moreover, since the output voltage ripple is assumed by the linear regulator, the capacitance value of C_2 may be decreased. However, this implies higher losses in the regulator circuit, as can be observed from (15).

In order to minimize the regulator energy loss, a control strategy might be set for tracking the point where Q_1 power is minimum and yet avoiding the saturation of Q_1 and Q_2. Figure 4 shows the waveform of V_{REG} that leads to minimal losses in the current regulator while active region is guaranteed for both Q_1 and Q_2.

Thus, in closed-loop operation the control strategy would consist of adjusting the SEPIC duty cycle to keep the minimum value of V_{REG} slightly higher than 2.1 V (considering that Q_1 is a Darlington pair). Hence, the linear regulator loss is approximately

$$P_{REG} \approx \left(\frac{\Delta V_o}{2} + 2.1 \right) I_{LED}. \quad (15)$$

Dimming can be performed by setting an adequate value for R_2 (variable resistor in this case), which is responsible for adjusting the LED array current I_o, as given by:

$$I_o \approx \frac{0.7}{R_2}. \quad (16)$$

V. EXPERIMENTAL RESULTS

In order to verify the presented design methodology, a prototype for 35 LEDs connected in series operating in 127 and 220 V / 42 W was implemented in open loop. To drive the proposed lighting system the integrated circuit SG3525 PWM controller is used. Figure 5 shows the implemented circuit. The design data are presented in Table I

Using the equations from Sections II and III the values of the parameters of the SEPIC converter are derived and presented in Table II. Table III provides information about the converter devices. The regenerative snubber is designed considering the stray inductance (L_d) value of 500 nH. Capacitor C_{sn} value is chosen in order to guarantee a maximum switch voltage of 510 V, and inductor L_{sn} is set to a value that ensures that its own peak current value is limited to 1.125 A.

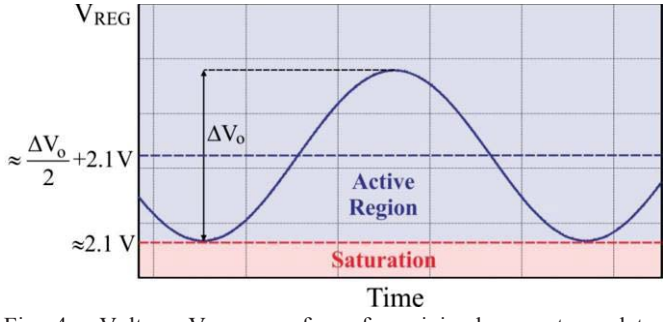

Fig. 4. Voltage V_{REG} waveform for minimal current regulator energy loss.

TABLE I
Data of the Implemented Prototype

Parameters	Values
V_{in} (RMS)	127 and 220 V
V_o (AVG)	126 V ± 5 %
I_o (AVG)	350 mA
P_{LEDs}	42.35 W
f_s	50 kHz
D	0.30 and 0.16
ΔI_{L1}	20 %
ΔV_o	5 %
ΔV_{C1}	35 %

TABLE II
Parameters Used in the Prototype

Parameters	Values
L_1	20.37 mH – Core EE-40/20 IP12R Thornton, 194/33 turns
L_2	318.2 µH - Core EE-30/7 IP12R Thornton, 128 turns
L_{sn}	30 µH – Core EE-16/7 IP12R Thornton, 16 turns
C_1	180 nF
C_2	2 parallel 75 µF (Epcos metallized polypropylene capacitor)
C_{sn}	2.2 nF

TABLE III
Devices Used in the Prototype

Parameters	Devices
D_{r1} - D_{r4}	1N4004
D_1	MUR460
S (MOSFET type CoolMOS™)	SPP24N60C3
D_{sn1} and D_{sn2}	MUR160
Q_1	BC546A + TIP31C (darlington configuration)
Q_2	BC546A
R_1	220 kΩ
R_2	2 Ω
LEDs	LXK2-PWC4-0220

From Figure 6 to Figure 8 the experimental results for an input voltage of 127 V are presented. Figure 6 depicts the input voltage (CH1), input current (CH2) and the current (CH4) and voltage (CH3) on the LEDs array. Figure 7 shows that the current THD is 1.87 %, being all harmonics in compliance with the IEC 61000-3-2 class C standard. It can be observed that there are some ripples on both measurements. As the system has operated in open loop, it there was no control on the minimum voltage of the linear regulator to obtain flicker-free current. In the operation point of minimum voltage, the linear regulator presented instability and the regulator energy loss increased a lot. To minimize

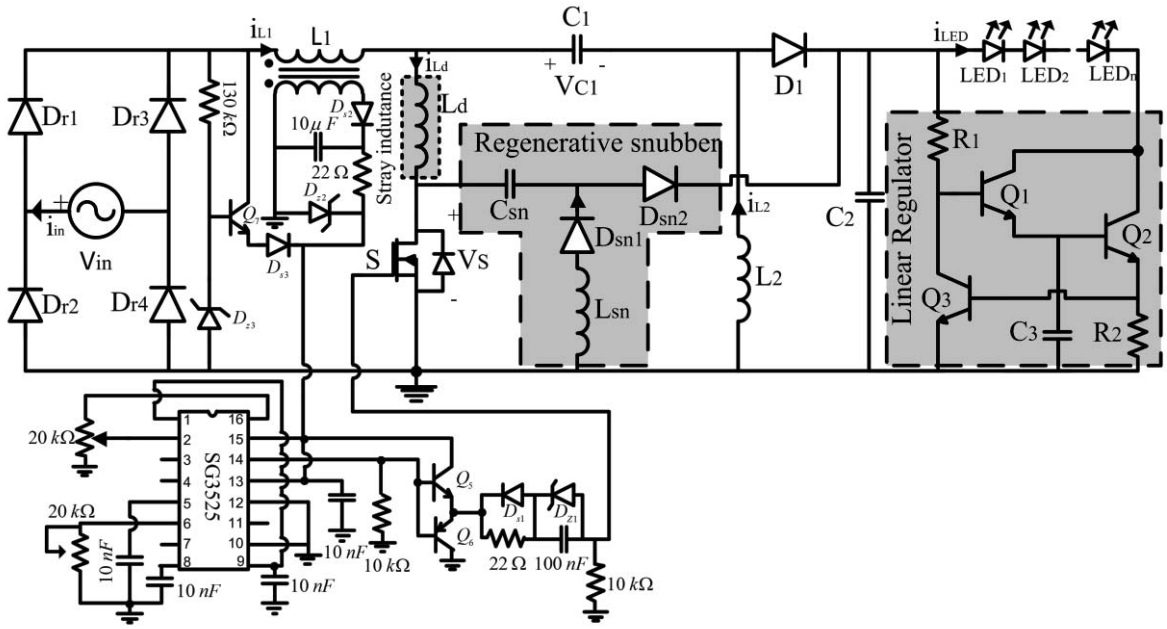

Fig. 5. Implemented circuit diagram.

the regulator energy loss, a control strategy must be set for tracking the point where the linear regulator power is minimum without going a lot into active region.

Figure 8 shows the linear regulator voltage (CH3), the LEDs array voltage (CH1) and current (CH4) and the DC-Link voltage (CH2) for 127 V at power supply. It is possible to observe that the minimum voltage on linear regulator is approximately 2 V and its average value measurement is 4.8 V. Thus, its average energy loss is approximately 1.7 W.

This loss only corresponds to 3.7 % of the total output power of the electronic lighting system. Therefore, this solution seems adequate for applications where this loss penalty is justified by all the features achieved with the proposed reduced components count circuit.

Figure 9 presents the input voltage (CH1) and input

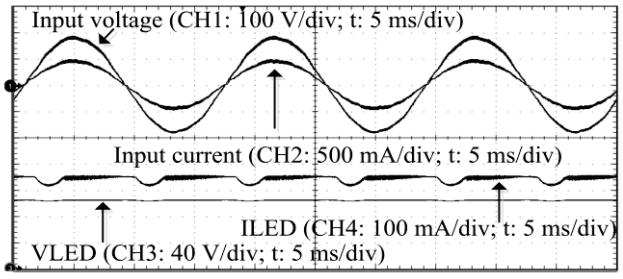

Fig. 6. Input voltage (CH1), input current (CH2), Current (CH4) and voltage (CH3) on the LEDs array for 127 V.

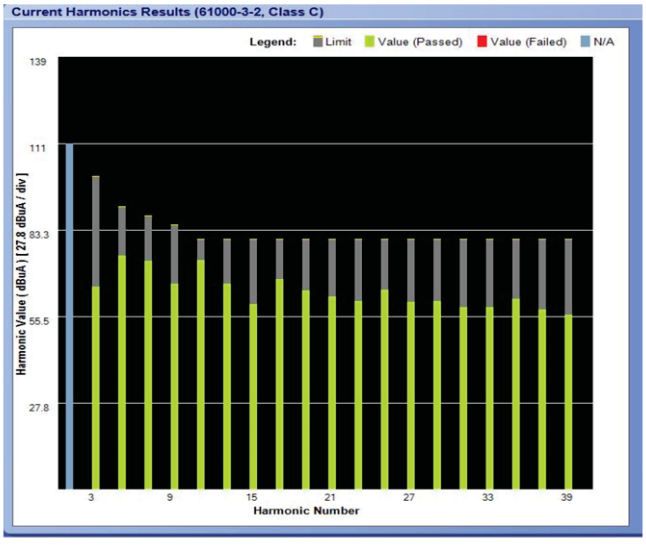

Fig. 7. Harmonic spectrum of the input current with THD of 1.87 %.

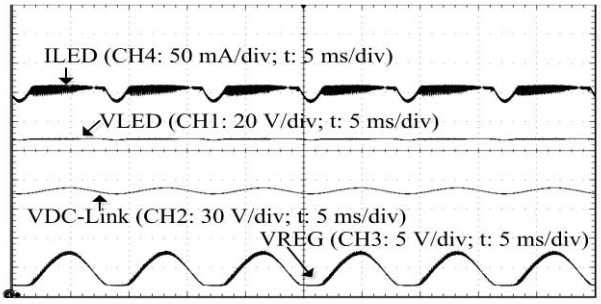

Fig. 8. LEDs current (CH 4), LEDs array voltage V_{LEDs} (CH1), DC link voltage V_{DC} (CH2) and Regulator linear voltage V_{REG} (CH3) for 127 V.

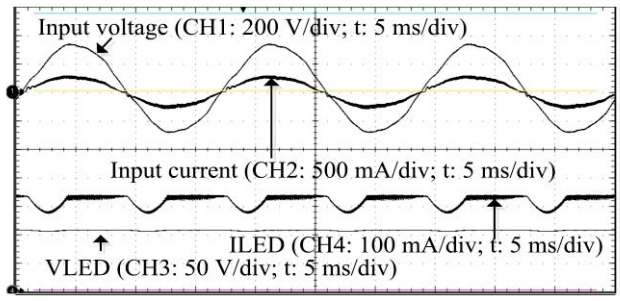

Fig. 9. Input voltage (CH1), input current (CH2), Current (CH4) and voltage (CH3) on the LEDs array for 220 V.

current (CH2) and the current (CH4) and voltage (CH3) on the LEDs array with system being feeding in 220 V. Even though it is not shown the harmonic content of the input current, its THD is 2.5 % with all harmonics satisfying standard IEC 61000-3-2 Class C too. Figure 10 shows the linear regulator voltage (CH3), the LEDs array voltage (CH1), the LEDs current (CH4) and the DC-Link voltage (CH2) for 220 V.

Figure 11 shows the efficiency variations under different input voltage operation conditions, firstly employing the proposed snubber and after employing the RCD snubber (R = 130 kΩ, C = 4.7 nF and MUR160). The system efficiency was measured with a YOKOGAWA WT3000 precision power analyzer, which results are 87.8 % at 127 V and 87.2 % at 220 V of input voltage for the proposed snubber. One can observe that, across the input voltage variation range, using the classical dissipative RCD snubber the system presented an efficiency lower than when employing the proposed regenerative snubber. It is noteworthy that although the efficiency improvement achieved by using the proposed circuit does not seem to be too significant, systems operating at higher switching frequencies should be better benefited from this solution. Perhaps for compact lamps, the recovered switching energy should be higher than that lost in the current regulator, thus leading to minimized efficiency impairment.

Figure 12 presents the inductor L_2 current at low (R1) and switching (CH2) frequencies at 127 V, where it can be observed that the SEPIC operates in DCM.

Figure 13 shows MOSFET voltage and current during the switching process employing the RCD snubber. Figure 14 also presents the detail of MOSFET switching but now considering the use of the proposed regenerative snubber. It can be observed that the switching conditions are better when using the proposed snubber, where the overlap between switch voltage and current is lower than that obtained for the RCD snubber. Moreover, the slew rate of switch voltage is decreased by the use of the proposed snubber, therefore resulting in a system where the electromagnetic interference is possibly reduced.

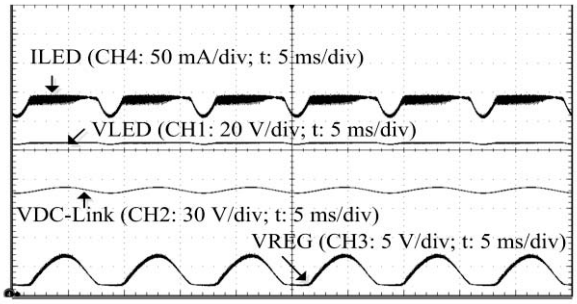

Fig. 10. LEDs current (CH 4), LEDs array voltage V_{LEDs} (CH1), DC link voltage V_{DC} (CH2) and Regulator linear voltage V_{REG} (CH3) for 220 V.

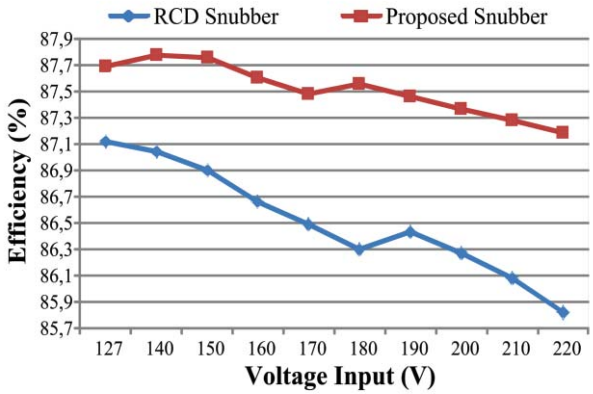

Fig. 11. Efficiency variations under different input voltage operation conditions.

VI. CONCLUSION

This paper presented an alternative solution to reduce the MOSFET switching losses by using an energy-regenerative-snubber applied to the non-isolated SEPIC PFC rectifier. The main goal of this study was to derive the fundamental equations that describe the converter behavior as well as its operation stages and main waveforms, providing the basis for further analyses, such as establishing a proper design

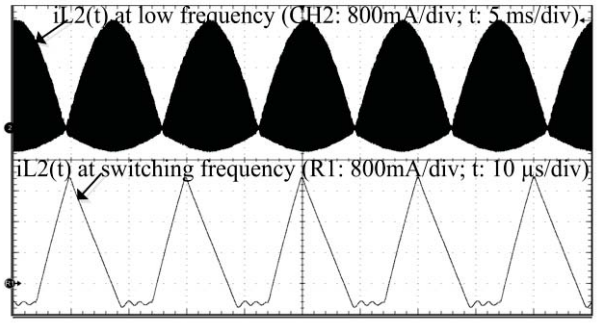

Fig. 12. Inductor L2 current: (R1) Low frequency; (CH2) switching frequency.

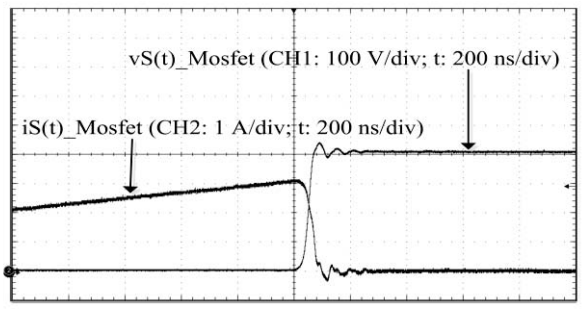

Fig. 13. Voltage (CH1) and current (CH2) on the MOSFET without regenerative snubber.

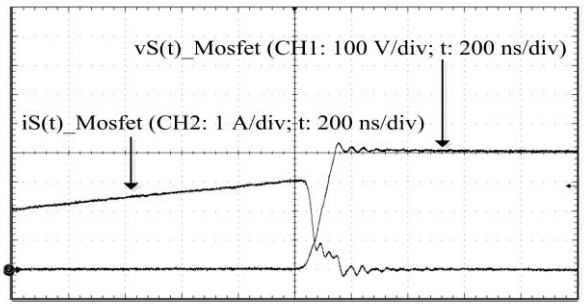

Fig. 14. Voltage (CH1) and current (CH2) on the MOSFET at switching frequency with regenerative snubber.

procedure, evaluation of component current and voltage stresses or even converter optimization. It was shown that the use of a linear current regulator combined with the DCM SEPIC rectifier exhibits interesting characteristics, such as low input current THD, flicker-free operation, universal input voltage and dimming capability, all achieved without any current control loop. However, a loss penalty is inevitable.

Experimental results performed in 127 V and 220 V show that by using the proposed energy-regenerative-snubber, it is possible to improve the system efficiency when compared to the employment of a classical RCD snubber. This improvement may be more accentuated in applications with higher switching frequency, increasingly common in LED lighting for achieving compact lamps. It is noteworthy that the regenerative snubber processes a small portion of the converter rated power and therefore it may not increase the converter's cost and size significantly.

Despite the fact that the results were obtained in open-loop operation, it is shown that by choosing an adequate value of duty cycle, the energy loss in the current regulator is minimized in both conditions of 127 V and 220 V. Thus, a control loop should be proposed for tracking the optimum operation point, being this subject currently under investigation by the authors.

REFERENCES

[1] D. G. Lamar, M. Fernandez, M. Arias, "Tapped-Inductor Buck HB-LED AC–DC Driver Operating in Boundary Conduction Mode for Replacing Incandescent Bulb Lamps," *IEEE Transactions on Power Electronics*, vol. 27, no. 10, pp. 4329 – 4337, Oct. 2012.

[2] S. Wang, X. Ruan, K. Yao, S.-C. Tan, "A Flicker-Free Electrolytic Capacitor-Less AC-DC LED Driver," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4540 – 4548, Nov. 2012.

[3] Y. Hu, L. Huber, M. M. Jovanovic´, "Single-Stage, Universal-Input AC/DC LED Driver With Current-Controlled Variable PFC Boost Inductor," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1579-1588, Mar. 2012.

[4] *Electromagnetic Compatibility (EMC), Part 3-2: Limits-Limits for harmonic current emissions (equipment input current ≤ 16 A per phase)*, International Standard IEC 61000-3-2, 2014.

[5] L. Yu and J. Yang, "The topologies of white LED lamps' power drivers," *in Power Electronics Systems and Applications*, 2009.

[6] Z. P. Fonseca., C. H I. Font, M. S. Kaster., A. J. Perin., C. B. Nascimento, "An electronic AC power system with buck PFC and linear regulator to drive and control the current of power LEDs," *in Brazilian Power Electronics Conference (COBEP),* 2011 Brazilian.

[7] M. F. Silva, J. Fraytag, M. E. Schlittler, T. B. Marchesan, M. A. D. Costa, J. M. Alonso, R. N. Prado, "Análise e Projeto da Topologia Integrada SEPIC Meia Ponte com Controle de Fluxo Luminoso para o Acionamento de Lâmpadas Fluorescentes sem Eletrodos," *Revista Eletrônica de Potência*, v. 18, no. 4 pp. 717-729, Nov. 2012.

[8] J. Fraytag, M. F. Silva, M. E. Schlittler, J. M. A. Álvarez, R. N. Prado, "Modulação PWM de Baixa Frequência Aplicada à Topologia Integrada SEPIC Meia-ponte para o Controle da Intensidade Luminosa de Lâmpadas Fluorescentes sem Eletrodos," *Revista Eletrônica de Potência*, v. 18, no. 1 pp. 843-854, Feb. 2013.

[9] T. F. Pan, H. J. Chiu, S. J. Cheng, and S. Y. Chyng, "An improved single-stage PFC flyback converter for high-luminance lighting LED lamps," *in The 8th International Conference on Electronic Measurement and Instruments*, vol. 4, pp. 212 – 215, 2007.

[10] C. Park and C.T. Rim, "Filter-free AC direct LED driver with unity power factor and low input current THD using binary segmented switched LED strings and linear current regulator," *in Applied Power Electronics Conference and Exposition (APEC)*, 2013.

[11] H. Ma, J. S. Lai, Q. Feng, W. Yu, C. Zheng and Z. Zhao, "A Novel Valley-Fill SEPIC-Derived Power Supply Without Electrolytic Capacitor for LED Lighting Application," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 3057-3071, Nov. 2012.

[12] Y. Hu and M. M. Jovanovic, "LED driver with self-adaptive drive voltage," *IEEE Transactions on Power Electronics*., vol. 23, no. 6, pp. 3116-3125, 2008.

[13] Y. Shen, J.Jiang, Y. Xiong, Y. Deng, X. He and Z. Zeng, "Parasitic Inductance Effects on the Switching Loss Measurement of Power Semiconductor Devices" *in IEEE International Symposium on Industrial Electronics*, vol. 2, pp. 847-852, 2006.

[14] T. Meade, D. O'Sullivan, , R. Foley, C. Achimescu, M. Egan and P. McCloskey, "Parasitic Inductance Effects on the Switching Loss Measurement of Power Semiconductor Devices," *in Applied Power Electronics Conference and Exposition (APEC)*, 2008.

[15] Bonfa, V.A; Menegaz, P.J.M.; Vieira, J. L F; Simonetti, D. S L, "Multiple alternatives of regenerative snubber applied to Sepic and Cuk converters," *in 28th Annual Conference of the Industrial Electronics Society (IECON)*, vol. 1, pp. 123-128, 2002.

[16] Chih-Sheng Liao; Smedley, K.M., "Design of high efficiency Flyback converter with energy regenerative snubber," *in Applied Power Electronics Conference and Exposition (APEC)*, pp. 796-800, 2008.

[17] Abramovitz, A; Tang Cheng; Smedley, K., "Analysis and Design of Forward Converter With Energy Regenerative Snubber," *IEEE Transactions on Power Electronics*, vol. 25, no. 3, pp. 667-676, Mar. 2010.

[18] D. S. L. Simonetti, J. Sebastian. and J. Uceda, "The Discontinuous Conduction Mode Sepic and´ Cuk Power Factor Preregulators: Analysis and Design," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 5, pp. 630-637,1997.

[19] H. Ma, J. S. Lai, Q. Feng, W. Yu, C Zheng and Z. Zhao, "A Novel Valley-Fill SEPIC-derived Power Supply Without Electrolytic Capacitors for LED Lighting Application," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 3057-3071, June 2012.

[20] J. Sebastian, J. A. Cobos, J. M. Lopera and J. Uceda, "The Determination of the Boundaries Between

Continuous and Discontinous Conduction Modes in PWM DC-to-DC Converters Used as Power Factor Preregulators," *IEEE Transactions on Power Electronics*., vol. 10, no. 3, pp. 574-582, 1995.
[21] M. R. Cosetin, E. A. Bitencourt, T. E. Bolzan, M. F. Silva, J. M. Alonso and R. N. do Prado, "Comparison of single stage SEPIC and integrated SEPIC-Buck converter as off-line LED drivers," *in Brazilian Power Electronics Conference (COBEP)*, pp. 1134 – 1139, 2013.
[22] Z. Ye, F. Greenfeld and Z. Liang, "Design considerations of a high power factor SEPIC converter for high brightness white LED lighting applications," *in Power Electronics Specialists Conference*, pp. 2657 – 2663, 2008.
[23] C. Walding, "High Current LED - Isolated Low Voltage AC Drive," *ON Semiconductor, Application Note*, 2003.
[24] E. M. Sa Jr, "Estudo de Estruturas de Reatores Eletrônicos para LEDs de Iluminação," Thesis in Portuguese, UFSC, 2010.
[25] C. R. B. S. Rodrigues, P. S. Almeida, G. M. Soares, M. F. Braga, and H. A. C. Braga, "A Novel Linear Circuit for Current Equalization in Led Strings," *Revista Eletrônica de Potência*, v. 18, no. 3, p.1109-1117, 2013.

BIOGRAPHIES

Ismael Burgardt was born in Ponta Grossa, Paraná, Brazil, in 1989. He received the B.E. degree in electronic engineering from Federal University of Technology, Ponta Grossa, Brazil, in 2013, where he is currently pursuing the M.S. degree. His research interests include lighting system and power converters.

Eloi Agostini Junior was born in Lages, SC, Brazil, in 1983. He received the B.S., M.S. and Ph.D. degrees from the Federal University of Santa Catarina in 2006, 2008 and 2012, respectively. He is currently a Professor in the Electronics Department of the Federal University of Technology – Paraná. His research interests include power converters, soft-switching, power factor correction, converter modeling and renewable energy processing.

Carlos Henrique Illa Font was born in Erval Grande, RS, Brazil, in 1976. He received the B.S., M.S. and Ph.D. degrees from the Federal University of Santa Catarina in 2001, 2003 and 2009, respectively. He is currently a Professor in the Electronics Department of the Federal University of Technology – Paraná. His research interests include power factor correction, high power factor rectifiers and switching-mode power supply.

Claudinor Bitencourt Nascimento was born in Tubarão, Santa Catarina, Brazil, in 1971. He received the B.E., M.S., and Ph.D. degrees in electrical engineering from Federal University of Santa Catarina, Florianópolis, Brazil, in 1994, 1996, and 2005, respectively. He has worked in the Electronics Department of the Federal University of Technology - Paraná, Ponta Grossa, Brazil, since 1997, where he is currently Professor of Power Electronics and Automation and Control. He is currently the Coordinator of Postgraduate Program in Electrical Engineering, Campus of Ponta Grossa, where he was engaged in education and research on power electronics. His research interests include lighting system, power-factor-correction circuits and new converter topologies.

.