BIDIRECTIONAL FLYBACK-PUSH-PULL DC-DC CONVERTER

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***Abstract* - This paper presents a bidirectional flyback-push-pull dc-dc converter. The main characteristics of the proposed converter are galvanic isolation by high-frequency transformers, high efficiency, reduced number of components and low current ripple at both the input and output DC power supplies. The typical applications include isolated bidirectional interface between two low voltage DC buses, where low current ripple is required. The study presents theoretical analysis, design example and experimental data for an 800 W, 80 VDC input, 160 VDC output and 50 kHz of switching frequency, on the laboratory prototype. The measured performance and theoretical predictions were in good agreement.**

***Keywords* – High-Current, Isolated, Low-Current Ripple, Low-Voltage, Push-Pull, Simmetrical Bidirectional Dc-Dc Converter.**

NOMENCLATURE

α	Subscript indicating transformer side, p for primary and s for secondary
a	Secondary-Primary winding turns ratio
$carrier_x$	Carrier signal relating to g_{px}
$C_{g\alpha}$	Clamping circuit capacitor of α side
D	Duty cycle
$D_{g\alpha k}$	Clamping circuit diode k of α side
$D_{\alpha k}$	Diode of switch $S_{\alpha k}$
E_α	Voltage Source of α side
f_s	Switching frequency
$g_{\alpha k}$	Transistor $T_{\alpha k}$ gating signal
i_α	Current through E_α source
I	Current level value of i_p
ΔI	Current ripple
i_{s_ref}	Reference signal of i_s
k	Numeric subscript
$L_{FB\alpha}$	Flyback winding of α side
$L_{PP\alpha k}$	Push-Pull winding k of α side
$l_{FB\alpha}$	Leakage inductance of $L_{FB\alpha}$ winding
$l_{PP\alpha k}$	Leakage inductance of $L_{PP\alpha k}$ winding
m	Modulating signal
p_{con}	Power processed by the converter
p_{FB}	Power processed by flyback transformer
q	Static gain
$R_{g\alpha}$	Clamping circuit resistor of α side
$S_{\alpha k}$	Switch k of α side
T_{FB}	Flyback transformer
T_{PP}	Push-Pull transformer
T_s	Switching period
$T_{\alpha k}$	Transistor of switch $S_{\alpha k}$
Δt	Duration of operation stage
V_{Sxy_max}	Theoretical maximum voltage across S_{xy} switch
$x_{(n)}$	Value of x during stage n
$\langle x \rangle$	Average value of x over half-switching period
$\bar{X}$	Normalized value of X
$X_{[n]}$	Magnitude of the nth harmonic of X
X_o	Value of X in a given operation point
ΔX	Variation of X around X_o

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I. INTRODUCTION

The electrical load of conventional automobile has increased over the recent years due to the improve of passenger conveniences, such as air conditioner and audio system, and safety, e.g. electric assist steering and ABS brake system, to a degree that the current 14 V electrical power system can no longer meet the energy demand of the vehicle [1], [2]. A new power system has already been proposed to increase the voltage bus to 42 V [3] but this change cannot be done immediately since most of the automotive devices are rated to the current power system voltage. Therefore, a provisional power system with two voltage buses, 14 and 42 V, is necessary to enable this transition. A possible power system architecture is to employ one battery with each rated voltage. Higher power loads, alternator and starter motor are connected to the 42 V battery and lower power loads to the 14 V battery. A bidirectional dc-dc converter is required to interface the two buses in order to: 1) charge the low voltage battery and 2) transfer power from low voltage battery to high voltage bus during critical events such as starting of the internal combustion engine. Galvanic isolation between the two buses is an interesting property to avoid failures related to loss of common ground reference [4]. If the batteries and loads are connected to the same electrical point, a load reference loss establishes a circuit which the higher voltage battery charges the lower voltage one. Since the batteries are of different voltages levels, the batteries voltages will not be equalized and the charge process will continue until the low voltage battery will be overcharged. In this condition, the voltage polarity applied to the low voltage load is inverted. Additionally, low current ripple is required in both batteries to prevent decrease of its life span. These two features are dependable by the choice of the bidirectional dc-dc converter.

Several isolated bidirectional converters were proposed in the recent years that can be employed to aforementioned application. The dual active bridge (DAB) [5], the dual half-bridge (DHB) and their topological variations [6] usually are very interesting options for high voltage buses, about 400 V,

since they present soft switching, high efficiency and high power density. However, filters are necessary at input and output to reduce current ripple and its efficiency decreases for low voltage and high current applications due to the large amount of reactive power that circulates inside the converter. Modulation strategies [7]–[11], design methodologies [12]–[14] and adaptive circuitry [15] were proposed to minimize reactive power at the cost of increasing operation principle complexity. Full-bridge, half-bridge and push-pull topologies [16]–[20] are alternatives to reduce current ripple and present low current ripple in one of the side but still requires a current filter for the other side. This current ripple can be minimized if the duty cycle range is restricted to a region near to the value which occurs zero current ripple. Normally, this value is also the theoretical upper limit and it is not feasible due to prevent short circuit with the transistors and voltage source. Hence, operation with zero current ripple in both sources is not possible. The bidirectional Cùk converter [21], [22] presents low current ripple at both input and output but its efficiency decreases for higher power applications. Moreover, all the topologies above mentioned requires a bulky dc blocking capacitor or an active winding current control to prevent transformer saturation.

In this research, an isolated bidirectional flyback-push-pull dc-dc converter topology is proposed. Thereby, it has some desirable advantages as compared with the solutions mentioned above, namely (a) two switches in each side with a common gate reference; (b) distributed current stress among switches; (c) no need for split dc capacitor; (d) only two switches in the current path and (e) inherent protection against push-pull transformer core saturation in both power flow directions. As the proposed circuit belongs to the push-pull family, the theoretical voltage across the power switches is approximately the double of the DC voltage of the related voltage source; therefore, it is not appropriate for high voltage applications. Thus, as it will be demonstrated hereafter, it is suitable for low voltage and high current applications.

II. PROPOSED CONVERTER AND OPERATION PRINCIPLE

Figure 1 shows the power stage diagram of the proposed flyback-push-pull converter topology, along with typical gate signals. A modulating signal m is compared to two sawtooth waveforms signals phased by each other by $180°$, $carrier_1$ and $carrier_2$, to generate transistors gating signals. Both transformers have the same secondary-primary windings turns ratio a.

The modulation strategy consists of gating transistors T_{p1} and T_{p2} by two signals, g_{p1} and g_{p2}, with the same duty cycle, D, and frequency, f_s, but shifted by half the switching period. Transistor T_{s1} and T_{s2} gating signals, g_{s1} and g_{s2}, are complementary with T_{p2} and T_{p1} ones, respectively. Although dead time between the g_{p1} and g_{s2} signals is needed as well as between the g_{p2} and g_{s1} signals, it is not required between transistors gating signals from the same side. The duty cycle can vary from zero to unity, hence, and there are two operation modes: one in which the primary transistor gating signals are not overlapped and another, in which they are. Since this is

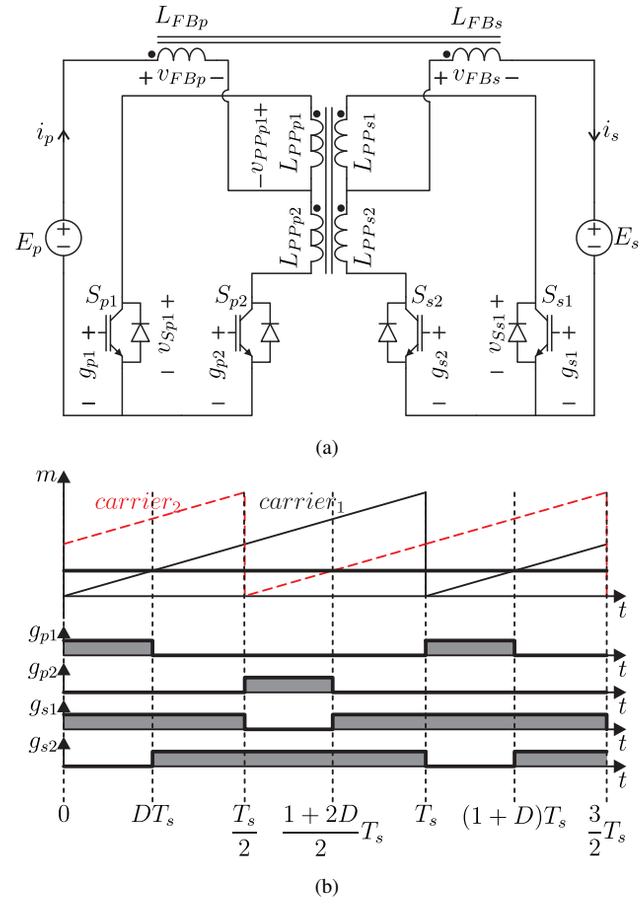

Fig. 1. (a) Power stage diagram of the proposed isolated bidirectional dc-dc converter and (b) the corresponding typical modulator waveforms.

a bidirectional converter, there are two sub-modes depending on the power flow directional to each mode above mentioned. Table I defines these operation modes.

TABLE I
Operation Modes

Power Flow	$0 < D < 0.5$	$0.5 < D < 1$
Primary to secondary	$\text{Buck}_{\text{p}\rightarrow\text{s}}$	$\text{Boost}_{\text{p}\rightarrow\text{s}}$
Secondary to primary	$\text{Boost}_{\text{s}\rightarrow\text{p}}$	$\text{Buck}_{\text{s}\rightarrow\text{p}}$

The buck and boost analogies are used since this converter presents similar pulsed or continuous current characteristics at the input and output.

Although there are four operation modes, only $\text{Buck}_{\text{p}\rightarrow\text{s}}$ and $\text{Boost}_{\text{p}\rightarrow\text{s}}$ modes will be described herein due to the converter input-output symmetry. However, in the following description, the switches will be considered ideal, and also, transformers have very high magnetizing inductance. Only the first half switching period will be described as the other half is analogous. In the illustrations of the topological state, a circle at the transistor gate will be used as the symbol that represents it is enabled.

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A. *Buck*$_{\mathrm{p}\rightarrow\mathrm{s}}$ *Operation Mode*

First stage: at the instant $t = 0$, transistors T_{p1} and T_{s1} are enabled, but due to the current i_s direction, diode D_{s1} conducts instead of T_{s1}. Transistors T_{p2} and T_{s2} are disabled. Current flows through both flyback windings. Figures 2 (a) and (c) show this topological state and its equivalent circuit referred to the secondary side. Figure 2(c) demonstrates that the difference between the sources voltages is applied on the windings. Half of this value is applied to each winding since both transformers have the same secondary-primary windings turns ratio. The v_{PPp1} voltage is the difference between v_{FBp} and E_p. Therefore v_{Sp2} is twice this value and v_{Ss2} is equal to this value referred to the secondary side.

Second stage: at the instant $t = DT_s$, transistor T_{p1} is turned off and T_{s2} turned on, while T_{p2} and T_{s1} maintain their previous state. Although T_{s1} and T_{s2} are both gated on, the current i_s flows through diodes D_{s1} and D_{s2}. This current also flows through the flyback transformer secondary winding, and its value is twice the value at the end of the previous stage due to the magnetic flux conservation. Figures 2(b) and (d) show this topological stage and its equivalent circuit referred to the secondary side, respectively. In this case, as it can be seen in Figure 2(d), the secondary source voltage is only applied across L_{FBs}, and the primary source does not affect the windings voltages. The voltages across the push-pull transformer windings are zero. As a consequence, voltages v_{Sp1} and v_{Sp2} are the sum of E_p and the secondary source voltage referred to the transformer primary side.

Figure 3 shows the relevant waveforms for the converter operating in Buck$_{\mathrm{p}\rightarrow\mathrm{s}}$ mode.

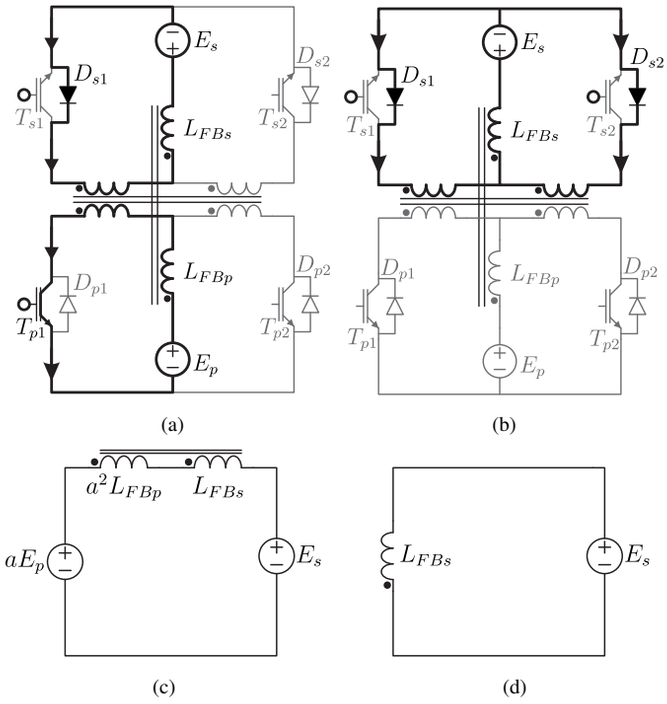

Fig. 2. (a) First operation stage and (c) its equivalent circuit in Buck$_{\mathrm{p}\rightarrow\mathrm{s}}$ operation mode. (b) Second operation stage and (b) its equivalent circuit in Buck$_{\mathrm{p}\rightarrow\mathrm{s}}$ operation mode.

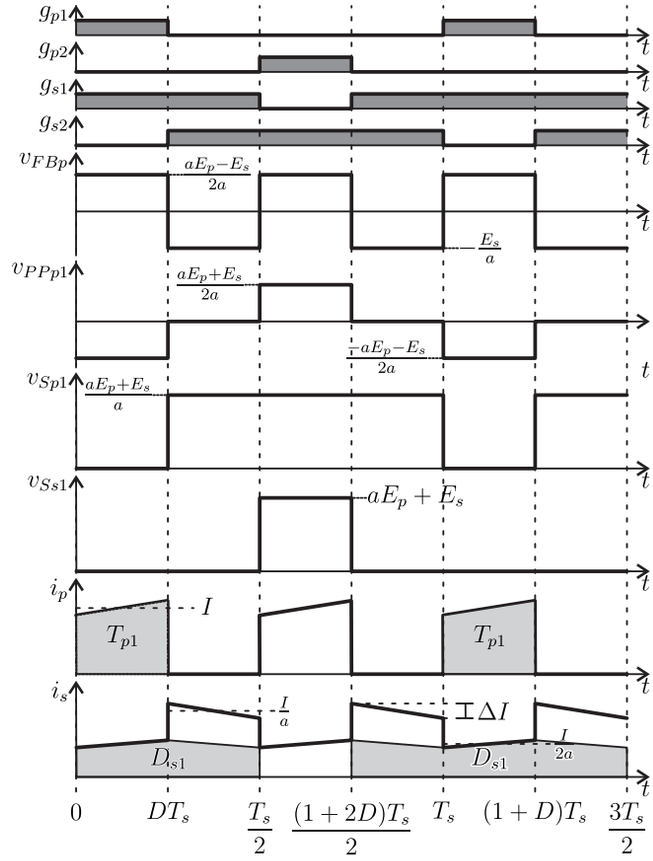

Fig. 3. Main theoretical waveforms for Buck$_{\mathrm{p}\rightarrow\mathrm{s}}$ operation mode.

B. *Boost*$_{\mathrm{p}\rightarrow\mathrm{s}}$ *Operation Mode*

First stage: this operation stage begins at the instant $t = T_s/2$, transistors T_{p1} and T_{p2} are enabled, and each one starts conducting half of the transformer primary current i_p. Transistors T_{s1} and T_{s2} are disabled. Figures 4(a) and (c) show this topological state and the equivalent circuit referred to the primary side, respectively. Figure 4(c) depicts that E_p voltage is entirely applied on flyback winding L_{FBp} and the E_s voltage does not have influence on the windings voltages. The voltage across the push-pull transformer windings are null and therefore v_{Ss1} and v_{Ss2} are equal to the voltage sum of E_s and the E_p referred to the secondary side.

Second stage: at the instant $t = (2D-1)T_s/2$, transistor T_{p2} is turned off and transistor T_{s1} is turned on. Although transistor T_{s1} is enabled, current i_s flows through diode D_{s1}. The current i_p is reduced to half of its previous value in order to maintain the magnetic flux unchanged, through the flyback transformer core. Figure 4(b) shows the topological state and Figure 4(d) illustrates its equivalent circuit referenced to the primary side. According to Figure 4(d), the difference between the sources voltages is imposed across the transformer windings, like in the first stage of the Buck$_{\mathrm{p}\rightarrow\mathrm{s}}$ operation mode. Thereby, the v_{Sp2} and v_{Ss2} have the same values like in the Buck$_{\mathrm{p}\rightarrow\mathrm{s}}$ operation mode case.

Figure 5 shows the main waveforms for the converter operating in Boost$_{\mathrm{p}\rightarrow\mathrm{s}}$mode.

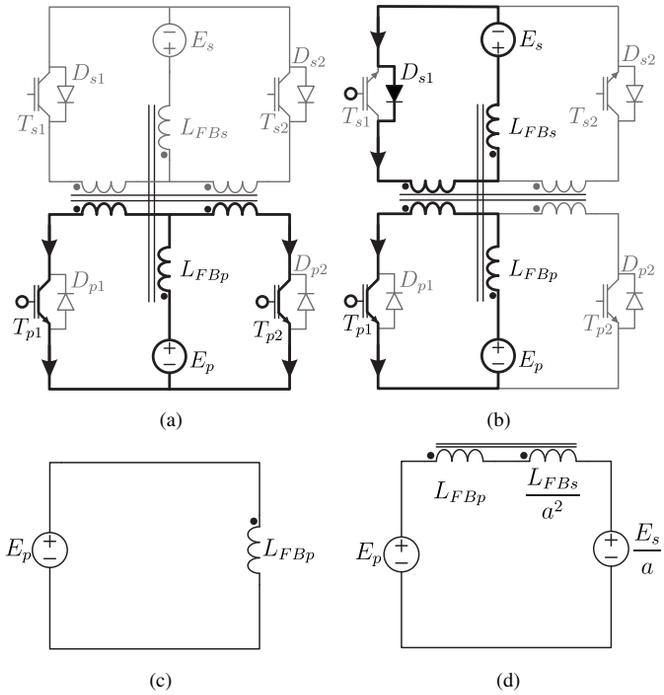

Fig. 4. (a) First operation stage and (c) its equivalent circuit in $\text{Boost}_{\text{p}\to\text{s}}$ operation mode. (b) Second operation stage and (b) its equivalent circuit in $\text{Boost}_{\text{p}\to\text{s}}$ operation mode.

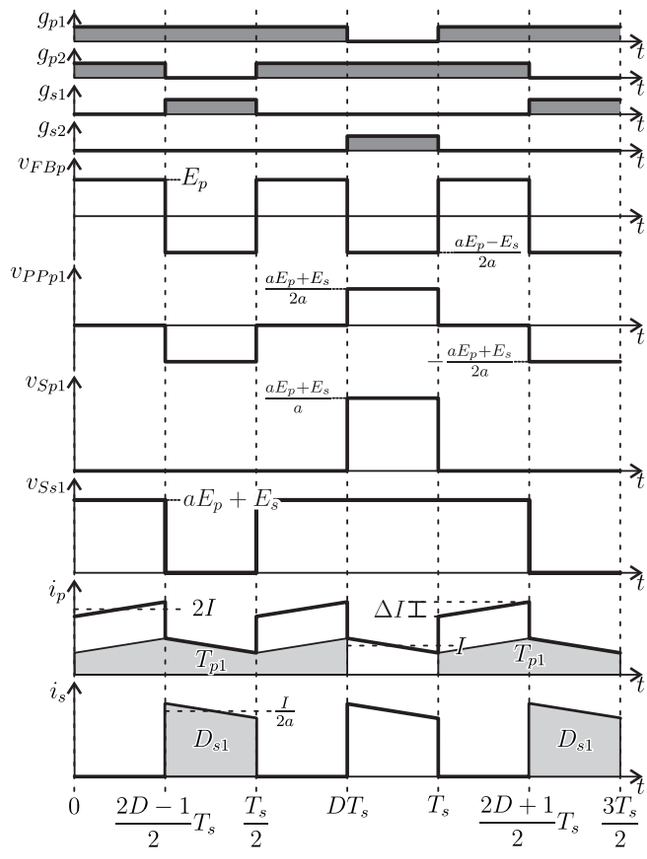

Fig. 5. Main theoretical waveforms for $\text{Boost}_{\text{p}\to\text{s}}$ operation mode.

III. STEADY STATE QUANTITATIVE ANALYSIS

In this section, besides the static gain, maximum voltage across semiconductors, power transferred by the flyback transformer and primary and secondary current harmonic components are presented as function of the duty cycle.

A. Static Gain

In the steady state operation, the average flyback winding voltage is zero over a switching period interval and this restriction is used to determine the converter static gain. As stated before, this converter operates in four operation modes depending on the power flow and duty cycle value. The power flow does not affect the flyback windings voltage waveforms and, therefore, it will not be considered. Hence, only the duty cycle will be taken into account. The average value of the voltage v_{FBp}, according to Figures 3 and 5, can be represented by:

$$\frac{2}{T_s}\left(v_{FBs(1)}\Delta t_{(1)} + v_{FBs(2)}\Delta t_{(2)}\right) = 0. \tag{1}$$

Substituting the values given in Figure 3, into (1), yields:

$$\frac{2}{T_s}\left(\frac{aE_p - E_s}{2a}DT_s - \frac{E_s}{a}\frac{2D-1}{2}T_s\right) = 0. \tag{2}$$

After appropriate algebraic manipulation, static gain in $\text{Buck}_{\text{p}\to\text{s}}$ and $\text{Boost}_{\text{s}\to\text{p}}$ operation modes can be obtained and it is given by:

$$q(D) = \frac{E_s}{E_p} = a\frac{D}{1-D}. \tag{3}$$

For $\text{Boost}_{\text{p}\to\text{s}}$ and $\text{Buck}_{\text{s}\to\text{p}}$ operation modes cases, this procedure can be replicated by employing Figure 5. The result is the same as shown by (3).

The normalized static gain, shown by (4), is obtained dividing $q(D)$ by a, so that:

$$\bar{q}(D) = \frac{D}{1-D}. \tag{4}$$

B. Voltage Stress Across Semiconductors

According to the waveforms depicted in Figures 3 and 5, the maximum voltages across primary and secondary side switches are given respectively by:

$$V_{Spk\_max} = \frac{aE_p + E_s}{a} \tag{5}$$

$$V_{Ssk\_max} = aE_p + E_s. \tag{6}$$

Equation (7) is obtained by isolating E_s in (3) and replacing it into (5).

$$V_{Spk\_max} = \frac{E_p}{1-D} \tag{7}$$

The maximum voltage across secondary switches can be rewritten as function of duty cycle and secondary source voltage by isolating E_p in (3) and substituting it into (6), so that:

$$V_{Ssk\_max} = \frac{E_s}{D}. \tag{8}$$

The normalized maximum voltage across primary and secondary switches, represented by (9) and (10) respectively, are obtained dividing V_{Spk} by E_p and V_{Ssk} by E_s .

$$\bar{V}_{Spk\_max} = \frac{1}{1-D} \tag{9}$$

$$\bar{V}_{Ssk\_max} = \frac{1}{D} \tag{10}$$

C. Power Transferred by Flyback Transformer

The power transferred by the flyback transformer, $\langle p_{FB} \rangle$, in $\text{Buck}_{\text{p}\rightarrow\text{s}}$ and $\text{Boost}_{\text{p}\rightarrow\text{s}}$ operation modes is determined in this subsection. Primary and secondary current ripple, ΔI, is disregarded. Also, the intermediary steps are not presented for the sake of simplicity.

The power processed by the converter in both operation modes is calculated by:

$$\langle p_{con} \rangle = \frac{2}{T_s} \int_0^{\frac{T_s}{2}} E_p i_p dt$$

$$\langle p_{con} \rangle = 2DE_pI. \tag{11}$$

The average power transferred by the flyback transformer is determined by:

$$\langle p_{FB} \rangle = \left| \frac{2}{T_s} \int_0^{\frac{T_s}{2}} v_{FBp} i_p dt \right|$$

$$\langle p_{FB} \rangle = \begin{cases} E_pI\dfrac{1-2D}{D(1-D)} & \text{if D} < 0.5 \\ E_pI(2D-1) & \text{if D} > 0.5 \end{cases}. \tag{12}$$

The normalized power transferred by the flyback transformer is obtained by dividing (12) by (11), and resulting in:

$$\bar{p}_{FB} = \begin{cases} \dfrac{1-2D}{2(1-D)} & \text{for D} < 0.5 \\ \dfrac{2D-1}{2D} & \text{for D} > 0.5 \end{cases}. \tag{13}$$

D. Primary and Secondary Current Harmonic Components

Primary current harmonic components are determined by:

$$\left|I_{p[n]}\right| = \left| \frac{4}{T_s} \int_0^{\frac{T_s}{2}} i_p e^{-jn\frac{4\pi}{T_s}t} dt \right|$$

$$\left|I_{p[n]}\right| = \begin{cases} 2\left|I\right| D & \text{if n} = 0 \\ \dfrac{\sqrt{2}\left|I\right|}{\pi n}\sqrt{1-cos(n4\pi D)} & \text{if n} > 0 \end{cases}. \tag{14}$$

The normalized primary current harmonic components are obtained dividing (14) by the primary current average value, so that:

$$\left|\bar{I}_{p[n]}\right| = \frac{\sqrt{1-cos(n4\pi D)}}{\sqrt{2}\pi nD}. \tag{15}$$

The same procedure can be applied to the secondary current, resulting into:

$$\left|\bar{I}_{s[n]}\right| = \frac{\sqrt{1-cos(n4\pi(1-D))}}{\sqrt{2}\pi n(1-D)}. \tag{16}$$

Figure 6 shows the normalized static gain, normalized maximum voltage across semiconductors, normalized power transferred by flyback transformer and normalized harmonic components of the currents in primary and secondary sources versus duty cycle. As it can be noted, the current harmonic components magnitude and power transferred by flyback transformer is zero for duty cycle equal to 0.5. Thus, the primary and secondary current distortion is low, and the flyback transformer has reduced size if the converter operates near this duty cycle. The voltage across the semiconductors is also minimized for this operation point.

IV. COMPARISON BETWEEN THE PROPOSED CONVERTER AND THE CONVENTIONAL PUSH-PULL

A comparison between the proposed converter and the conventional push-pull converter will be presented in this section taking into account the source current ripple feature. The push-pull topology is chosen due to its similarities with the proposed converter: same number of switches and magnetic elements but the analysis is also valid to full-bridge and half-bridge topologies. The proposed converter input and output current ripple are null if the duty cycle is 50 %, as presented in Section III. However, this condition restrains the static gain to a constant value. Generally, the static gain must vary in a range due to source voltage variation and, consequently, the duty cycle also varies. This variance influences differently the current ripple of each converter.

In order to demonstrate this characteristic, two designs were made considering the application presented in Section I, one for each topology. The push-pull voltage source side is connected to the 42 volts battery and the current source side to the low voltage battery. In automotive applications, the battery voltage is around 13 volts but it may vary between 11 and 16 volts depending on the situation, i.e., the static gain varies between 0.261 to 0.381. The secondary-primary winding turns ratio is adjusted to let the converters operate in the best duty cycle zone from the current ripple point of

view. For both converters, this zone is near 50 % . In the case of the proposed converter, duty cycle can vary between 0.449 and 0.542 and, in the push-pull case, the theoretical interval is between 0.344 and 0.5. In practice, 50 % duty cycle must be avoid for push-pull to prevent short circuit between switches and voltage source, hence, the duty cycle upper limit must be lower than 50 % by a safety margin. In this design, a 5 % margin is employed, therefore, the push-pull duty cycle interval is between 0.3 and 0.45.

The push-pull low voltage side current will be considered ripple free. The push-pull high voltage side current waveform is similar to the proposed converter i_p current for duty cycle lesser than 50 %, therefore, (15) can be used to evaluate its current harmonic components. Figure 7 shows the fundamental harmonic component amplitude of the converters primary and secondary normalized current versus battery voltage variation. The PP and $FBPP$ symbols refer to push-pull and the proposed converter caes, respectively.

In the case of the push-pull converter, the $\bar{I}_{s[1]}$ current has no ripple but $\bar{I}_{p[1]}$ current is almost unitary in the worst case scenario. On the other hand, the proposed converter input/output currents present around 20 % fundamental harmonic component amplitude. At least, one current filter is necessary for each case. This filter can be composed just of a capacitor connected in parallel with the battery and its capacitance is determined by the current harmonic spectrum. Higher current harmonic component amplitude requires higher capacitance and rated RMS current capacitor and, consequently, a more voluminous component. Hence, although the proposed converter requires filters for both batteries, its total filter volume will be smaller than the volume of the push-pull filter since push-pull $\bar{I}_{p[1]}$ is larger than the sum of proposed converter $\bar{I}_{p[1]}$ and $\bar{I}_{s[1]}$ currents.

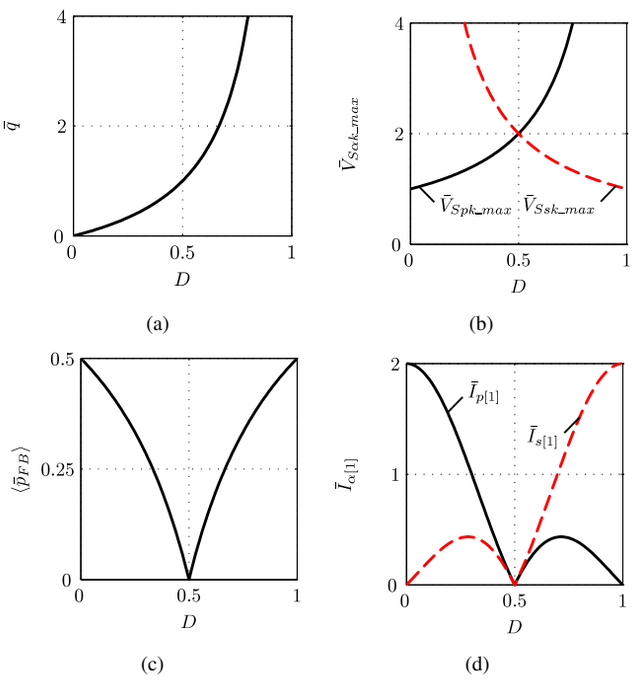

Fig. 6. (a) Normalized static gain, (b) normalized maximum voltage across primary and secondary side semiconductors, (c) normalized power transferred by flyback transformer and (d) normalized fundamental component of primary and secondary currents versus duty cycle.

V. CURRENT CONTROL

In application where the converter interfaces two voltage sources, current control is necessary to establish the processed power value and its direction. Therefore, $\langle i_s \rangle$ current transfer function is essential and, thence, its deduction will be presented in this section.

Equation (17) represents the average value over half switching period of the voltage v_{FBs}.

$$\langle v_{FBs} \rangle = \frac{L_{FBs}}{a} \frac{d}{dt} (\langle i_p \rangle + a \langle i_s \rangle) \tag{17}$$

Equation (18) represents the converter static gain in terms of average input and output currents.

$$\langle i_p \rangle = \frac{aD_o}{1 - D_o} \langle i_s \rangle \tag{18}$$

Equation (19) is obtained by replacing (18) into (17).

$$\langle v_{FBs} \rangle = \frac{L_{FBs}}{1 - D_o} \frac{d \langle i_s \rangle}{dt} \tag{19}$$

The voltage $\langle v_{FBs} \rangle$ is also given by:

$$\langle v_{FBs} \rangle = \frac{E_s}{D_o} D - E_s. \tag{20}$$

Equation (21) is obtained by replacing (20) into (19) and manipulating it properly.

$$\frac{d \langle i_s \rangle}{dt} = \frac{1 - D_o}{L_{FBs}} \left(\frac{E_s}{D_o} D - E_s \right) \tag{21}$$

Current $\langle i_s \rangle$ and duty cycle D can be rewritten respectively as:

$$\langle i_s \rangle = \langle I_{so} \rangle + \Delta \langle i_s \rangle \tag{22}$$

$$D = D_o + \Delta D. \tag{23}$$

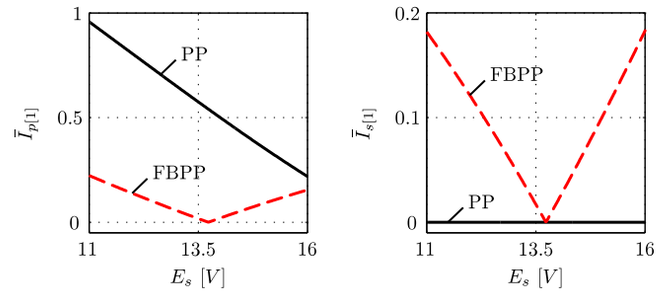

Fig. 7. Comparison between normalized fundamental harmonic component input/output current of the proposed converter and push-pull considering E_s voltage variation.

Equation (24) is obtained by replacing (22) and (23) into (21).

$$\frac{d\Delta\langle i_s\rangle}{dt} = \frac{1-D_o}{D_o}\frac{E_s}{L_{FBs}}\Delta D \tag{24}$$

After the application of the Laplace transform, the transfer function is obtained by:

$$G(s) = \frac{\Delta I_s(s)}{\Delta D(s)} = \frac{1-D_o}{D_o}\frac{E_s}{L_{FBs}}\frac{1}{s}. \tag{25}$$

Figure 8 depicts the control architecture that can be used to control current $\langle i_s\rangle$. The $C(s)$ block is the controller and can be a proportional-integral type since the transfer function, $G(s)$, presents just one pole and no zeros.

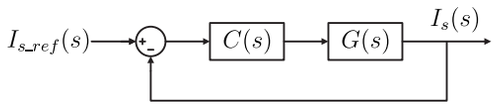

Fig. 8. Secondary current control diagram.

VI. EXPERIMENTAL RESULTS

A laboratory prototype with the specifications given in Table II was designed and built. The corresponding component parameters are given in Table III. Figure 9 shows the power stage diagram of the implemented prototype, with the inclusion of a semi regenerative clamping circuit used to limit the voltage spike across power semiconductors.

TABLE II
Laboratory Prototype Specifications

Parameter	Symbol	Value
Output Power	P_{con}	800 W
Primary Side Voltage	E_p	80 V
Secondary Side Voltage	E_s	160 V
Switching Frequency	f_s	50 kHz
Nominal duty cycle	-	0.5
Duty cycle range	-	0.45 to 0.55

TABLE III
List of Prototype Component Parameters

Component	Description
Secondary-primary turns ratio	$a = 2$
Flyback self-inductance	$L_{FBp} = 15.4\mu$H, $L_{FBs} = 60,54\mu$H,
Leakage inductances	$l_{FBp} = 138$ nH, $l_{FBs} = 550$ nH, $l_{PPp1} = 0.505\mu$H, $l_{PPp2} = 0.615\mu$H, $l_{PPs1} = 2.02\mu$H, $l_{PPs2} = 2.46\mu$H,
IGBT	S_{p1}, S_{p2}: IRGP50B60PD S_{s1}, S_{s2}: IRGP4PC30UD
Clamping circuit diodes	D_{gp1}, D_{gp2}, D_{gs1}, D_{gs2}: MUR160
Clamping circuit resistors	R_{gp}=10kΩ, R_{gs}=20kΩ
Clamping circuit capacitors	C_{gp}=470nF, C_{gs}=470nF

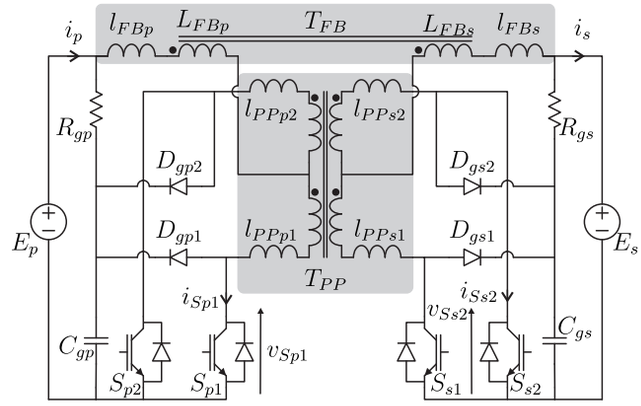

Fig. 9. Power stage diagram of the implemented laboratory prototype.

Figures 10 and 11 show the voltage and current waveforms of primary and secondary sources while the converter operates in $\text{Buck}_{\text{p}\to\text{s}}$ and $\text{Boost}_{\text{p}\to\text{s}}$ modes, respectively.

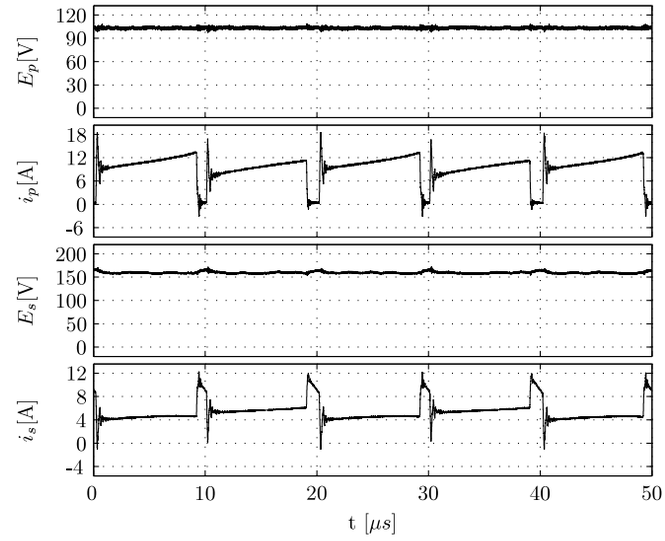

Fig. 10. Experimental voltages and currents waveforms of primary and secondary sources in $Buck_{p\to s}$ operation mode.

The secondary side source, E_s, was set to 160 V in both cases. The duty cycle was adjusted to 0.45 for the $\text{Buck}_{\text{p}\to\text{s}}$ mode case and 0.55 for the $\text{Boost}_{\text{p}\to\text{s}}$ mode case. The static gain experimentally obtained was 1.60 for $\text{Buck}_{\text{p}\to\text{s}}$ mode and 2.33 for $\text{Boost}_{\text{p}\to\text{s}}$ mode. According to (3), it was expected to be 1.64 and 2.44, respectively. These differences are caused by the power components losses that were not accounted in the analysis.

The expected normalized value of current $\bar{I}_{p[1]}$ was 0.219 for $\text{Buck}_{\text{p}\to\text{s}}$ mode and 0.179 for $\text{Boost}_{\text{p}\to\text{s}}$ mode. The experimental values were 0.238 and 0.180, respectively. The normalized current $\bar{I}_{s[1]}$ presented a similar behavior.

Figures 12 and 13 illustrate the voltage and current waveforms of T_{p1} and T_{s1} switches in the $\text{Buck}_{\text{p}\to\text{s}}$ and $\text{Boost}_{\text{p}\to\text{s}}$ mode, respectively. The clamping circuit limited the voltage across power semiconductors as expected. The current

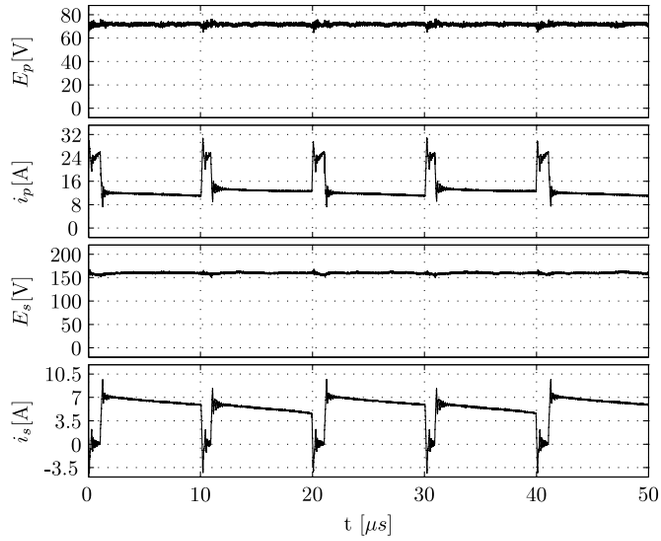

Fig. 11. Experimental voltages and currents waveforms of primary and secondary sources in $Boost_{p\rightarrow s}$ operation mode.

waveforms are very similar to those presented in Section II except for the non-idealities not accounted in the theoretical analysis.

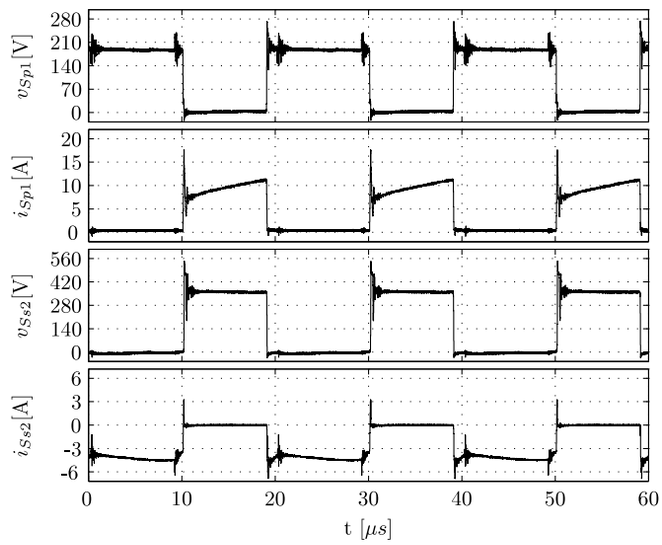

Fig. 12. Experimental waveforms of switches voltages and currents in $Buck_{p\rightarrow s}$ operation mode.

Figure 14 presents the efficiency curves for the $\text{Buck}_{\text{p}\rightarrow\text{s}}$, $\text{Boost}_{\text{p}\rightarrow\text{s}}$, $\text{Buck}_{\text{s}\rightarrow\text{p}}$ and $\text{Boost}_{\text{s}\rightarrow\text{p}}$ modes. The secondary voltage E_s was adjusted to 160 V in all tests, but the duty cycle was kept at 0.45 for the $\text{Buck}_{\text{p}\rightarrow\text{s}}$ and $\text{Boost}_{\text{s}\rightarrow\text{p}}$ operation modes, and 0.55 for the $\text{Boost}_{\text{p}\rightarrow\text{s}}$ and $\text{Buck}_{\text{s}\rightarrow\text{p}}$ operation modes. The maximum measured efficiency was 93.66 % and it occurred at 78 % of rated power in $\text{Buck}_{\text{p}\rightarrow\text{s}}$ operation mode.

A proportional-integral (PI) current controller, transfer function presented in (26), was designed and implemented in the laboratory prototype, with a phase margin, PM, of 70° and gain-crossover frequency, ω_c, of $2\pi 2000$ rad/s in order to verify the converter bi-directionality experimentally.

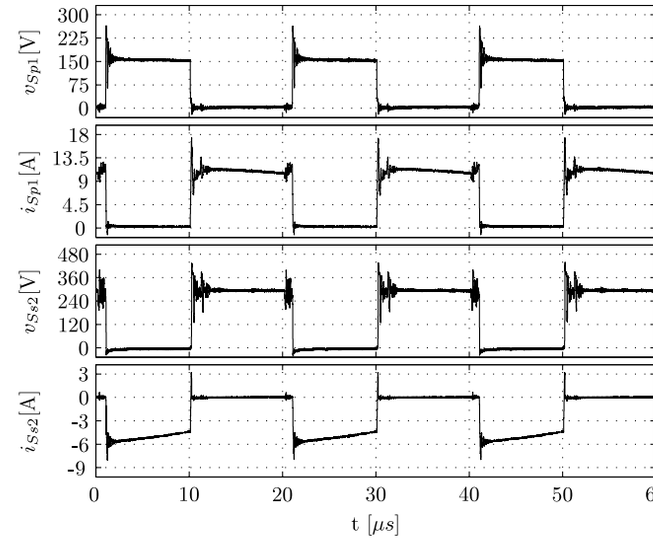

Fig. 13. Experimental waveforms of switches voltages and currents in $Boost_{p\rightarrow s}$ operation mode.

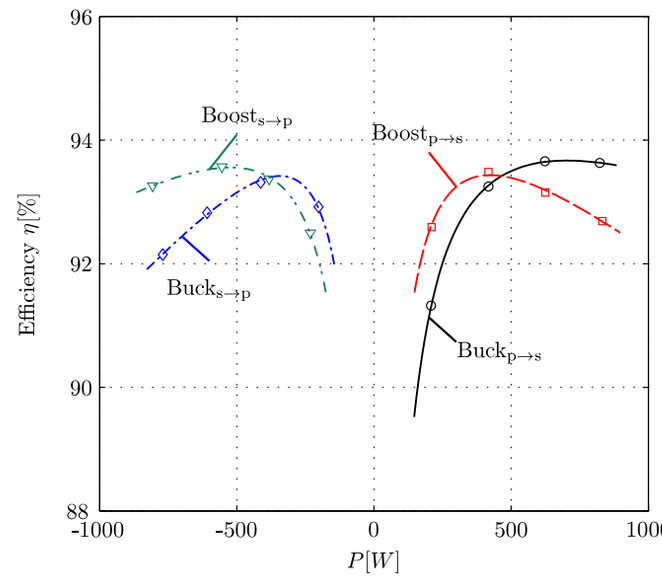

Fig. 14. Efficiency curves versus load power.

$$C(s) = K_{PI}\frac{s + Z_o}{s} \tag{26}$$

In first place, controller zero must be placed to establish the required phase margin at gain-crossover frequency. Its position is determined by (27).

$$Z_o = \frac{\omega_c}{tan(PM + 270° - \angle G(j\omega_c))} \tag{27}$$

$$Z_o = 2\pi 727[rad/s]$$

Secondly, the K_{PI}, determined by (28), is adjusted to $|C(s)G(s)|$ have a unitary gain for $s = j\omega_c$.

$$K_{PI} = \frac{L_{FBs}}{E_s} \frac{{\omega_c}^2}{\sqrt{{\omega_c}^2 + {Z_o}^2}} \tag{28}$$

$$K_{PI} = 4.549\text{x}10^{-3}$$

Figure 15 shows the current dynamic response, of the implemented converter, to a quasi-rectangular current reference, with amplitude of 5 A. According to the figure, power flows from 80 Vdc source to 160 Vdc source when the current is positive, and vice-versa. Therefore, the converter bidirectional power flow capability is fully demonstrated.

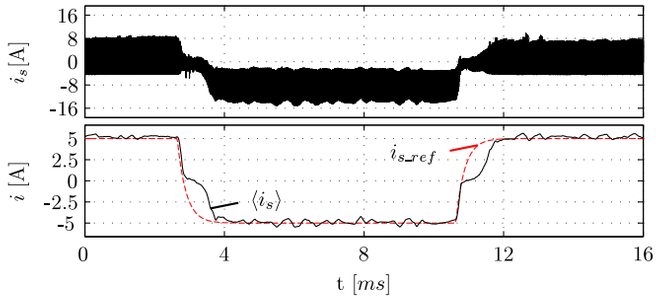

Fig. 15. Transient response of the converter to a quasi-rectangular current reference (i_{s_ref}), demonstrating the bidirectional power flow capability.

VII. CONCLUSION

The flyback push-pull bidirectional isolated dc-dc converter was addressed in this paper, with the intention to apply it in the control of the power flow between the sources of the dual low voltage systems. From the theoretical analysis and experimental studies conducted in the laboratory, it was possible to draw the following conclusions.

1. The experimental results agreed well with the results predicted in the analysis, both in steady state and transient operation;
2. Both the input and output current ripple, which are severe problems in low voltage and high current applications, are lower in comparison with the conventional isolated bidirectional dc-dc converters, such as the DAB family and conventional push-pull, full-bridge and half-bridge topologies;
3. The appropriate semi-regenerative clamping circuits can be used to protect the power semiconductors against over-voltages caused by the commutation and leakage inductances, instead of the complex clamping circuits, without sacrificing the converter efficiency;
4. The derived equations may be used to design a converter to comply with different specifications and applications.
5. As a fraction of the load power is processed by the flyback transformer, which has some offset current, more studies are necessary to compare the overall transformers size and volume, with pre-existing bidirectional topologies.

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