PROPOSAL OF A CONTROL ALGORITHM APPLIED TO A THREE-PHASE, FOUR WIRE, AC-DC CONVERTER FOR EV AND UPS APPLICATIONS

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Abstract – **This paper introduces a control algorithm for a multifunctional, three-phase, four-wire ac-dc converter. The converter is so-called multifunctional because it operates as a battery charger and as a load power supply. In other words, two different loads in parallel are simultaneously connected to the converter. The proposed algorithm can be applied to nonisolated three-phase UPS (uninterruptible power supply) systems, and electric vehicle (EV) battery charging systems. Relevant features of the proposed approach are power factor correction, common neutral point between the input and output facilitates the installation of the bypass circuit, balanced and symmetrical output voltages that allow the use of inverters with neutral point, and control of the battery current. The operation principle of the proposed algorithm is discussed in detail, while experimental results are also presented.**

Keywords - **Control Algorithm, Power Factor Correction, Rectifiers, Three-phase AC-DC Converter, Three-phase Battery Charger.**

I. INTRODUCTION

Power supplies based on three-phase rectifiers are typically employed in industrial applications, server farms, and EV chargers because the total current is distributed among the system phases, with the consequent reduction of the rms current that flows through cables if compared with single-phase systems [1], [2].

Computer loads can be supplied by the ac mains through the use of a three-phase ac–dc–ac converter [3], [4], thus drawing nearly sinusoidal currents with consequent high input power factor and maintaining regulated output voltages whose harmonic content is reduced [5]–[7]. For this purpose, the aforementioned arrangement must comprise two three-phase back-to-back converters with four-wire connection in order to supply several single-phase loads, thus providing simpler bypass structure. The output neutral must be connected to the mains neutral to simplify earth fault protection [8]. The work [9] proposes a battery charger for EVs through the use of a semi-controlled three-phase rectifier operating as pre-regulator with high power factor associated with a buck + boost converter, the latter has the purpose of controlling both charge and discharge the battery bank and the power delivered to the DC motor. In [10] the authors introduce a multiterminal set composed of drive / motor - generator that can act as the engine in drive mode and as an isolated transformer in charging mode, aiming to eliminate the charger while ensuring high power factor. In [11] a quick 50kW charger is presented by employing a three-phase six pulses rectifier associated to an active filter connected to three-phase power grid, using six groups of interleaved DC-DC converters, powered by the unregulated DC bus. The control of the DC-DC converter is accomplished through the Battery Management System. In [12] the authors proposed the use of three-phase motor as inductor during the charging phase, taking advantage of the existing connection on the central point of the star connection and employing the appropriate modulation to the common mode voltage of the inverter. In [13] an algorithm is proposed for an offline battery charger for electric vehicles based on state of charge of the battery estimator performed through obtaining the internal impedance of the battery, which in turn enables the transition between modes under constant load voltage or current, according to the charge status of the batteries. Many papers have been dedicated to the application of such converters to battery charging [10]-[15] and [16] while some techniques are based on the analysis of the state of charge (SOC), state of health (SOH), and improved control of floating voltage and charging current (i.e. Constant Current, Constant Voltage – CCCV). The integration of several functions performed by two or more converters in single stage approaches has also been analyzed aiming at achieving multifunctional characteristics.

The control schemes proposed in [17], [18] and [19] use a conventional sine-triangle pulse width modulation (CSPWM) scheme to generate the gating signals to drive the converter switches. The three sinusoidal reference voltages are compared with a common high-frequency triangular carrier. It is shown that such PWM scheme results in a peak-to-peak neutral current ripple greater than the peak-to-peak ripple in the line currents. A common important feature associated to three-phase rectifiers is power factor correction and the reduced voltage stress across the active semiconductors, which can be achieved by using suitable topologies and control techniques. The analysis, design, and control of a three-leg converter with split dc link was studied in [8]-[21], where the proposed control and modulation structures and strategies are supposed to reduce the harmonic content of the currents drawn from the ac mains. The approaches include PWM (pulse width modulation) [18], vector control [20], space vector modulation [22], hysteresis in current mode

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control [23], average current mode control and peak current mode control. The control of three-phase four-wire rectifiers is based on two characteristics: regulation of the dc output voltage when supplying balanced or unbalanced loads [24]-[27] while maintaining the total harmonic distortion (THD) of the input currents as low as possible, with consequent high input power factor. According to the Brazilian Standard NBR 15014 (2003) [30], UPSs are classified into three main categories: on-line or double conversion, where the load is continuously supplied by the rectifier and inverter, thus performing dual power conversion (ac-to-dc and dc-to-ac); line interactive; and off-line or stand-by. Figures 1(a) to (c) show the topologies defined according to the aforementioned standard, while all of them demand the use of a separate battery charger based on an isolated or nonisolated converter.
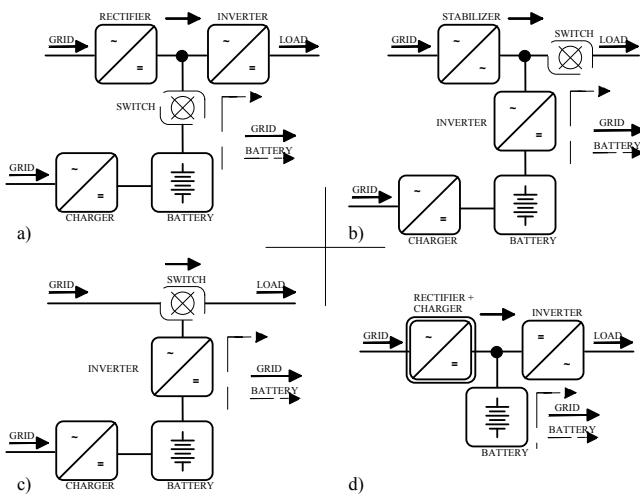

Fig. 1. Definition of UPS systems according to Brazilian standard NBR 15014 (2003): (a) Double conversion UPS system; (b) Line interactive UPS; (c) Standby UPS; (d) Proposed definition for a novel the double conversion UPS system.

Within this context, this paper proposes a modification to the conventional method for power factor correction so that the use of a battery charger is not necessary. Besides, constant charging current (Constant Current) and output voltage regulation for the rectifier stage (Constant Voltage) are achieved while still ensuring the high power factor. The novel system is defined in Figure 1(d), where the battery charger and the rectifier integrate a single stage. The four-wire connection simplifies bypassing, thus allowing supplying single-phase loads.

This paper presents the analysis, design, and control of a three-leg converter with split dc link, which can be four-wire front-end converter in three-phase transformerless line conditioners and UPS applications, so as a battery charger for EVs. It also expands the work [28], with improved theoretical and experimental results, better algorithm and dynamical analysis and higher converter power rating.

II. MULTIFUNCTIONAL CONVERTER

The concept shown in Figure 2 presents a two-level bidirectional rectifier operating as an ac-dc stage, with batteries connected indirectly to the dc link through thyristors. However, efficiency is compromised in the battery powered mode and two separated battery banks are necessary due to the different reference connections in the output side. In this case, two separated battery chargers are used. Such additional charging stage increases overall cost, and reduces efficiency if compared to the concept depicted in Figure 3(a).
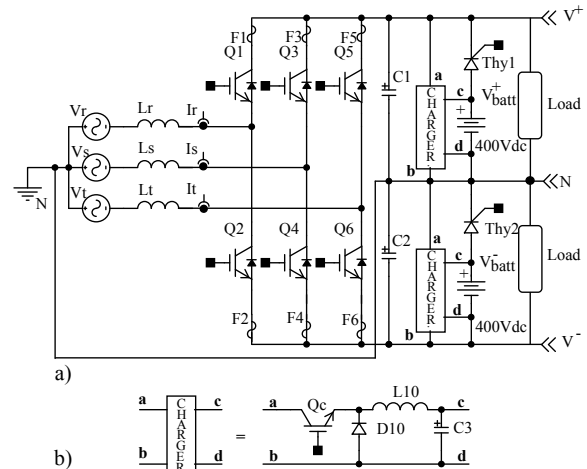

Fig. 2. (a) Two level, three-phase rectifier with four-wire connection associated to (b) buck battery charger with the main protection circuits necessary for safe operation [28].

The concept proposed in Figure 3(a) presents the advantage of requiring only two battery banks. The removal of the charger increases the efficiency due to the reduced number of power processing devices that operates in the battery charging mode. Besides, the three-phase four-wire block can be replaced by any kind of converter i.e. even multilevel converters with proper circuit modifications. However, in this case, the battery bank is not isolated from the load and the ac mains, which is a possible drawback when a fault occurs in the power stage semiconductors, and as a result a dc voltage is applied to the load.
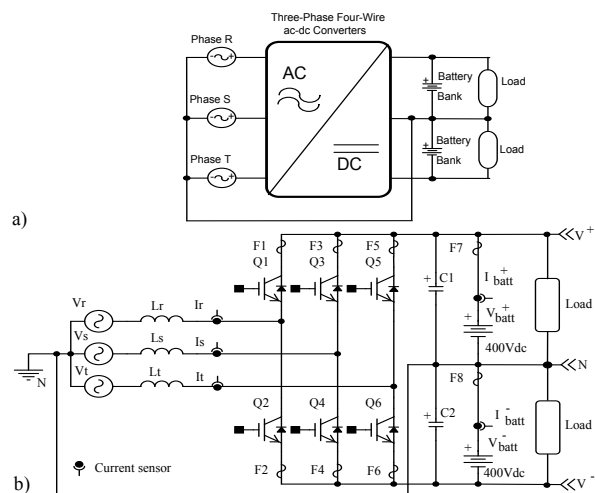

Fig. 3. (a) Simplified block diagram of a multifunctional three-phase four-wire ac-dc converter supplying two loads simultaneously; (b) Proposed multifunctional two-level three-phase rectifier with four-wire connection and without the presence of battery chargers, associated to the main protection circuits necessary for safe operation [28].

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Besides, additional battery charging modes and better battery decoupling between the dc link and load can be achieved. The main advantage of the concept presented in Figure 3(a) is simple connection, reduced number of semiconductors, and reduced number of power processing stages if compared to the concept presented in Figure 1(a) and Figure 2.

By comparing both topologies, it can be stated that the first block diagram shown in Figure 3(a) corresponds to Figure 3(b), which presents prominent advantages.

The four-wire controlled rectifier in Figure 3 allows the simplification of bypass operation and connection of unbalanced loads to the dc link. Besides, there is the possibility to supply three-phase inverters with neutral point, as it is necessary to control the output voltages for different load conditions.

III. CONTROL STRATEGY

Once the batteries are configured as shown in Figure 3(b), the use of additional protections for IGBT (insulated gate bipolar transistor) modules and batteries of the dc link is mandatory to avoid damage to the mains and the UPS system if a fault occurs during inappropriate triggering of the switches.

A classical approach proposed for controlling the three-phase rectifier is shown in Figure 4, whose elements are: $C_I(s)$ – current loop controller per phase; V_{sum} – sample of the total voltage across the dc link; $C_V(s)$ – voltage loop controller; V_{diff} - sample of the differential voltage across the dc link; $C_d(s)$ – differential voltage loop controller. This strategy usually employs PI (proportional-integral), P+Ressonant (proportional+ressonant, for the $C_I(s)$ current controller) or PID (proportional-integral-derivative) controllers, whose main characteristics are reduced computational effort and well-established tuning strategies reported in technical literature.
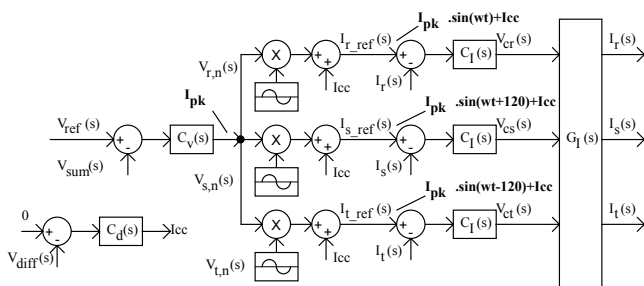

Fig. 4. Classical control method applied to power factor correction in three-phase rectifiers.

A modification of the classical control strategy used in three-phase rectifiers is presented in Figure 5, where three loops are responsible for the regulation of the dc link voltage and control of the currents through the battery banks by using a proper switch to multiply the control signals of the current controllers by the total output voltage sample.
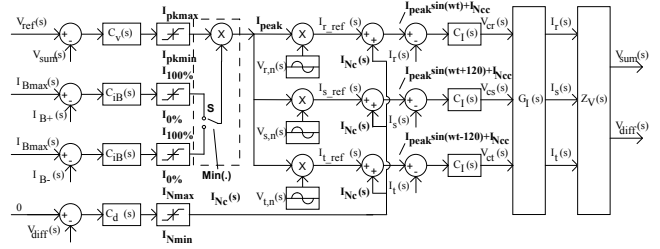

Fig. 5. Proposed block diagram of the control algorithm for the three-phase four-wire rectifier, where the control loops monitors the input current, the current through the battery and the voltage across each battery.

The transition between the charging battery current regulation and the total bus voltage regulation loops occurs by employing a minimum priority value selector given by switch S and the first multiplication stage. This selector uses the lowest value of the controller's outputs $C_{iB}(s)$, ensuring that none of the battery banks receive more than that was established by I_{Bmax} charging current reference. The lowest controller output value is then multiplied by the output of the total bus voltage controller. This will limit the peak value of sinusoidal current reference of the rectifier.

Once obtained the peak values of the current that will flow through the grid, the current references for each phase are calculated using the product between the peak value and the sinusoidal reference of each phase. An internal controller calculates the neutral current that the rectifier should impose to the grid. This will ensure that there will be no imbalance in the bus voltages.

IV. MATHEMATICAL MODELS

Figure 6 and Figure 7 shows the main circuit and waveforms, respectively, during some switching periods for the single-phase representation of the two-level converter. This representation is valid considering that the angular grid frequency ω_{grid} is typically much lower than the angular switching frequency ω_s, so that the grid voltage is constant in a switching period.

A. Single-Phase Time Domain Analysis

In order to perform the time domain analysis, ideal switches and capacitors are considered, and the converter operates in continuous conduction mode, as the current through the inductor does not become null during the entire switching period.

The nomenclature used for analysis of the rectifier shown in Figure 6 and waveforms in Figure 7, considers that the variables are divided into three categories: quiescent or DC units, average values over one switching period, which combine both quiescent and small-signal units, and small-signal variables i.e.

• $V_{\{r,s,t\}}$, E^+_{batt}, E^-_{batt} and V_{cN} are quiescent grid voltages (whose frequency is much smaller than switching frequency, so that it can be considered a quiescent point), internal battery voltages, and the quiescent voltage imposed by the converter with respect to the neutral point, respectively;

• Some equations need the following assumption: $r_b = 0$ and $r_c = 0$. This will imply that $V^+ = E^+_{batt}$, $V^- = -E^-_{batt}$, which are DC link voltages, whose values are referred to the internal battery voltages. Also, $V^+ > 0V$, and $V^- < 0V$.

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- $I_{\{r,s,t\}}$, I^+_{batt}, I^-_{batt}, I^+_{load}, and I^-_{load}, are quiescent currents through the phases, batteries and load, respectively;
- $D_{\{r,s,t\}}$ and $D'_{\{r,s,t\}}$ are quiescent duty cycles and their corresponding complementary values, respectively;
- $v_{\{r,s,t\},N}(t)$, $v_{cN}(t)$, $e^+_{batt}(t)$, $e^-_{batt}(t)$, $v^+(t)$, and $v^-(t)$ are instantaneous grid phase voltages, the voltage imposed by any phase of the converter, instantaneous battery voltages, and dc link voltages, respectively.
- $i_{r,s,t}(t)$, $i^+_{batt}(t)$, $i^-_{batt}(t)$, $i^+_{load}(t)$, and $i^-_{load}(t)$, are instantaneous grid currents, instantaneous battery currents, and instantaneous load currents, respectively.
- $d_{\{r,s,t\}}(t)$ and $d'_{\{r,s,t\}}(t)$, are the instantaneous duty cycles and their corresponding complementary values, respectively;
- It is assumed that the magnitudes of the quiescent quantities are much higher than the small-signal ones e.g. $\left|\hat{d}_{\{r,s,t\}}(t)\right| \ll \left|D_{\{r,s,t\}}\right|$, $\left|\hat{v}_{\{r,s,t\},N}(t)\right| \ll \left|V_{\{r,s,t\},N}\right|$ and $\left|\hat{i}_{\{r,s,t\}}(t)\right| \ll \left|I_{\{r,s,t\}}\right|$.
- The small-signal variables are described by circumflex sign e.g. $\hat{d}_{\{r,s,t\},N}(t)$ corresponds to a small-signal disturbance in the duty cycle of each phase;
- The instantaneous average value of any variable is described by the relationship: $\langle x(t) \rangle_{T_s} = \frac{1}{T_s}\int_{t}^{t+T_s} x(\tau)d\tau = X + \hat{x}(t)$, which incorporates both quiescent values and small-signal variations;

Let us consider that i_a, i_p, and i_c are the average currents through the active, passive, and common terminals, respectively, as shown in Figure 6. This assumption allows the analysis of the switch model.
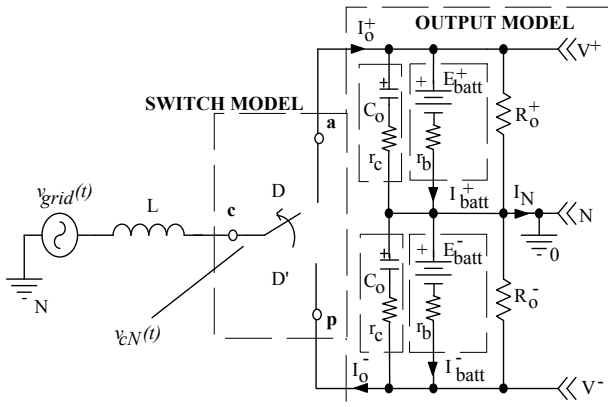

Fig. 6. Single-phase two-level converter: Ideal switch model.

The average switch voltage over one switching period is:

$$\langle v_{cN}(t) \rangle_{Ts} = \frac{1}{T_s}\int_{t}^{t+T_s} v_{cN}(\tau)d\tau$$
$$\cong d_x(t)\langle v^+(t) \rangle_{T_s} + d'_x(t)\langle v^-(t) \rangle_{T_s}. \tag{1}$$

By expanding (1), linearizing it by applying a Taylor series expansion and removing the nonlinear second-order ac terms, the small-signal equivalent value of the switch voltage becomes:

$$\hat{v}_{cN}(t) = \hat{d}_x(t)V^+ + \hat{d}'_x(t)V^- + D_x\hat{v}^+(t) + D'_x\hat{v}^-(t)$$
$$\approx \hat{d}_x(t)V^+ + \hat{d}'_x(t)V^-. \tag{2}$$

The expression (2) describes the voltage across the averaged switch model, which depends on the voltage of each dc link, duty cycle and its corresponding complement considering that the converter operates in CCM. Note that the small signal variation on the bus voltages in (2) can be removed – this procedure can be done if the small ac variations on the positive and the negative bus voltages are symmetric or non-existent, which will lead to a simpler but accurate model. According to Figure 8, it looks like a controlled voltage source.
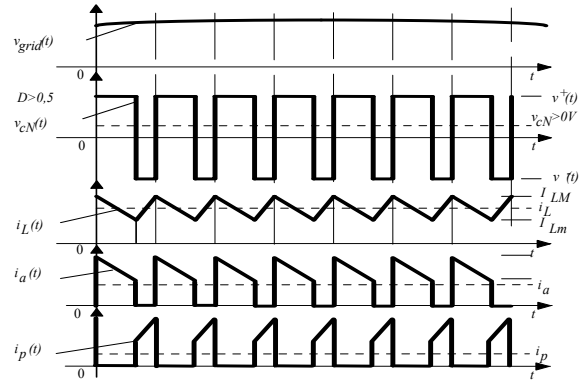

Fig. 7. Single-phase two-level converter main waveforms, assuming $v_{grid} > 0V$.

The same procedure can be carried out to determine the currents through the active switch terminal (I_a) and passive switch terminal (I_p) i.e.:

$$\langle i_a(t) \rangle_{Ts} = \frac{1}{T_s}\int_{t}^{t+T_s} i_a(\tau)d\tau \cong d_x(t)\langle i_c(t) \rangle_{T_s} \tag{3}$$

$$\langle i_p(t) \rangle_{Ts} = \frac{1}{T_s}\int_{t}^{t+T_s} i_p(\tau)d\tau \cong d'_x(t)\langle i_c(t) \rangle_{T_s}. \tag{4}$$

By expanding (3) and (4), linearizing them, and removing the nonlinear second order ac terms, the small-signal equivalent values of the currents through each switch terminal are:

$$\hat{i}_a(t) = \hat{d}_x(t)I_c + D_x\hat{i}_c(t) \approx \hat{d}_x(t)I_c \tag{5}$$

$$\hat{i}_p(t) = \hat{d}'_x(t)I_c + D'_x\hat{i}_c(t) \approx [1 - \hat{d}_x(t)]I_c. \tag{6}$$

Expressions (5) and (6) show that the current flowing through the common switch terminal is distributed through active and passive terminals, which depend on the duty-cycle and its complement. Such averaged representation is analogous to a controlled current source as shown in Fig 8.

B. Single-Phase Averaged Switch Model

An averaged model of the converter is analyzed as proposed in [2]. Such analysis yields the instantaneous averaged value electrical model for a single phase converter, as shown in Figure 8.
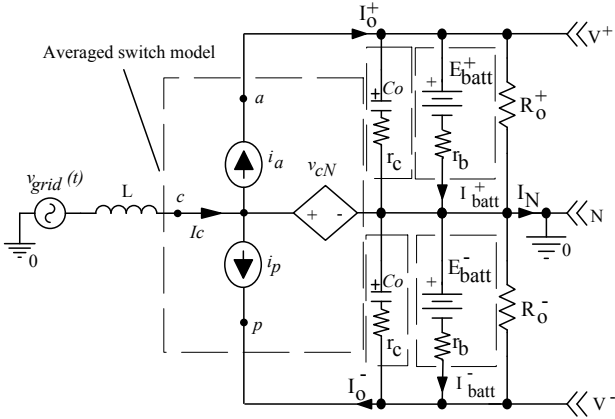
Fig 8. Averaged single-phase model for the two-level converter operating in CCM.

Using the derived switch model in Figure 8, the currents through the active terminal (I_a) and passive terminal (I_p) ports, necessarily depend on the current flowing through the common terminal (I_c) whose value is equal to that flowing through inductor L and obtained from:

$$L\frac{d\langle i_L(t)\rangle_{T_s}}{dt} = v_{grid}(t) - \langle v_{cN}(t)\rangle_{Ts} =$$
$$v_{grid}(t) - \left[d_x(t)\langle v^+(t)\rangle_{T_s} + d'_x(t)\langle v^-(t)\rangle_{T_s}\right]. \quad (7)$$

The currents through the active (I_a) and passive (I_p) terminals can be partially divided between the load and the battery, so that a current controller can monitor battery charging also providing regulation of the dc voltage with a proper control strategy.

C. Three-Phase Model

Figure 9 shows the complete model of the three-phase rectifier, considering the instantaneous average values in the PWM switch model, while the batteries are represented as dc voltage sources and the load is not connected to the dc link [27]. The static single-phase model is extended to a three-phase version as presented by (8) and (9).

In steady-state condition, the variation of the current expression, (9) is supposed to be null, otherwise the current through the inductor tends to increase indefinitely. The current controller imposes small variations to the phase duty cycle, resulting in successive increments of the integral term, thus enabling the proper shaping of current through each phase.

$$v_{cN,\{r,s,t\}}(t) = \hat{d}_{\{r,s,t\}}(t)V^+ + \hat{d}'_{\{r,s,t\}}(t)V^- \quad (8)$$

$$L\frac{d\langle i_{L\{r,s,t\}}(t)\rangle_{T_s}}{dt} = v_{\{r,s,t\},N}(t) - \langle v_{cN,\{r,s,t\}}(t)\rangle_{Ts} = \quad (9)$$
$$v_{\{r,s,t\},N}(t) - \left[\hat{d}_{\{r,s,t\}}(t)V^+ + \hat{d}'_{\{r,s,t\}}(t)V^-\right].$$

The rectifier output power delivered to both load and battery is expressed in terms of the efficiency η so that:

$$P_{in} = \frac{3}{2}V_{Pk}I_{Pk} \therefore V_{sum}(t)I_o(t) = \eta P_{in}(t). \quad (10)$$

In steady-state condition, considering that slowly variant peak grid currents imposed by current and bus voltage controllers exist, the rectifier input power is:

$$P_{in}(t) = \frac{3}{2}V_{Pk}I_{Pk}(t). \quad (11)$$

It is possible to demonstrate that the total output current ($I_o(t)$) in the rectifier corresponds to the sum of the load ($I_{load}(t)$) and battery ($I_{batt}(t)$) currents, which are related to the grid peak current as:

$$I_o(t) = I_{batt}(t) + I_{load}(t) = \eta\frac{3}{2}\frac{V_{Pk}}{V_{sum}}I_{Pk}(t). \quad (12)$$

In steady-state condition, the average currents through the DC link capacitors are zero, so the expression (12) can be simplified.

The current through the batteries ($I_{batt}(t)$) is the sum of the average current available from each rectifier stage minus the current delivered to the load ($I_{load}(t)$), which is also given in (12). Considering the balance of energy absorbed from the grid and delivered to the load and battery, it is possible to demonstrate that $I_o(t)$ in (10) can be obtained from the relationship between the peak value of the time-variant mains current $I_{Pk}(t)$ (whose value is adjusted by the voltage loop controller), the mains peak voltage $V_{Pk}(t)$, (which is also a time-variant quantity), and the sum of dc link voltages $V_{sum}(t)$.
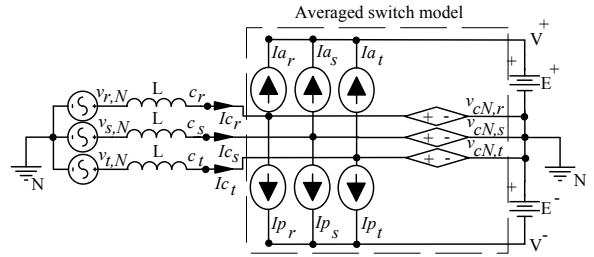

Fig. 9. Three-phase simplified model for CCM operation considering the complete model of the rectifier, where the load was removed for simplicity.

A change is proposed to the classic power factor correction controller (Figure 5), so that the current flowing through the load and battery is controlled by changing the peak current drawn from the grid with the appropriate shape, thus ensuring high input power factor and low THD.

The proposed controller employs the following loops:
• three current loops for phases r, s, and t to impose sinusoidal shape to the input currents;
• a differential voltage loop to ensure the balance between the dc link voltages V^+ and V^-;
• a voltage loop to ensure proper regulation of voltages V^+ and V^-;
• a current loop to allow controlling the charging currents of the batteries connected to the positive and negative dc links.

This methodology can be extended to single-phase systems and can be used with DQ reference frame or P+Resonant based controllers to improve error-free tracking associated to the grid current controller.

D. Single-Phase Dynamic Model

By analyzing the large signal model shown in Figure 8, the main transfer functions that allow controlling and performing the stability analysis of the converter is obtained from expressions (13) to (20). The transfer function of the current through the inductor to the duty cycle is presented in (13). Such expression is necessary for the proper design of current loop controller.

$$
\begin{aligned}
G_{iLd}(s) &= \frac{\hat{i}_L}{\hat{d}} = \\
&-\frac{R_o}{r_{eq} + R_o} \frac{V^+ - V^-}{sL + \left(D'_{static} - D_{static} \right)\left(r_{eq} \parallel R_o \right)}.
\end{aligned}
\tag{13}
$$

It is worth to mention that parameter r_{eq} corresponds to the equivalent series resistance of the battery (r_b) in parallel with the capacitor equivalent series resistance (r_{se}).

Expressions (14) and (15) correspond to the transfer function of the output voltage to the inductor current, which is essential to design properly the dc link voltage loop controller.

$$
Z_{v^+ - i_L}(s)\Big|_{\substack{v^- = 0 \\ d = 0}} = \frac{\hat{v}^+}{\hat{i}_L} = \frac{sL}{D_{static}} + R_o \frac{D_{static}}{1 + sR_oC_o}
\tag{14}
$$

$$
Z_{v^- - i_L}(s)\Big|_{\substack{v^+ = 0 \\ d = 0}} = \frac{\hat{v}^-}{\hat{i}_L} = -\frac{sL}{D'_{static}} - R_o \frac{D'_{static} + 1}{1 + sR_oC_o}.
\tag{15}
$$

E. Converter Output Dynamic Model

Let us consider the output power stage shown in Figure 6, so that the decomposition of currents I_o^+ and I_o^- can be described by the expressions (16) to (18).

$$
I_o^+(t) = I_o^-(t) + I_N(t)
\tag{16}
$$

$$
I_o^+(t) = I_{Co}^+(t) + I_{Ro}^+(t) = C_o \frac{dV^+(t)}{dt} + \frac{V^+(t)}{R_o}
\tag{17}
$$

$$
I_o^-(t) = I_{Co}^-(t) + I_{Ro}^-(t) = C_o \frac{dV^-(t)}{dt} - \frac{V^-(t)}{R_o}.
\tag{18}
$$

By applying the Laplace transform, it is possible to obtain the transfer function that relates such currents and voltages in (19) and (20). Thus, it is possible to obtain expressions for the dynamic differential voltages, and the total voltage across the dc link do that it is possible to design properly the controllers considering expressions (19) and (20).

$$
G_{diff}(s) = \frac{\hat{v}_{diff}}{\hat{i}_N} = \frac{R_o}{1 + sC_oR_o}
\tag{19}
$$

$$
G_{sum}(s) = \frac{\hat{v}_{sum}}{\hat{i}_{Pk}} = \eta \frac{3V_{Pk}}{V_{sum}} \frac{R_o}{1 + sR_oC_o}.
\tag{20}
$$

It should be noted that the removal of the battery current from (16) is mandatory, as the converter should be able to operate under stable conditions even if the battery is disconnected from the DC bus.

V. EXPERIMENTAL RESULTS

In order to validate the theoretical assumptions, an experimental prototype was designed and implemented according to the procedure developed in Section II.

Table I shows the parameters used to tune the controllers employed in the experimental prototype, so that it is possible to verify the performance of the proposed technique. Table II shows specifications for the power stage of the experimental prototype.

TABLE I
Specifications of the Controllers Used in the Experimental Prototype.

Voltage and current controller specifications at f_{sample}=20 kSPS F_C: Crossover frequency, PM: Phase Margin			
Controller	Desired	Controller gains	Remarks
Line current controller	F_C=2 kHz	K_p=0.5, K_i=0.2, T_i=0.25 ms	One PID controller for each grid current
	PM>45°	K_d=0.2, T_d=0.01 ms	
Total dc link voltage controller	F_C=20 Hz	K_p=0.7, K_i=0.05, T_i=5.0 ms	One PID controller
	PM>60°	Kd = 0.125, T_d=6.25 μs	
Differential dc link voltage controller	F_C=60 Hz	K_p=0.4, K_i=0.3, T_i=166.66 μs	One PID controller
	PM>60°	K_d=0.125, T_d=6.25 μs	
Battery current controller	F_C=10 Hz	K_p=0.1, K_i=0.04, T_i=1.250 ms	One PID controller for each battery
	PM>60°	K_d=0.125, T_d=6.25 μs	

TABLE II
Specification of the Power Stage Elements

Main Components of the Ac-dc Converter			
Component	Specification	Description	Remarks
$L_{r,s,t}$	5.5 mH	Input inductances	Maximum current: 10 A$_{rms}$
$S_{1,2,3,4,5,6}$	1200V / 10A	IGBTs + drivers	—
$C_{1,2}$	Capacitors by Epcos	6×2200 μF / 450V connected to each dc link	—
$Batt_{1,2}$	Lead acid battery rated at 12V, 7Ah	32 series-connected batteries for each dc link	—
$R_{1,2}$	Load resistance	106 Ω/1500W for each dc link	

The input phase voltage of the prototype can vary from 200V$_{rms}$ to 265V$_{rms}$. The rated total output power is 3 kW (1.5kW for each DC bus), with an output voltage of ±400 V, employing 32+32 series-connected batteries at 12 V, 7Ah, each.

The frequency response of the open loop grid current controller − $C_i(s)$, associated to the plant transfer function $G_{iLd}(s)$ is shown in Figure 10: *FTLAcc(s)* − Grid Currents. Figure 10 also shows the open loop frequency response for total and differential DC link voltages, each associated with their respective controllers: $C_v(s)$ with $G_{sum}(s)$ becoming the *FTLAcc(s)* − Total *VBus*, or V_{sum}; $C_d(s)$ with $G_{diff}(s)$, which becomes the *FTLAcc(s)* − Differential *VBus*, or V_{diff}. All frequency response curves are based on the parameters given in Table I and Table II.

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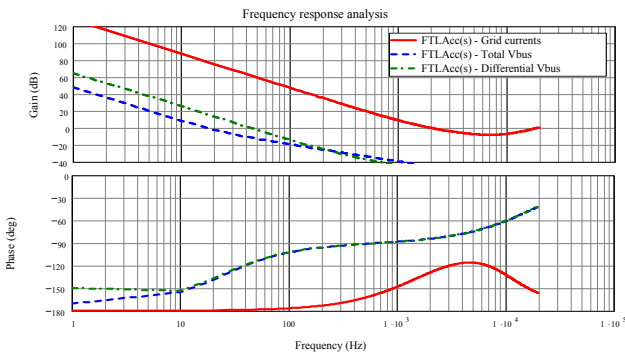Eletrôn. Potên., Campo Grande, v. 20, n. 3, p. 263-271, jun./ago. 2015

Fig. 10. Open loop frequency response for the employed controllers.

Figure 11 shows the experimental setup for the proposed rectifier, wich employs a dsPIC© (digital signal peripheral interface controller) based controller to implement the proposed algorithm. Experimental results on the prototype are given in Figure 12 to 15, and a detailed analysis is presented as follows.
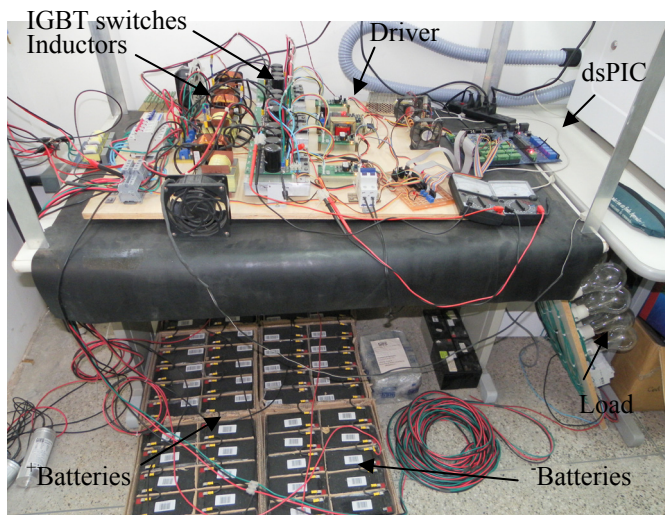

Fig. 11. Complete view of the 3-kW experimental prototype.

Figure 12 shows the experimental results for both dc links at rated load condition. It can be seen that the voltages are balanced and regulated at 400 V. The grid currents are shown in Figure 13, where the input power factor is 0.99 and the phase currents THD is 5.0% at rated load, measured with power analyser MEGABRÁS MAR-715L. It is also worth to mention that the aforementioned waveforms were acquired when using balanced loads and charged batteries.
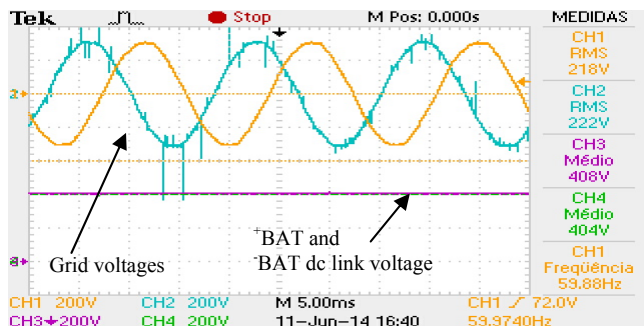

Fig. 12. Voltages across phase r and s, positive and negative dc link voltages.
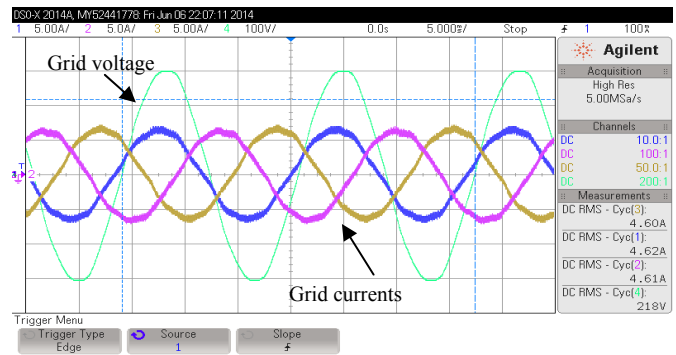

Fig. 13. Grid voltage across a single phase and current through phases r, s, and t.

The upper trace in Figure 14 shows a grid fault during about eight seconds. To verify the battery current comportment, when grid voltage is reconnected, a detail of one second is shown in the same figure. During the discharging mode, a positive current of 3.5A flows through the battery. When the grid is restored, the average current through the positive battery bank is limited to about 500 mA to restore battery charge.

Figure 15 shows some results when unbalaced loads are connected to the dc links. The upper trace shows four distinct negative and positive load steps in order to verify stability.
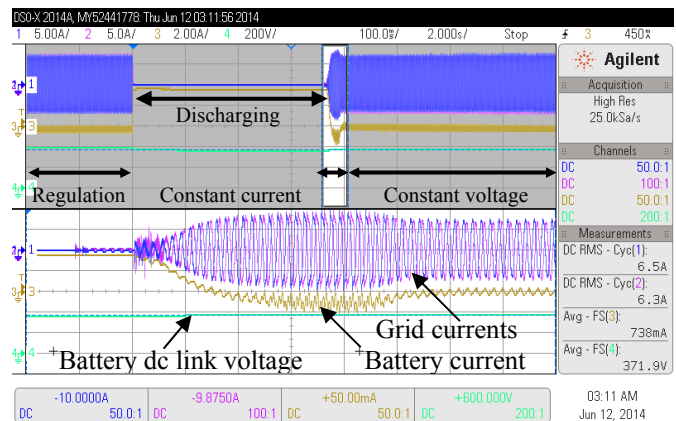

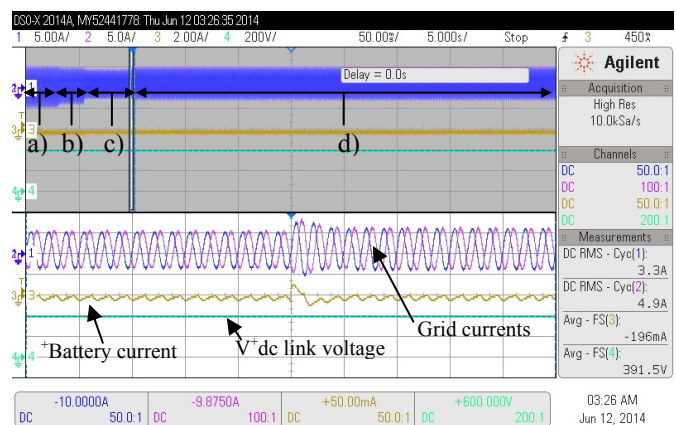Fig. 14. Transient response of the three-phase rectifier during a grid fault.

Fig. 15. Experimental results for the proposed control algorithm under unbalanced load condition.

The detailed view of the transient behavior is presented in the bottom waveforms, where the loads connected to the

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positive and negative dc links vary according to the following pattern: a) rated load, 50%+50%, b) 50%+40%, c) 40%+20%, and d) 50%+20%. According to Figures 13, 14, and 15, the proposed algorithm allows adequate voltage regulation across both dc links even under unbalanced load conditions, also ensuring high input power factor i.e. close to unity while keeping the CCCV charging mode for both battery banks. In order to improve the performance of the currents through the batteries, the use of small LC (inductor-capacitor) filters is suggested, which must be properly tuned to reduce the output current ripple.

VI. CONCLUSION

This paper has proposed an algorithm to control a two-level three-phase rectifier, which can be easily extended to other three-phase rectifier topologies aiming at the removal of the battery charger stage and incorporating its functionality to the control loops. The present study expands the work [28], with improved theoretical and experimental results, better algorithm and dynamical analysis, higher converter power rating, showing the feasibility of the proposed control algorithm for charging batteries without a separate charger. Such algorithm ensures the main features associated of the operation of a three-phase rectifier i.e.:

• High input power factor even during battery charging;

• Battery is charged in rated load and no load condition even when the RMS grid voltage varies;

• Battery is charged by limiting the average current through them;

• Symmetrical voltages across the dc links even under unbalanced loads are guaranteed;

• The total output voltage is regulated through the use of a proper control loop;

• The absorbed power is fixed by limiting the current drawn from the grid in order to protect the power semiconductors.

A 3-kW prototype has been built to validate the proposed control algorithm, which was implemented by using digital control in a dsPIC© microprocessor. This strategy can be incorporated to medium and large-scale UPS systems, also in on-board EVs to charge batteries, due to its simplicity and low cost if compared to traditional configurations.

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