

MULTI-STATE AND INTERLEAVED CONVERTERS WITH PASSIVE IMPEDANCES FOR CURRENT SHARING

René P. T. Bascopé¹, Grover V. T. Bascopé², Francisco J. B. Brito Jr.¹, Sérgio Daher¹

¹Energy Processing and Control Group (GPEC), Electrical Engineering Department, Federal University of Ceará
Fortaleza - CE - Brazil

²Department of Research and Development, GTB Power Electronics R&T AB
Sibeliusingen, Kista - Sweden

e-mails: {rene, britojr, sdaher}@dee.ufc.br, grover.torrico@gmail.com

Abstract - This paper presents multilevel switching cells that allow the generation of high-power nonisolated dc-dc, ac-dc, dc-ac, and ac-ac converters. The cells are classified in two groups: multi-state switching cells based on autotransformer and interleaved switching cells based on inductors. Each switching cell has an impedance based on a small inductor connected between the legs, which is named current sharing circuit and guarantees zero average voltage across the involved magnetic components, therefore compensating eventual differences between the pulse width modulation duty cycles. The inductor should be small because it causes the duty cycle reduction. In order to verify the current sharing between the magnetic components, two dc-dc buck converters operating at 25 kHz and rated at 1 kW, where the input voltage is 200 V and the output voltage is 60 V, are implemented and evaluated in laboratory.

Keywords – Current Sharing, Interleaving Technique, Multi-State Switching Cell, Passive Impedance.

I. INTRODUCTION

Applications such as electric motor drives, renewable energy conversion systems, power transmission systems, solid-state transformers (SSTs), electric vehicle battery chargers, among others, typically involve high power levels. Considering that the use of classic converters is limited by the power levels that can be processed, technical literature presents some techniques that can overcome such restriction. Parallelism of semiconductors, interleaved converters, multi-state switching cells, and multilevel converter topologies have been introduced as possible solutions. The first three aforementioned techniques may lead to current unbalance when duty cycle variations occur, as presented in [1].

In order to achieve current sharing through the components in parallel converters, a given balancing strategy based on passive or active techniques may be adopted. Among the passive strategies, there are two popular approaches found in literature. The first one consists in coupling the magnetic components, where the interaction between them occurs through the energy stored in the mutual inductance [2]-[8]. The second one consists in the converter operation in discontinuous current mode (DCM) [9],[10] or critical/boundary conduction

mode (CRM) [11]-[13] in order to avoid the saturation of magnetic components. In [14] the virtual vectors concept is used to ensure equal current sharing between adjacent legs, thus avoiding saturation of the coupled inductors.

An active balancing strategy has also been proposed in literature [15]-[21], which is based on the implementation of a current control loop to balance the current through the parallel components. An active technique based on droop method was proposed to achieve current sharing in the paralleled converters [22]. A control strategy for the parallel operation of inverters ensuring the proper sharing of the load current was presented in [23]. The influence of the current balancing between commutation cells of a same phase is investigated in [24], while an active solution is proposed to minimize the current imbalance in parallel inverters.

A simple and effective current sharing circuit using inductors has been successfully applied to balance the current through paralleled switches operating with the same pulse-width modulation (PWM) signals [25]-[27].

Within this context, this paper proposes the addition of current sharing circuits formed by impedances, where inductors are firstly used in multi-state and interleaving switching cells to avoid the current unbalancing caused by differences between PWM signals of the switches. Such topologies present some displacement among the PWM signals according to the number of involved legs, so that the converter aggregates new operation features. Multi-state and multilevel cells used in the generation of high-power nonisolated converters are also introduced. The detailed description of the current sharing circuit including a theoretical analysis and experimental results are properly presented and discussed.

II. APPLICATION OF THE CURRENT SHARING CIRCUIT

The multi-state switching cells (MSSC) based on autotransformer and the interleaved switching cells (ISC) based on non-coupled or coupled inductors have an impedance based on a small inductor L_{sh} , which is connected between the legs, named current sharing circuit (CSC), which guarantees zero average voltage across the involved magnetic components. Therefore, it is possible to minimize eventual differences between the PWM duty cycles. Since the inductor should be small because it causes the duty cycle reduction. By applying the proposed current sharing circuit, twelve multi-state and interleaved cells can be obtained, which are divided in two sub-groups: I-Type and T-Type cells. The resulting cells with idealized switches are shown in Figure 1. They are based

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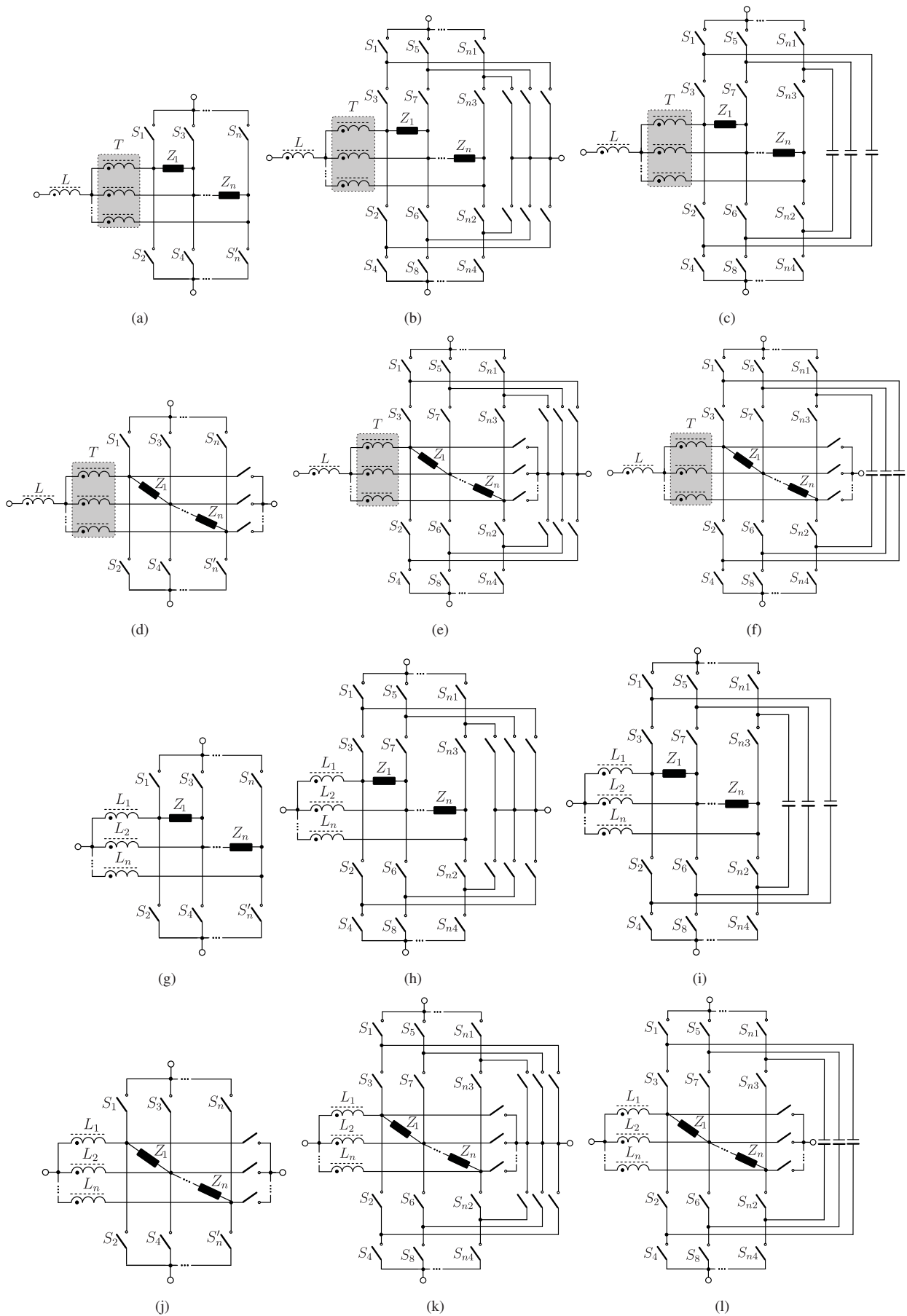


Fig. 1. Multi-state switching cells (MSSC): I-type cells [(a) general, (b) NPC and (c) FC] and T-type cells [(d) general, (e) NPC and (f) FC]; and interleaved switching cells (ISC): I-type cells [(g) general, (h) NPC and (i) FC] and T-type cells [(j) general, (k) NPC and (l) FC].

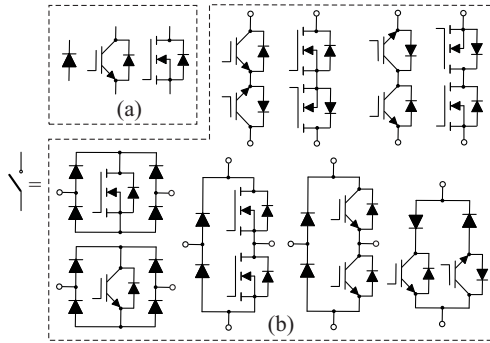


Fig. 2. Idealized switch realization using: (a) semiconductor devices or (b) bidirectional configurations.

on simple approaches, i.e., the general cell, the neutral-point clamped (NPC) and the flying capacitor (FC) cells, and can be used to generate novel high power nonisolated dc-dc, ac-dc, dc-ac, and ac-ac converters. The ideal switch can be implemented using only one semiconductor device, e.g., diodes, IGBTs and MOSFETs [see Figure 2.a], or bidirectional configurations of switches. Possible combinations for bidirectional switches involving the use of main semiconductor devices are presented in Figure 2.b, these configurations are reversible in current and voltage.

A. Nonisolated DC-DC Buck Converters with I-Type Multi-State and Interleaved Switching Cells

In this section, two dc-dc buck converters applying the I-Type multi-state and interleaved switching cells presented in Figure 1.a and Figure 1.g are studied. These topologies are shown in Figure 3.a and Figure 3.b, respectively.

1) *Principle of operation* - Both converters have similar operation. This paper is focused only on the analysis of the dc-dc buck converter based on IT-MSSC, shown in Figure 3.a. In order to simplify the analysis, the following assumptions are made: the operation occurs in continuous conduction mode (CCM); the circuit operates in steady state; the autotransformer presents unity turns ratio; the semiconductor compo-

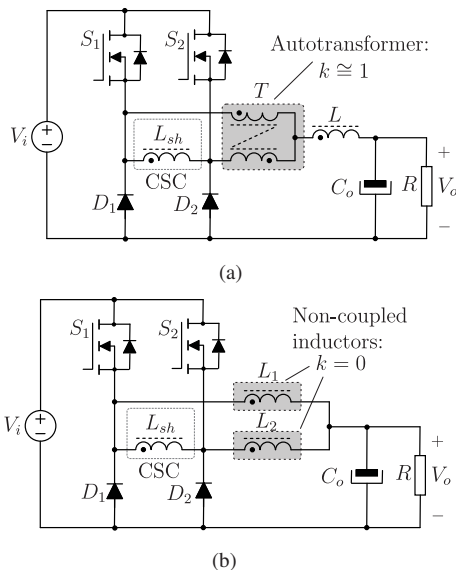


Fig. 3. DC-DC buck topologies based on: (a) IT-MSSC, (b) IT-ISC.

nents are ideal; the duty cycle of the switches is less than 0.5 (which characterizes the nonoverlapping mode (NOM)); PWM signals are displaced by 180 degrees.

Nine operating stages for distinct duty cycles of the PWM signals are described as follows and shown in Figure 4. The main theoretical waveforms are shown in Figure 5.

First stage (t_0, t_1): This stage begins when switch S_1 is turned on, while switch S_2 remains turned off. The current through diode D_2 is equally shared between winding N_2 and inductor L_{sh} . This stage finishes when the current through L_{sh} becomes zero.

Second stage (t_1, t_2): The same conditions of the previous stage are maintained. The current through L_{sh} increases linearly until it equals $[I_{M1}/2] + \Delta i$, when this stage is finished.

Third stage (t_2, t_3): Switch S_1 remains on and S_2 is off. Diode D_2 is reversely biased and the input current is shared between windings N_1 and N_2 through inductor L_{sh} .

Fourth stage (t_3, t_4): Switch S_1 is turned off and diode D_1 is forward biased, while switch S_2 remains off. The output current that flows through diode D_1 is shared between windings N_1 and N_2 due to inductor L_{sh} .

Fifth stage (t_4, t_5): This stage begins when switch S_2 is turned on, while switch S_1 remains off. The current through D_1 is shared between winding N_1 and inductor L_{sh} . The sum of the input current and the current through L_{sh} flows through winding N_2 . This stage finishes when the current through L_{sh} reaches zero.

Sixth stage (t_5, t_6): The same conditions of the previous stage are maintained. The current through L_{sh} decreases linearly until it equals $-[I_{M1}/2] + \Delta i$, when this stage is finished.

Seventh stage (t_6, t_7): Switch S_2 remains on and S_1 is off. Diode D_2 is reversely biased. The input current is shared between windings N_1 and N_2 through inductor L_{sh} .

Eighth stage (t_7, t_8): This stage represents the variation of the duty cycle Δt_D , which is applied to switch S_2 . The same conditions for the previous stage are maintained and the peak current through the switch increases to I_{M1} , as shown in Figure 5. The current sharing among the magnetic components is explained as follows.

Ninth stage (t_8, t_9): Switch S_2 is turned off and S_1 is maintained off. Diode D_2 is forward biased and the output current flows through it, which is shared between windings N_1 and N_2 through inductor L_{sh} .

2) *Theoretical analysis* - Inductor L_{sh} ensures zero average voltage across the winding, which allows the minimization of duty cycle differences, thus enabling equal voltages across the autotransformer windings. Therefore, the current is equally shared through windings N_1 and N_2 . By analyzing the operating stages, it can be seen that the CSC acts as a current source that provides half of the output current and also a path for balanced currents to flow through the windings.

The physical implementation of the autotransformer must consider that both windings are nearly identical, i.e., they must present the same impedance. The magnetizing inductance of the autotransformer is not able to share the current equally when duty cycle variations are applied to switches, as it can be seen in [1]. The autotransformer model with the addition of the current sharing inductor and considering the output

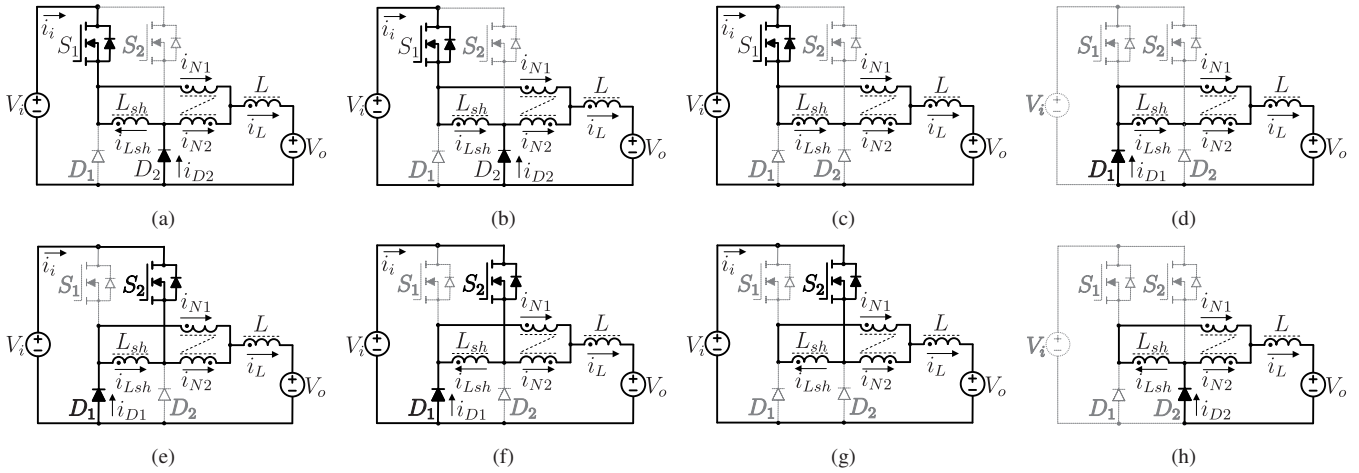


Fig. 4. Operation stages of the converter based on IT-MSSC: (a) 1st stage; (b) 2nd stage; (c) 3rd stage; (d) 4th stage; (e) 5th stage; (f) 6th stage; (g) 7th & 8th stage; and (h) 9th stage.

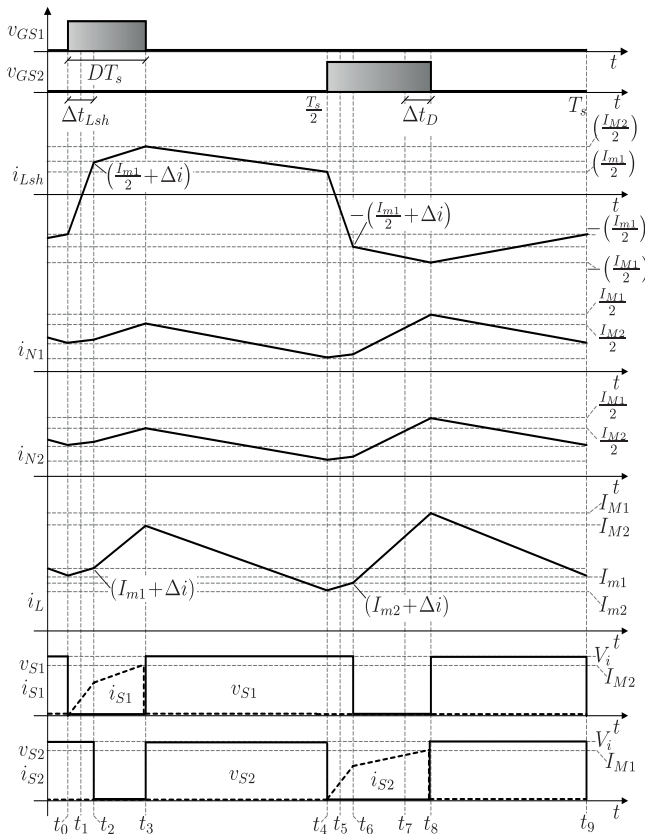


Fig. 5. Main theoretical waveforms.

filter inductor is shown in Figure 6, while the magnetizing inductance position changes according to the PWM signals. The model in Figure 6.a is equivalent to the stage when switch S_1 is turned on. Otherwise, the model in Figure 6.b is valid when switch S_2 is turned on.

3) *Static gain* - The static gain of the dc-dc buck topology is given by:

$$G = \frac{V_o}{V_i} = 2D - \Delta D \quad (1)$$

where:

V_o - Output voltage;

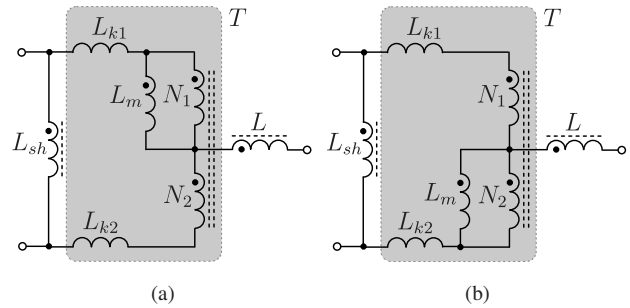


Fig. 6. Equivalent autotransformer model when: (a) switch S_1 is turned on, (b) switch S_2 is turned on.

V_i - Input voltage;

D - Duty cycle;

ΔD - Duty cycle reduction.

The static gain is valid for $D < 0.5$, which corresponds to NOM condition. It can be seen that such expression presents a duty cycle reduction due to the addition of the current sharing circuit, which is given by:

$$\Delta D = \frac{L_{sh} I_o}{V_i} f_s \quad (2)$$

where:

L_{sh} - Current sharing inductor;

I_o - Output current;

f_s - Switching frequency.

When compared with the topology without CSC [28],[29], the static gain of the analyzed converter is doubled, as shown in Figure 7.

4) *Output characteristics* - Due to the addition of the CSC, the converter presents duty cycle reduction. From (1), the output characteristic of the converter can be represented by:

$$V_o(I_o, D) = V_i \left(2D - \frac{L_{sh} I_o}{V_i} f_s \right). \quad (3)$$

The curves for the output voltage as a function of the output current considering several values of duty cycle are shown in Figure 8.

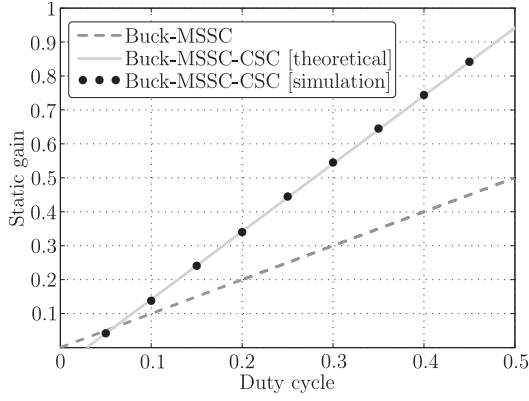


Fig. 7. Static gain as a function of duty cycle.

5) *Current sharing inductor design* - From (1) and (2), the sharing inductance can be obtained by:

$$L_{sh} = \frac{\Delta t_D}{\Delta I_{Lsh}} V_{Lsh} \quad (4)$$

where:

Δt_D - Time variation during the duty cycle reduction;
 ΔI_{Lsh} - Current variation through sharing inductor;
 V_{Lsh} - Voltage across the sharing inductance, which is equal to the input voltage.

With addition of the CSC, the topology achieves a new duty cycle which is given by:

$$D = \frac{1}{2} \left(\frac{V_o}{V_i} + \Delta D \right). \quad (5)$$

III. DESIGN EXAMPLE

The design procedure for both buck converters is similar to that presented in [1] and [29]. The specifications used in the implementation of the laboratory prototype are listed in Table I.

The design procedure is developed for the operation with duty cycle D , i.e., without the addition of the current sharing circuit. For the buck converter based on IT-MSSC, inductor L is given by:

$$L = \frac{V_i}{\beta f_s \Delta I_L} = \frac{200}{16 \cdot 25 \cdot 10^3 \cdot 3.34} = 145 \mu H \quad (6)$$

where:

TABLE I
Design Specifications

Parameters	Value
Input voltage	$V_i=200$ V
Output voltage	$V_o=60$ V
Rated output power	$P_o=1$ kW
Switching frequency	$f_s=25$ kHz
Output voltage ripple	$\Delta V_o=1\%V_o=0.6$ V
Inductor L current ripple	$\Delta I_L=20\%I_o=3.34$ A
Inductor L_{sh} current ripple	$\Delta I_{Lsh}=I_o=16.67$ A
Active duty cycle interval	$t_D=12$ μ s
Time variation during duty cycle reduction	$\Delta t_D=20\%t_D=2.4$ μ s

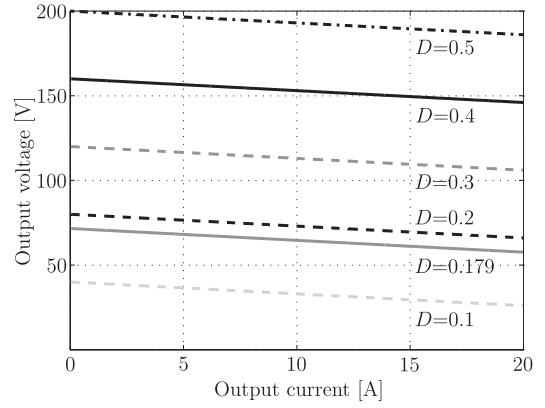


Fig. 8. Output characteristic.

β - Normalized current ripple;
 ΔI_L - Inductor L current ripple.

On the other hand, inductors L_1 and L_2 of the buck converter based on IT-ISC are determined by:

$$L_{1,2} = \frac{V_o (1 - 2D)}{f_s \Delta I_L} = \frac{60 \cdot 0.4}{25 \cdot 10^3 \cdot 3.34} = 290 \mu H. \quad (7)$$

From (4) by using the design and parameter specifications, the sharing inductor can be determined by:

$$L_{sh} = \frac{2.4 \cdot 10^{-6}}{16.67} \cdot 200 \cong 28 \mu H. \quad (8)$$

For the design procedures, one has considered that the duty cycle variations are around 20%. Therefore, the inductor L_{sh} is able to maintain proper sharing under such condition. After determining inductance L_{sh} and by using (2), the duty cycle reduction can be obtained from:

$$\Delta D = \frac{28 \cdot 10^{-6} \cdot 16.667}{200} \cdot 25 \cdot 10^3 = 0.058. \quad (9)$$

The new duty cycle for converters with CSC is determined from (5), as follows:

$$D = \frac{1}{2} \cdot \left(\frac{60}{200} + 0.058 \right) = 0.179. \quad (10)$$

The detailed description of the components used in the experimental prototype is given in Table II.

TABLE II
Prototype Components

Component	Description
Switches S_1 and S_2	MOSFET IRFP4768
Diodes D_1 and D_2	Ultrafast diode 30EPH06
Output capacitor C_o	Epcos B43501, 1 mF/250V
Inductors L_1 and L_2 (buck converter based on IT-ISC)	Core: Thornton NEE-55/28/21; Inductance: 290 μ H; Turns: 27; Wire: 17xAWG 26
Inductor L (buck converter based on IT-MSSC)	Core: Thornton NEE-55/28/21; Inductance: 145 μ H; Turns: 22; Wire: 33xAWG 26
Autotransformer T	Core: Thornton NEE-65/33/26; turns ratio: 1:1; magnetizing inductance: 10 mH
Inductor L_{sh}	Core: Thornton NEE-30/14; Inductance: 29 μ H; Turns: 17; Wire: 15xAWG 26

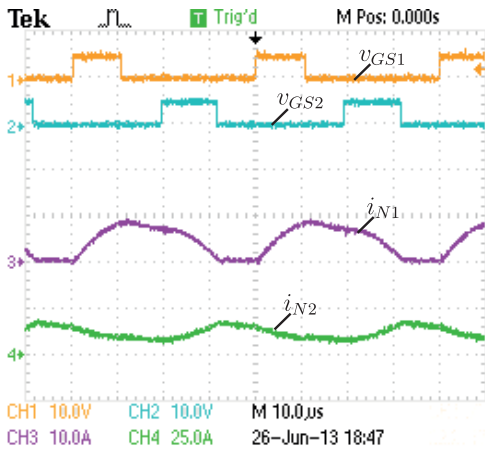


Fig. 9. Gate voltage of switches S_1 and S_2 , and currents through the autotransformer windings N_1 and N_2 .

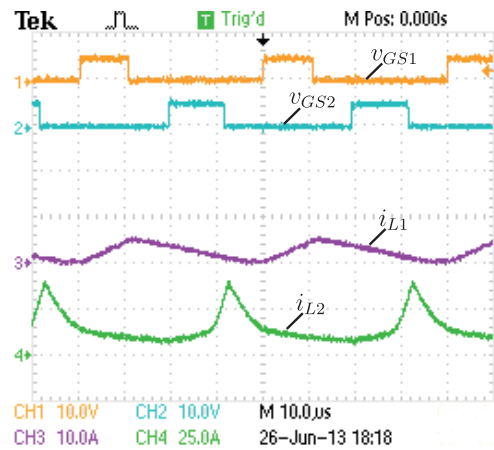


Fig. 10. Gate voltage of switches S_1 and S_2 , and currents through the inductors L_1 and L_2 .

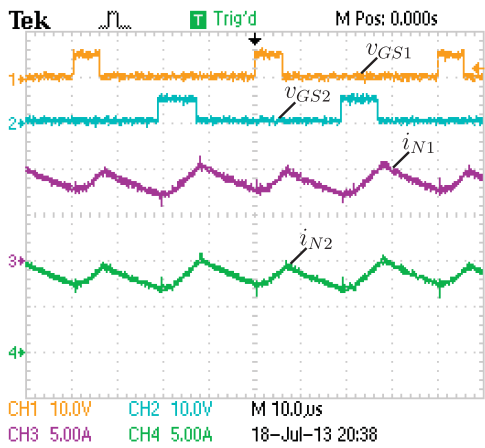


Fig. 11. Gate voltage of switches S_1 and S_2 , and currents through the autotransformer windings N_1 and N_2 .

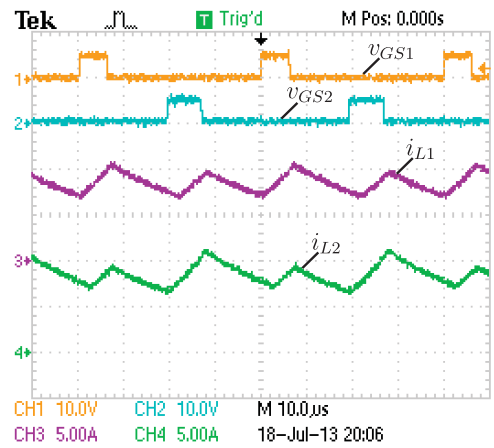


Fig. 12. Gate voltage of switches S_1 and S_2 , and currents through the inductors L_1 and L_2 .

IV. EXPERIMENTAL RESULTS

In order to validate the proposed current sharing method, a versatile modular prototype was implemented and two resulting converters were evaluated in laboratory. Some results are presented for both topologies with and without the CSC for unbalanced duty cycles. It is worth to mention that a duty cycle variation of 20% is applied to one switch. In terms of time, such variation corresponds to about $1.4 \mu\text{s}$, which is distributed during turn-on and turn-off of the switch. A similar test was performed in [1] and a comparative analysis for converters based on the parallelism of semiconductors, interleaved cells, and multi-state switching cells is also presented.

A. Results for Converters without Current Sharing Circuit

Figure 9 shows the measured gate-to-source voltages for switches S_1 and S_2 (v_{GS1} and v_{GS2} , respectively), and also the currents through the autotransformer windings (i_{N1} and i_{N2}) for the buck converter based on IT-MSSC. Figure 10 shows the measured gate-to-source voltages for switches S_1 and S_2 (v_{GS1} and v_{GS2} , respectively), and also the current waveforms for the interleaved inductors (i_{L1} and i_{L2}) in the buck converter based on IT-ISC.

B. Results for Converters with Current Sharing Circuit

Figure 11 shows the measured gate-to-source voltages for switches S_1 and S_2 (v_{GS1} and v_{GS2} , respectively), and also currents through the autotransformer windings (i_{N1} and i_{N2}) for the buck converter based on IT-MSSC. Figure 12 shows the measured gate-to-source voltages for switches S_1 and S_2 (v_{GS1} and v_{GS2} , respectively), as well as the current waveforms for the interleaved inductors (i_{L1} and i_{L2}) in the buck converter based on IT-ISC.

The experimental results presented in Figures 9 and 10 demonstrate that the topologies without CSC present large unbalance between the currents through the autotransformer windings and inductors. It can be also seen that the magnetic elements present core saturation. The topologies with CSC do not present current unbalance involving the same aforementioned currents. The duty cycle variations are compensated by the CSC, as it can be seen in the experimental results presented in Figures 11 and 12.

The experimental curves of efficiency as a function of the output power for two topologies with and without the addition of CSC are shown in Figure 13. When compared with topologies without CSC, CSC-based converters tend to present lower efficiency due to one additional magnetic component.

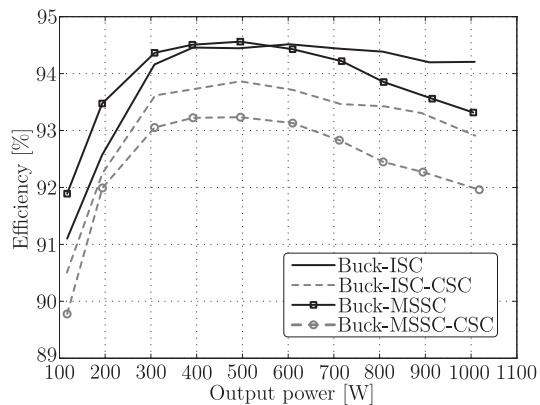


Fig. 13. Experimental curves of efficiency as a function of the output power.

V. CONCLUSION

This paper has presented MSSCs and ISCs with the addition of a CSC that allow the generation of novel high power level converters. The small differences in the duty cycle of the controlled switches cause serious current unbalance in magnetic components, which may lead to saturation. In order to minimize such issue, impedances based on small inductors can be added between the legs of the switching cells, which ensure zero average voltage across the windings of magnetic components. Therefore, the currents are properly shared through magnetics. During the physical implementation process, it is worth to mention that the magnetic windings must present nearly the same impedance, since the proposed technique is only able to compensate for duty cycle variations.

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René Pastor Torrico Bascopé received the B.Sc. degree in Electrical Engineering from San Simón University, Cochabamba, Bolívia, in 1992, and the M.Sc. and Dr. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1994 and 2000, respectively.

He is currently an Associate Professor with the Department of Electrical Engineering, Federal University of Ceará, Fortaleza, Brazil. His main research interests include power supplies, power factor correction techniques, uninterruptible power systems, and renewable energy systems.

Dr. Torrico-Bascopé is a member of the Brazilian Society of Power Electronics

Grover Victor Torrico Bascopé received the B.Sc. degree in Electrical Engineering from San Simón University, Cochabamba, Bolívia, in 1993, and the M.Sc. and Dr. degrees in Electrical Engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1996 and 2001, respectively.

From 2001 to 2002, he was an Advisor with Emerson Energy System, Brazil. In 2003, he was a Senior Design Engineer with Emerson Network Power Company, Ltd., Stockholm, Sweden. From 2004 to 2009, he was a Senior Engineer in Power Electronics Designs with the R&D Group, Eltek Valere AB, Sweden. Since July 2009, he has been a Senior Design Engineer with GTB Power Electronics Research and Technology AB, Kista, Sweden. He has published more than 20 technical papers and is the holder of two patents. His main research areas are industrial power electronics and creation of new platforms with high efficiency topologies for high-power and green energy applications.

Francisco José Barbosa de Brito Júnior was born in Nova Olinda - CE, Brazil, in 1989. He received the B.Tech. degree in Industrial Automation from the Federal Institute of Ceará, Juazeiro do Norte, Brazil, in 2010 and the M.Sc. degree in Electrical Engineering from the Federal University of Ceará, Fortaleza, Brazil, in 2013.

He is currently pursuing his doctoral degree in Electrical Engineering from the Federal University of Ceará and develops researches with the Energy Processing and Control Group (GPEC). His research areas include power electronics converters, series and parallel connection of power converters, and high-efficiency topologies.

MSc. Brito Jr. is student member of the IEEE Power Electronics Society (PELS) and the Brazilian Society of Power Electronics (SOBRAEP).

Sérgio Daher was born in Fortaleza, Brazil, in 1971. Received the B.Sc. degree in electrical engineering from Federal University of Paraíba - Brazil in 1995, M.Sc. degree in electrical engineering from Federal University of Ceará, Brazil in 1997, and Dr.-Ing. degree in electrical engineering from Universität Kassel - Germany in 2006.

Currently, he is a senior lecturer at the Federal University of Ceará. His research areas include Electrical Machines Drives, Power Electronics and Renewable Energy Systems.