TWO DIGITAL-SCALAR PWM SCHEMES FOR GENERATING THREE-PHASE UNBALANCED VOLTAGES

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***Abstract* - This paper presents two modulation approaches for generating unbalanced voltages by means of four-leg voltage source inverters (VSI). The first modulation is an extended scheme of a digital scalar pulse width modulation previously proposed for controlling three-leg inverters. The second one is based on the decomposition of the voltage reference signals into their symmetrical components. The schemes are compared theoretically, by simulations and by experimental results. As consequence, it is found out a total equivalence between the two modulations despite their different inspirations. The fundamentals of both techniques and a mathematical proof of their equality are unfolded. Also, the performance of the techniques with respect to the harmonic distortion and power switching loss are discussed. The results show that the techniques are effective.**

***Keywords* – Four-Leg Converter, Power Quality, Scalar PWM, Sequence Components, Space Vector PWM, Unbalanced Voltages.**

I. INTRODUCTION

Pulse width modulation techniques have a central role in the control process of power electronic devices connected to the grid for monitoring and controlling power quality indexes of sensitive and critical loads, allowing the reproduction of the control signals, by means of pulse-width modulation (PWM) techniques. To be effective, these techniques are supposed to reproduce PWM signals with low total harmonic distortion (THD), small delay and be easy to implement in digital signal controllers.

Nowadays, several power electronics devices are applied to mitigate power quality problems. This tendency can be understood as there are an increasing number of sensitive electronic loads with growing control capabilities connected to the utility grid. Most of these problems result in unbalanced current or voltage variations [1]. To compensate these variations, the devices must be able to generate and insert three-phase unbalanced voltages into the power supply by means of a VSI. To provide the neutral, one can use split DC-linked capacitors and tying the neutral point to the mid-point of the DC linked [2] or use a four-leg inverter topology and tying the neutral point to the mid-point of the fourth leg [3].

To control the VSI, many modulations techniques has been proposed in the literature. When it comes to synthesize balanced voltages, a three-leg, three-wire VSI is sufficient. In this situation, one alternative is to use carrier-based techniques, which can be implemented analogically [4] or digitally, [5]. Other approach is to employ the two-dimensional space-vector PWM. This technique is most popular due to their flexibility and good performance in relation to harmonic content [6]. Nevertheless, custom power devices such as dynamic voltage restorers, active power filters, FACTs usually have to compensate the variations with unbalanced voltages [7–9]. To synthesize these voltages, there have been proposed a plethora of methods, mainly based on a four-leg VSI. A common approach of controlling the switching instants is to extend the space-vector analysis to the third-dimension [10–13]. This leads to flexible techniques, with good harmonic content characteristic, but at a cost of higher computational effort and awkward implementation. An interesting technique was proposed in [14], which is also based on the space-vector modulation. The technique makes use of two planes of state vectors to generate asymmetric voltages in lieu of a three dimensional analysis.

Scalar modulation techniques, as opposed to space-vector ones, have the advantage of being computationally more efficient [15], [16]. Nevertheless, these techniques are seldom presented for a four-leg VSI. In [17], it was established a clear equivalence between the space-vector modulation and the digital scalar method. The paper presented a method for implementing the two-dimensional space-vector modulation by using the simpler framework of the digital scalar technique. However, the method was developed for a three-leg VSI to synthesize balanced voltages. Still regarding scalar modulations, a technique based on symmetrical components was proposed in [18]. The implementation of this technique is simple and takes advantage of the fact that many methods for compensating unbalanced voltage signals intrinsically use a decomposition of symmetrical components of the voltages [19], [20].

In this paper, it is proposed an extension of the work presented in [17] to control a four-leg VSI and generate unbalanced voltages. Moreover, it is proved that this technique is equivalent to the one presented in [18]. The paper is organized as follows: The second section briefly describes a digital scalar pulse width modulation (DSPWM) and its equivalence to the well-known space vector pulse width modulation (SVPWM). The third section presents the extended digital scalar pulse width modulation (EDSPWM) which is an adaptation of the DSPWM for controlling the four-leg inverters. The fourth section outlines a modulation

Manuscript received 14/12/2011; Revised on 11/02/2012. Accepted for publication 24/02/2012 by recommendation of the Editor Joo Onofre Pereira Pinto.

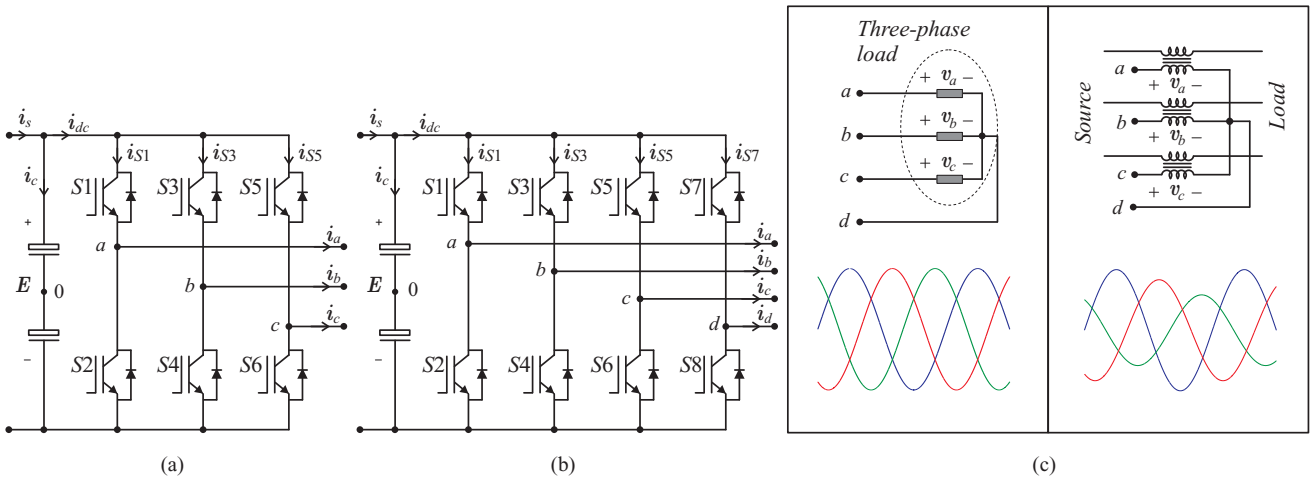


Fig. 1. Voltage source inverters. (a) Three-legs. (b) Four-legs. (c) Typical applications with three-phase four-wire system demanding: (left) balanced voltages, as in motor drive; and (right) unbalanced voltages, as used in DVR.

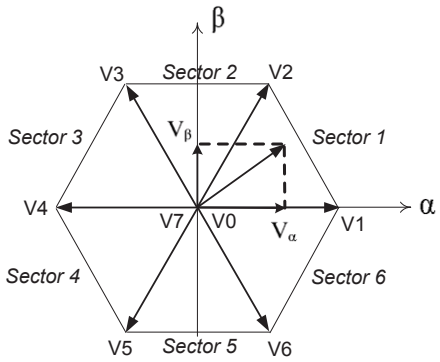


Fig. 2. A space vector located at first sector in the $\alpha\beta$-plane.

technique based on symmetrical components theory, the so-called symmetrical component pulse width modulation (SCPWM). The fifth section demonstrates the equivalence between the two modulations. The results are presented in the sixth section and the conclusions are drawn in the seventh section.

II. DIGITAL SCALAR PULSE WIDTH MODULATION FOR THREE-LEG INVERTERS

A sinusoidal three-phase voltage system can be represented by a complex vector rotating in a two-dimensional reference frame. This vector should be used as the reference voltages for the PWM signals in each phase of a three-phase, three-leg VSI. The power converter with a three-phase Y connected load with neutral "n" non interconnected is shown in Figure 1(a).

When the reference sinusoids are balanced, the two-dimensional space vector modulation (SVPWM) is widely employed for purpose of PWM generation, due to its flexibility [6]. Figure 2 shows the complex vector in the first sector. On the plane, there are six active voltage vectors of amplitude $\sqrt{\frac{2}{3}}E$, spatially separated 60^o from each other, and two null voltage vectors. The space vector can be represented by a pondered sum of the two adjacent vectors and two null vectors.

Figure 3(a) depicts two adjacent PWM periods. Note that the first period starts at low level whilst the second one starts at high level. The intervals of time t_1 and t_2 represent the period where the two adjacent vectors collaborate to the average of the signal. The intervals t_{01} and t_{02} are periods in which all top switches from the inverter are closed or opened. The rate $\mu = t_{01}/(t_{01} + t_{02})$ is the so-called "distribution rate" to be arbitrarily fixed.

Alternatively to the SVPWM, the DSPWM imposes to the pole voltage of the inverter (v_{a0}, v_{b0} and v_{c0}), an average voltage value corresponding to each reference phase within the sampling interval. This strategy is simpler than the SVPWM but does not impose directly the reference to the voltage phases. A version of this technique, proposed in [17], overcomes this problem by adding to the pole references an homopolar voltage v_h:

$$v_j^{*\prime} = v_j^* + v_h, \qquad j = a, b, c \tag{1}$$

where voltages v_j^* are the reference voltage samples desired to be imposed to the phases by the inverter during a PWM period. Thus, as the usual scalar-digital PWM, the pulse widths of the pole voltages are determined by:

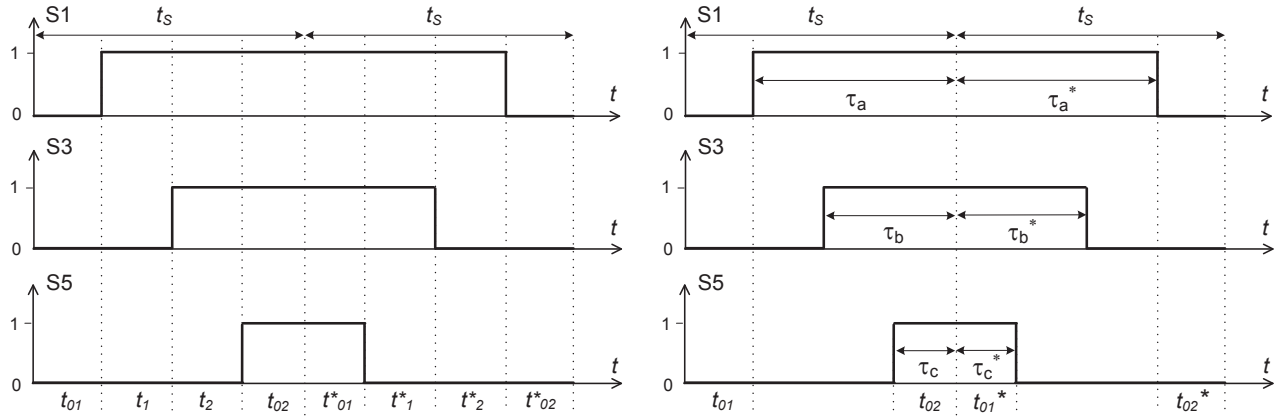
$$\tau_j = \left(\frac{v_j^{*\prime}}{E} + \frac{1}{2}\right) t_s \tag{2}$$

with t_s being the sampling period of the signal and E being the DC voltage of the inverter. Figure 3(b) shows the pulse widths synthesized by the top switches of the inverter. The homopolar voltage v_h is defined as:

$$v_h = E\left(\frac{1}{2} - \mu\right) - (1 - \mu)\, v_M - \mu v_m \tag{3}$$

with v_M and v_m being the maximum and minimum voltage value chosen among the three reference voltages for each sampled time.

It has been established a correlation between the DSPWM and the SVPWM techniques. This is useful because the former



(a) (b)

Fig. 3. Switching functions for generating a space vector in the first sector. (a) Three-phase pulses from SVPWM; (b) Three-phase pulses from DSPWM.

is quite simple to implement, and the latter has desirable features in respect with harmonic distortion. Nevertheless, the DSPWM technique in [17] has not been developed to generate unbalanced voltages. Also, the inverter shown in Fig. 1(a) is not suitable for this task since it has no path for the zero-sequence current. This problem could be solved by connecting the neutral of the load to the middle point of the capacitors. However, such procedure has the disadvantages of reducing the use of DC voltage resulting in higher variations in this voltage. Figure 1(b) (together with load options in the Figure 1(c)) shows a better inverter configuration which overcomes these drawbacks. Next section presents the EDSPWM technique to control such inverter.

III. EXTENDED DIGITAL-SCALAR PULSE WIDTH MODULATION - EDSPWM

The idea behind this technique is to impose the homopolar voltage v_h to the pole d of a fourth leg. Thus, it follows:

$$v_a^{*\prime} = v_a^* + v_h \quad (4)$$
$$v_b^{*\prime} = v_b^* + v_h \quad (5)$$
$$v_c^{*\prime} = v_c^* + v_h \quad (6)$$
$$v_d^{*\prime} = 0 + v_h. \quad (7)$$

This procedure assures that any desired references v_a^*, v_b^*, and v_c^* will be imposed to the voltage phases of the load. This can be verified by examining the circuit path "ad0a" in Figure 1(b). Thus, for phase a, one can write:

$$v_{ad} = v_{a0} - v_{d0}. \quad (8)$$

As voltages v_{a0} and v_{d0} are imposed to be equal to the references $v_a^{*\prime}$ and $v_d^{*\prime}$ through the switches S_1, S_2, S_7 and S_8, one can have any set of voltage phases, balanced or not. The pulse widths are determined as:

$$\tau_a = \left(\frac{v_a^{*\prime}}{E} + \frac{1}{2}\right) t_s, \quad (9)$$
$$\tau_b = \left(\frac{v_b^{*\prime}}{E} + \frac{1}{2}\right) t_s, \quad (10)$$
$$\tau_c = \left(\frac{v_c^{*\prime}}{E} + \frac{1}{2}\right) t_s, \quad (11)$$
$$\tau_d = \left(\frac{v_d^{*\prime}}{E} + \frac{1}{2}\right) t_s, \quad (12)$$

IV. SYMMETRICAL-COMPONENT PULSE WIDTH MODULATION - SCPWM

An alternative approach for generating unbalanced three-phase voltage references with a 4-leg inverter uses a scalar modulation based on the symmetrical components theory. The idea is to take advantage of an instantaneous component symmetric transformation presented in [21]. Thus, if v_a^*, v_b^*, and v_c^* are the instantaneous unbalanced voltage values to be reproduced by the inverter, one can extract the zero sequence from these values to obtain the sum of the positive and negative symmetrical sequences v_{as}^*, v_{bs}^*, and v_{cs}^*. In turn, zero-sequence values must be added to the homopolar voltage v_{hs} defined analogously to (3):

$$v_{hs} = E\left(\frac{1}{2} - \mu\right) - (1-\mu)\, v_{Ms} - \mu v_{ms} \quad (13)$$

with v_{Ms} and v_{ms} now being the maximum and minimum values chosen among v_{as}^*, v_{bs}^* and v_{cs}^* for each sampled time. Therefore, one can write the pulse widths to the pole voltages as:

$$\tau_1 = \left(\frac{v_{as}^{*\prime}}{E} + \frac{1}{2}\right) t_s \quad (14)$$
$$\tau_2 = \left(\frac{v_{bs}^{*\prime}}{E} + \frac{1}{2}\right) t_s \quad (15)$$
$$\tau_3 = \left(\frac{v_{cs}^{*\prime}}{E} + \frac{1}{2}\right) t_s \quad (16)$$

where $v_{as}^{*\prime} = v_{as}^{*} + v_{hs}$, $v_{bs}^{*\prime} = v_{bs}^{*} + v_{hs}$, and $v_{cs}^{*\prime} = v_{cs}^{*} + v_{hs}$.

If these pulses were applied to the poles of the inverter, they would impose the sum of positive and negative symmetrical voltages across the phases of the load. To take into account the zero sequence, first, consider the situation where the fourth leg is not operating (switches $S7$ and $S8$ are open). If $S1$ close and $S3$ and $S5$ opened, the phase voltages are $\frac{2}{3}E$, $-\frac{1}{3}E$ and $-\frac{1}{3}E$. Now, consider the closuring of $S8$, without changing the positions of the other switches. The phase voltages are:

$$v_{an} = E = \frac{2}{3}E + \frac{1}{3}E \tag{17}$$

$$v_{bn} = 0 = -\frac{1}{3}E + \frac{1}{3}E \tag{18}$$

$$v_{cn} = 0 = -\frac{1}{3}E + \frac{1}{3}E. \tag{19}$$

The phase voltages are the same as those generated by the 3 legs but with the addition of a zero sequence voltage to each one of the phase voltages. Table I shows the zero sequence voltage generated by the fourth leg with the switches in the first three legs set to generate the state vectors.

TABLE I
Zero sequence voltage generated in each state

State	Zero sequence voltage S7	S8
V0	0	E
V1	$-\frac{2}{3}E$	$\frac{1}{3}E$
V2	$-\frac{1}{3}E$	$\frac{2}{3}E$
V3	$-\frac{2}{3}E$	$\frac{1}{3}E$
V4	$-\frac{1}{3}E$	$\frac{2}{3}E$
V5	$-\frac{2}{3}E$	$\frac{1}{3}E$
V6	$-\frac{1}{3}E$	$\frac{2}{3}E$
V7	$-E$	0

Now consider the switching sequence shown in Table II for generating a space vector in any sector of the diagram shown in Figure 2. The phase voltages for the 4-leg converter are the sum of the corresponding voltages for the 3-leg inverter and a zero sequence voltage which varies during the switching period as shown in Figure 4. The two stepped waveforms shown in this figure result from the closure of $S8$ or $S7$. Note that the stepped waves are vertically displaced from each other by the constant voltage of the DC-link.

TABLE II
Switching sequences for generating PWM pulses

Sector	Switching sequence						
1	V7	V1	V2	V0	V2	V1	V7
2	V7	V3	V2	V0	V2	V3	V7
3	V7	V3	V4	V0	V4	V3	V7
4	V7	V5	V4	V0	V4	V5	V7
5	V7	V5	V6	V0	V6	V5	V7
6	V7	V1	V6	V0	V6	V1	V7

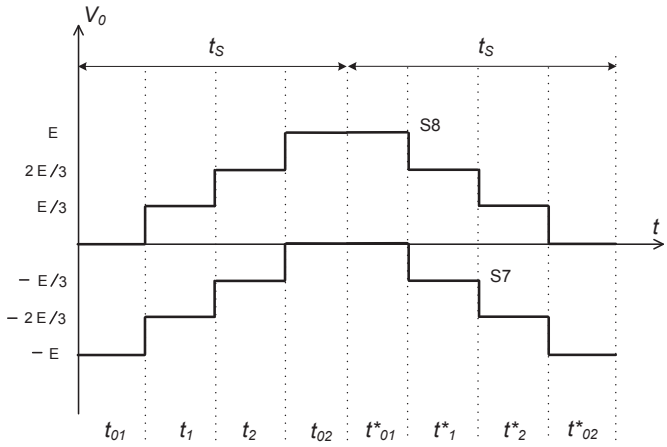


Fig. 4. Zero sequence voltage variation during any switching period.

Now, sort (τ_1, τ_2, τ_3) into $(\tau_{min}, \tau_i, \tau_{max})$. Then, it is fixed:

$$t_1 = (\tau_{max} - \tau_i)/2 \tag{20}$$

$$t_2 = (\tau_i - \tau_{min})/2. \tag{21}$$

Suppose $\mu = 0.5$, i.e., $t_{01} = t_{02} = t_z$. Also, suppose that $S8$ is closed during a switching period, except during an interval τ_4 when the switch $S7$ is closed. Then the zero sequence voltage generated during this switching period is given by:

$$v_0 = E\left[\frac{1}{2} - \frac{(t_1 - t_2)}{6t_s}\right] - \frac{\tau_4}{t_s}E. \tag{22}$$

Therefore, the switching interval for $S7$ required for generating a given zero sequence voltage v_0 is

$$\tau_4 = t_s\left(\frac{1}{2} - \frac{v_0}{E}\right) - \frac{t_1 - t_2}{6}. \tag{23}$$

Summarizing, the SCPWM scheme for the 4-leg inverter is given by the following steps:

(i) Determine τ_1, τ_2 and τ_3 (equations (14)-(16)).

(ii) Determine the intervals t_1,t_2 (equations (20) and (21)).

(iii) Determine the interval τ_4 for the fourth leg, as given by (23). Figure 5 shows the switching function for $S7$.

Note that the SCPWM is also a kind of digital-scalar PWM, since there is no need to define a complex vector for a sinusoidal 3-phase reference.

V. EQUIVALENCE BETWEEN EDSPWM AND SCPWM

A strict comparison between the two modulation schemes here proposed must be carried out by comparing the pulses $(\tau_1, \tau_2, \tau_3, \tau_4)$ with $(\tau_a, \tau_b, \tau_c, \tau_d)$.

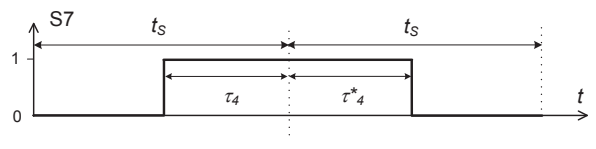


Fig. 5. Switching function for $S7$.

To prove that τ_1 and τ_a are equal, it is enough to show that $v_a^{*\prime}$ is equivalent to $v_{as}^{*\prime}$. Thus, by definition:

$$v_a^* = v_{as}^* + v_0 \tag{24}$$

$$v_M = v_{Ms} + v_0 \tag{25}$$

$$v_m = v_{ms} + v_0. \tag{26}$$

Substituting (25) and (26) in (3), it follows:

$$v_h = v_{hs} - v_0. \tag{27}$$

Finally, substituting (24) and (27) in (4), and having in mind (13), one readily finds:

$$v_a^{*\prime} = v_{as}^* + v_{hs}. \tag{28}$$

Thus, $v_a^{*\prime} = v_{as}^{*\prime}$, which means that $\tau_1 = \tau_a$. Analogous argument may be applied to find $\tau_2 = \tau_b$ and $\tau_3 = \tau_c$.

To show the equivalence between pulses τ_d and τ_4, first one has to rewrite (9)-(11), using (4)-(6):

$$v_a^* + v_h = \frac{\tau_a - (t_s - \tau_a)}{t_s} E \tag{29}$$

$$v_b^* + v_h = \frac{\tau_b - (t_s - \tau_b)}{t_s} E \tag{30}$$

$$v_c^* + v_h = \frac{\tau_c - (t_s - \tau_c)}{t_s} E. \tag{31}$$

Now observing Figure 3, one can write:

$$\tau_a = t_1 + t_2 + t_{02} \tag{32}$$

$$\tau_b = t_s - t_{01} - t_1 \tag{33}$$

$$\tau_c = t_{02} \tag{34}$$

and keeping in mind that

$$v_a + v_b + v_c = 3v_0 \tag{35}$$

one can sum up (29)-(31), and after some manipulation write:

$$v_h = -v_0 + \frac{-t_1 + t_2}{6t_s} E + \frac{t_{02} - t_{01}}{2t_s} E. \tag{36}$$

Then, substituting (36) in (12) to write:

$$\tau_d = \left[\frac{-v_0}{E} + \frac{-t_1 + t_2}{6t_s} + \frac{t_{02} - t_{01}}{2t_s} \right] t_s + \frac{1}{2} t_s \tag{37}$$

and finally, setting $\mu = 0.5$, that is $t_{01} = t_{02}$, the expression for τ_d is given by:

$$\tau_d = t_s \left(\frac{1}{2} - \frac{v_0}{E} \right) - \frac{t_1 - t_2}{6} \tag{38}$$

which is equal to (23).

Thus the pulse widths produced by EDSPWM and the SCPWM techniques have equivalent equations. This means the schemes generate the same unbalanced three-phase voltages.

VI. RESULTS

The first part of this section is comprised by simulations carried out to corroborate the equivalence of the EDSPWM and SCPWM modulation techniques. The second one presents the experimental results. Also, it is shown the effectiveness of these techniques by comparing them with a space vector modulation proposed in [14]. All the results presented here were generated with a PWM cycle, t_s of 100 μs.

A. Simulated results

To begin with, the EDSPWM and SCPWM modulations will be used to synthesize references of unbalanced voltages with the following characteristics: phase A (V_{an}) has magnitude of 100 V, phase B (V_{bn}) of 70 V, and phase C (V_{cn}) of 90 V. The references are shifted of 120° from each other. Figure 6 shows the modulated voltages synthesized by the converter phases from both techniques. It is clear the equivalence between the two methods. To demonstrate that the methods are producing the correct references, the fundamental phases of the modulated signals are shown in Figure 7. As can be noted, there is an agreement between them and the reference signals.

To investigate the performance of the EDSPWM with respect to the harmonic content, Figure 8 plots the weighted total harmonic distortion (WTHD) for the EDSPWM and for the technique presented in [14] in relation to the modulation index, M, defined as:

$$M = \frac{\sqrt{3}V}{E}, \tag{39}$$

where V is the highest peak among the three sinusoid references to be reproduced. It was established an asymmetry pattern for the three-phase voltages. Thus, for each modulation index value, phase A is a reference, phase B is fixed to 70% of A and phase C to 90% of A. The DC link voltage E is constant. In this figure, the technique proposed in [14] is labeled 4-leg SVPWM, since is, in fact, a kind of space vector used in four-leg inverters. The two modulations were implemented for a distribution rate, μ, equal to 0.5. From the figure, one can infer that for most values of M, the EDSPWM technique is advantageous over the 4-leg SPWM. This fact is accentuated for higher values of M.

Other important feature to be examined in any modulation technique is its behavior regarding the power losses resulting from the VSI switching. In this work, the loss estimation was based on the work presented in [22]. The tests presented here made use of a dual-module CM50DY-24H (POWEREX) insulated-gate bipolar transistor (IGBT) driven by a SKHI23 (SEMIKRON). The switch loss model includes: 1) IGBT and diode conduction losses; 2) IGBT turn-on losses; 3) IGBT turn-off losses; and 4) diode turn-off energy. Figure 9 compares the EDSPWM with the 4-leg SPWM, from reference [14]. It shows a normalized loss for the two techniques plotted against the modulation index. From the figure, one concludes that again the EDSPWM has a superior performance. This result can be better understood if one determines the average number of switching per cycle for each modulation. Table III summarizes these numbers for the three

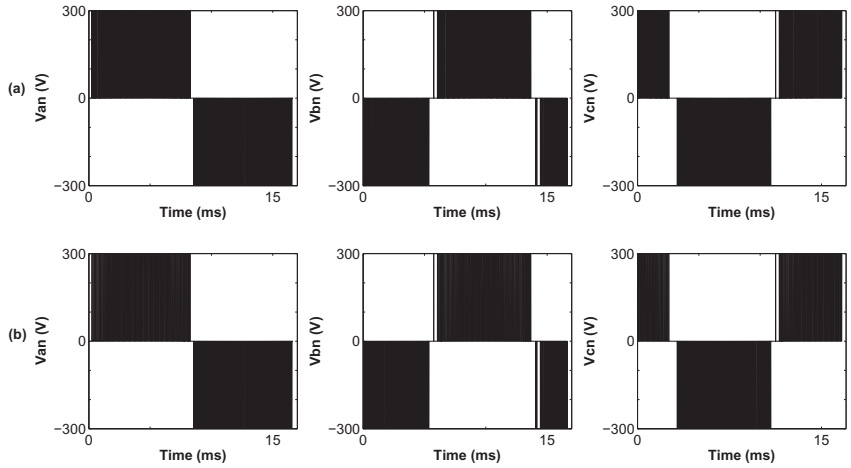


Fig. 6. Unbalanced modulated voltages produced by techniques: (a) EDSPWM; (b) SCPWM.

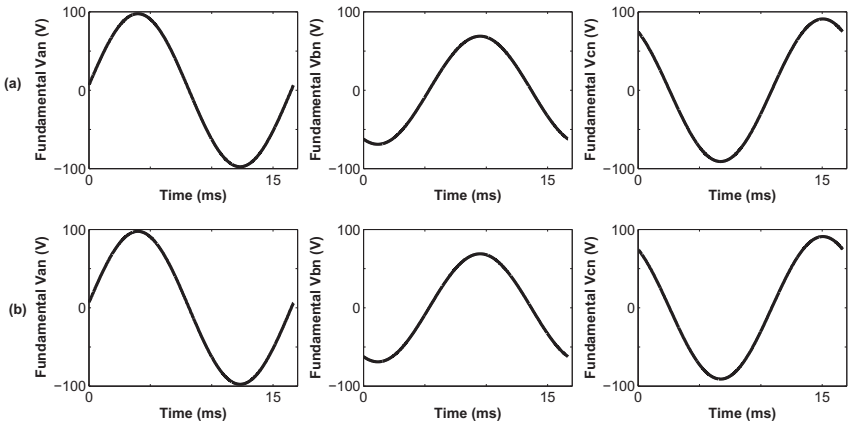


Fig. 7. Fundamental phases generated by techniques: (a) EDSPWM; (b) SCPWM.

modulations methods. As previously stated, the EDSPWM and the SCPWM present the same results.

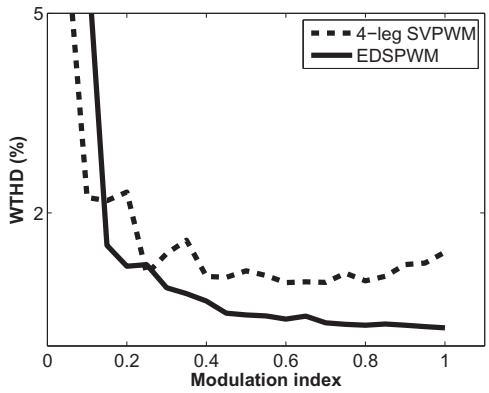


Fig. 8. Weighted total harmonic distortion variation with respect to the modulation index.

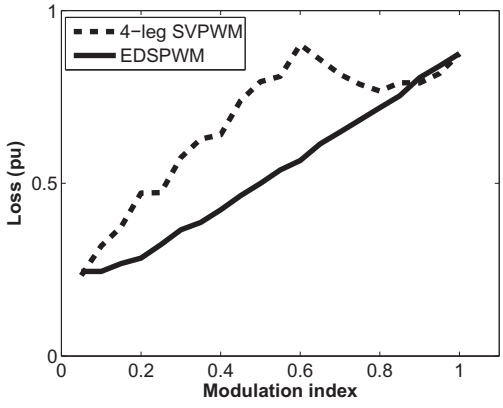


Fig. 9. Power loss variation with respect to the modulation index.

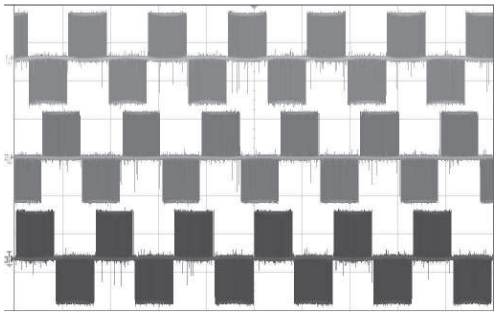
B. Experimental results

The experimental apparatus used to implement the modulation techniques comprises a four-leg VSI, with an acquisition and processor system. The DC bus voltage was

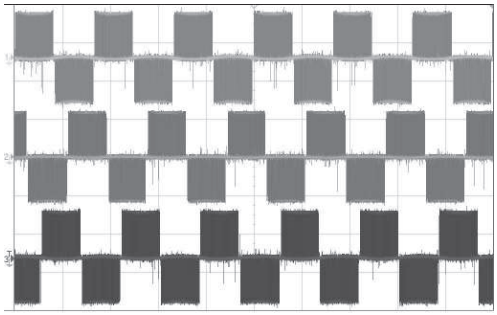
TABLE III
Comparison of PWM schemes in respect to the number of switching per PWM period

	EDSPWM	SCPWM	4-leg SVPWM
Number of switching	16	16	24

set in 300 V and the PWM cycle, t_s 100 μs. The reference voltages to be generated are the same of the simulated cases. Figure 10(a) and 10(b) show respectively the modulated phases V_{an}, V_{bn} and V_{cn} for the EDSPWM and the SCPWM techniques. As expected, they are identical. The fundamental phases are measured in Figure 11(a) and 11(b). They are filtered waveforms from the corresponding modulated voltages. Again, it is demonstrated the equivalence between the techniques.



(a) Modulated phase voltages for the EDSPWM. Vertical scale = $165V/div$.

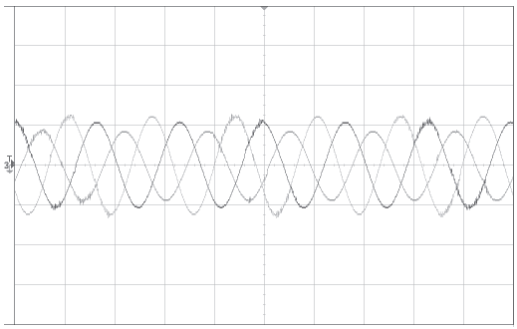


(b) Modulated phase voltages for the SCPWM. Vertical scale = $165V/div$.

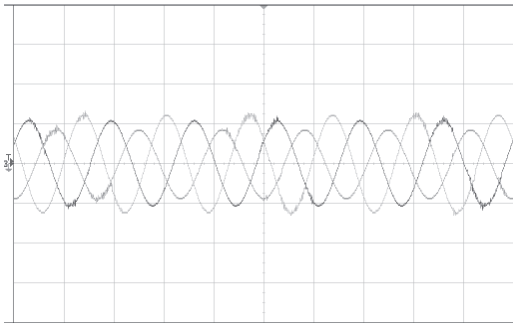
Fig. 10. Modulated phase voltages.

VII. CONCLUSION

This paper has presented two modulation schemes for generating unbalanced voltages by means of four-leg voltage source inverters. One technique, the EDSPWM, is new and is an extended version of the one proposed for three legs, whilst the other, called here SCPWM, was originally proposed from the use of sequence components. Moreover, it is analytically proved the complete equivalence between the two techniques. This was then showed through simulations and experimental implementations. Both techniques may be classified as scalar techniques and are of simple implementation. As opposed to the SCPWM, the EDSPWM directly imposes asymmetrical voltages on the phases without any symmetrical components



(a) Fundamental phase voltages for the EDSPWM. Vertical scale = $85V/div$.



(b) Fundamental phase voltages for the SCSPWM. Vertical scale = $85V/div$.

Fig. 11. Fundamental phase voltages.

separation. The results showed that both techniques presented good qualities regarding harmonic distortion and switching losses.

ACKNOWLEDGEMENT

The authors would like to thank Brazilian Research Council CNPq for providing financial support by means of project 481950/2009-5 and FAPESP project 10/01690-2.

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