

CONTROL OF UTILITY INTERFACES IN LOW-VOLTAGE MICROGRIDS

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Abstract – This paper presents a general control technique for utility interactive inverters in low-voltage microgrids. The Utility Interface (UI) is a three-phase power conversion unit, equipped with energy storage, which governs the interaction between the utility grid and the microgrid. The UI is in charge of several functions: in grid-connected operation, it performs as a voltage-supporting unit and compensates the reactive power, unbalance, and distortion caused by loads, whereas in islanded operation, it performs as a voltage-forming unit and sets the voltage and frequency for the entire microgrid. Moreover, the UI ensures seamless transitions from grid-connected to islanded operation and actively decouples the microgrid and the mains. Finally, the UI can perform as a centralized microgrid controller for distributed energy resources. The UI is therefore a crucial component, which needs to be analyzed carefully to ensure safe and reliable operation for the microgrid. This paper discusses a control approach that provides all required functionalities and ensures proper microgrid operation even in case of non-intentional islanding or severe load transients. The experimental results show the behavior of the system in different scenarios.

Keywords – Distributed Generation, Grid-connected Operation, Islanded Operation, Microgrid, Utility-interactive Inverter.

I. INTRODUCTION

The increasing penetration of Distributed Energy Resources (DERs) interfaced with the distribution grid through intelligent power processors poses new operational problems and, at the same time, enables new efficient operating regimes for low-voltage microgrids. The challenge of efficiently integrating every kind of DER increases the complexity of microgrid management, and calls for proper control strategies to ensure efficiency, autonomy, flexibility, reliability, and stability of the microgrid [1], [2].

Figure 1 shows a general microgrid structure, including N active nodes, M passive nodes, and the Utility Interface (UI). Each active node hosts an energy-supplying device, either a Distributed Generator (DG) or an Energy Storage (ES) unit, and an Energy Gateway (EG), which controls the active and reactive power flow to the grid. The EGs include a grid-interactive inverter and a local control and communication unit. According to grid connection standards [3], DERs should not regulate the voltage at their point of connections,

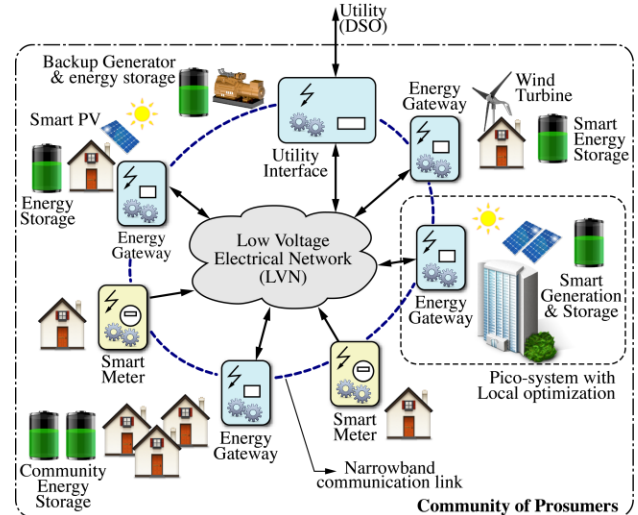


Fig. 1. General microgrid structure.

so that EGs typically perform as *current sources*, emulating high dynamic impedance at their outputs.

The passive nodes include only loads, and are not necessarily endowed with any particular kind of intelligent measurement or control device.

In this paper, the UI includes a three-phase grid-interactive inverter and an ES unit. The UI inverter is permanently controlled as a *voltage source* and performs as a grid-supporting device in grid-connected operation and as a grid-forming unit in islanded operation. The UI may perform as the master controller (MC) in any centralized control strategy applicable to microgrids.

An Information and Communication Technology (ICT) infrastructure provides the communication link between UI and EGs, thus enabling coordinated operation of all DERs.

This paper analyzes in detail the role, model, and design of the UI, proposing a multi-functional control approach for centralized microgrid strategy. The devised control system is experimentally tested on a laboratory-scale prototype.

II. ROLE OF THE UTILITY INTERFACE

In the structure of Figure 1, the role of the UI is crucial to assure smooth operation of the microgrid [4], [5] and to solve some open problems, like for example, the management of black starts when the microgrid starts up without grid support, and non-intentional transitions to islanded operation.

The typical structure and connection of the UI is shown in Figure 2.a. It is located at the Point-of-Common-Coupling (PCC) between the utility grid and the microgrid (i.e., at the output terminals of the step-down power transformer feeding the distribution network). The UI is made up of: a three-phase grid-connected inverter with line-side *LC* filter, aiming

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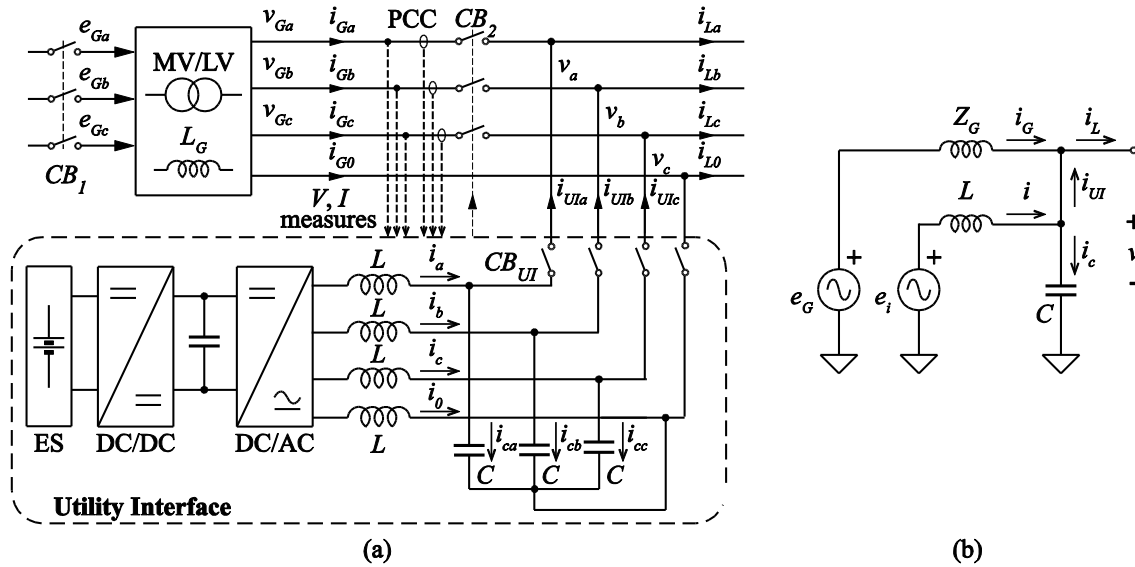


Fig. 2. Utility interface connected at PCC: (a) typical UI set-up; (b) equivalent single-phase representation.

at ensuring low harmonic content in the produced voltage and low high-frequency impedance; an energy storage device (e.g., a battery) equipped with a bidirectional power processor able to control the energy in- and out-flow to the battery/grid; and, possibly, a master control unit endowed with communication module, which collects data from the utility and the whole microgrid and processes control commands for the UI itself and for the distributed EGs [6].

In the following, we discuss a multi-functional control approach that provides all needed UI features, namely:

- in grid-connected operation, it performs as a grid-supporting voltage source, capable to compensate the reactive, unbalance, and distortion current terms drawn by the loads; it therefore performs like a shunt Active Power Filter (APF) that aims to compensate current disturbances;
- in islanded operation, it performs as a grid-forming voltage source, providing voltage and frequency references for the entire microgrid; it therefore performs as a conventional Uninterruptible Power Supply (UPS), which ensures voltage supply even during grid faults;
- during transitions from grid-connected to islanded, and vice-versa, it performs as an active smoothing device, ensuring seamless transitions even under non-intentional islanding;
- during changes of load and/or supply, it performs as an active decoupling device, avoiding perturbations to propagate from load to supply and vice-versa.

If compared with other devices known in the literature, it is possible to point out some advantageous features with respect to: 1) *hybrid voltage and current mode controls* [7], [8], which must switch between control modes; 2) *usual line-interactive UPS systems* [9], which present only some specific functionalities, and 3) *indirect current controls*, where no provisions are taken to control the grid current harmonics under heavily distorted mains voltage [4], [5].

III. UTILITY INTERFACE CONTROL PRINCIPLE

For simplicity, let us consider the equivalent single-phase (phase-to-neutral) representation of the UI shown in

Figure 2.b. The mains supplies AC voltage e_G through an impedance Z_G , and the UI inverter feeds AC current i through filter inductance L . This current is partially absorbed by shunt filter capacitor C (i_c), and partially flows to the PCC (i_{UI}), where load current i_L is drawn.

A voltage control loop is therefore needed, complemented by a fast internal inductor current loop to improve dynamic response and prevent overcurrents. A slow external grid current loop is also needed that, in the long term, adjusts the inverter currents so as to compensate disturbing effects from the load (reactive power, harmonic, and unbalance). Moreover, due to the low impedance of shunt capacitors C at high frequency, the UI can filter out a large part of the current harmonics generated by nonlinear loads and semiconductor switching.

An equivalent single-phase scheme of the UI control, including the three control loops, is sketched in Figure 3. The outer grid current loop may have a limited bandwidth (a few Hz) and enforces line current i_G to track reference i_G^* at low frequency, thus allowing control of power flow at PCC and unbalance compensation. The intermediate voltage loop has a wider bandwidth (a few hundred Hz), and enforces phase voltage v to track reference v^* in the mid-frequency range, thus providing the voltage source functionality required by the UI. The inner inductor current loop has a large bandwidth (a few thousand Hz), and enforces inverter current i to track reference i^* in the high-frequency range, providing prompt reaction to load and line transients.

Note that actual voltage reference v^* is obtained from ideal voltage reference e^* by subtracting voltage correction Δv^* , which is derived on the basis of the line current error $\varepsilon_{iG} = i_G^* - i_G$.

The proposed control architecture allows soft transitions from grid-connected to islanded operation. To this purpose, it is sufficient to set line current reference i_G^* to zero; within the time response of the external loop, the line current vanishes and the voltage loop brings the PCC voltage at reference value e^* . In case of non-intentional islanding the behavior is the same, with the additional time delay required to detect line current zeroing.

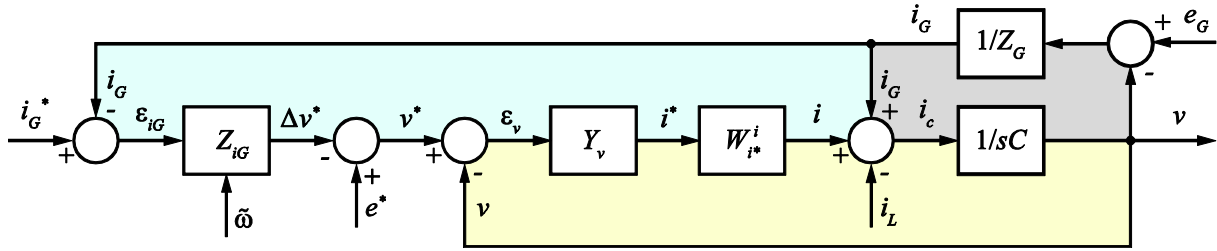


Fig. 3. Block scheme of UI control. Upper-left area: outer grid-current control loop; lower-right area: voltage control loop; upper-right area: LC resonant loop.

In general, the proposed control performs as follows:

- In grid-connected operation, the output UI voltage v is adjusted to enforce line current i_G to track reference i_G^* . If i_G^* is properly chosen (e.g., purely sinusoidal positive-sequence or normalized instantaneous PCC voltage), a slow control action occurs, which removes the reactive and unbalance currents at the fundamental frequency, thus, improving the power factor at PCC. Besides, if the grid current control loop is fast enough, the voltage correction Δv^* drives the inverter to compensate for harmonic currents too, thus reducing the Total Harmonic Distortion (THD_{iG}) at PCC.
- In islanded operation, error signal ϵ_{iG} vanishes, so that voltage correction Δv^* is brought to zero and inverter voltage reference v^* coincides with e^* . Therefore, the UI keeps the PCC voltage at the specified amplitude and frequency. Controller Y_v must damp the oscillations caused by the resonance of filter capacitor C with line inductance L_G . Moreover, it must provide enough control bandwidth to preserve the voltage purity at PCC in spite of load current harmonics.
- The transitions from grid-connected to islanded operation run smoothly since control discontinuities are prevented. In fact, voltage correction Δv^* is driven to zero as soon as islanding is detected.

IV. TRANSFER FUNCTIONS AND CONTROL DESIGN

A. Transfer Functions

In order to design the controllers, the main transfer functions of the block scheme in Figure 3 are determined. Let us consider first the resonant loop shown in the upper-right part of Figure 3 (grey area). We derive the transfer functions from input i to outputs v and i_G in the form G_{in}^{out} :

$$G_i^v = \frac{Z_G}{1 + sZ_G C} \quad (1)$$

$$G_i^{iG} = \frac{1}{1 + sZ_G C} \quad (2)$$

Then, we close the voltage control loop (yellow area) and determine the closed-loop transfer function between input v^* to output v in the form H_{in}^{out} :

$$H_{v^*}^v = \frac{Y_v W_{i^*}^i G_i^v}{1 + Y_v W_{i^*}^i G_i^v} \quad (3)$$

where $W_{i^*}^i$ is the closed-loop transfer function of the inner inductor current control loop. As discussed in [10], $W_{i^*}^i$ can be modeled by a low-pass filter or a pure delay. The effect of the static gain and cut-off frequency parameters of $W_{i^*}^i$ are analyzed in Figure 17 of Appendix.

Finally, the closed-loop transfer function of the outer grid current control loop can be expressed in the form W_{in}^{out} as:

$$W_{iG^*}^{iG} = \frac{Z_{iG} H_{v^*}^v}{1 + \frac{Z_{iG} H_{v^*}^v}{Z_G}} \quad (4)$$

In (3) and (4), the terms Y_v and Z_{iG} are, respectively, the regulator of the intermediate voltage control loop and the outer grid current control loop. These regulators can be designed on the basis of the open voltage control loop and the open grid current control loop transfer functions.

Note that all transfer functions depend on line impedance Z_G , which can be measured *off-line* or estimated from the short circuit impedance of MV/LV transformer and distribution line impedance.

B. Control Design

On the basis of the previous considerations, it is possible to show that by proper design of control parameters and selection of current and voltage references, the UI can provide all the aforementioned features. In general, the control of multi-functional grid-connected converters for microgrid applications is a delicate subject. The main aspects to be tackled in the design are steady-state accuracy, large-signal dynamic response, robustness stability, and grid synchronization [11], [12]. Various approaches addressing the various aspects have been analyzed in the literature [11], [12]. In [13] is shown that, for a voltage controlled Voltage Source Inverter (VSI), a Proportional Integral Derivative plus resonant (PID + R) controller provides satisfactory behavior over a wide range of operating modes, whereas grid current feed-forward and load current feed-forward can degrade stability in particular load conditions. Instead, [14] proposes the analysis and design of Synchronous Reference Frame Controllers (SRFC) applied to single-phase VSIs. Though the advantages of this approach are, in general, still not well defined, the paper shows that SRFC, combined with capacitor current active damping, grid voltage feed-forward, and multi-resonant harmonic compensation, can lead to effective solutions. In [15], [16], the H^∞ design approach combined with repetitive controllers is applied for robust control of grid-connected voltage-controlled VSIs. As concerns grid

synchronization, new Phase Locked Loop (PLL) free synchronization strategies have been recently proposed and implemented [17], [18]. Nevertheless, solutions based on conventional PLL still attract interest for their flexibility.

In this implementation, we took advantage of a fixed frequency digital hysteresis controller, detailed in [19], for the inner inductor current control loop and a Proportional-Integral (PI) regulator for the intermediate voltage loop. Controller Z_{iG} is implemented as in Figure 4 [20], and integrates a PI plus resonant controller (PI + R). The resonant controller R is tuned to grid frequency to minimize the steady-state tracking error up to seventh harmonic component, as in Figure 4.

Finally, a natural (abc) reference frame PLL [21] is used to estimate the fundamental angular frequency ω_l for automatically tuning the resonant controller $R(s)$.

For the design of regulators Y_v and Z_{iG} , shown in Figure 3, let us consider the worst condition (i.e., no-load operation in islanded mode). In this condition, for the design of voltage regulator Y_v , a suitable PI controller can be devised. Notice that the transfer function G_i^v in islanded operation depends only on capacitor C , because $|Z_G| \rightarrow \infty$. Once Y_v is designed, its performance must be verified also in the grid-connected case. Figure 5 shows the Bode plots of the open loop gain obtained by a PI regulator with target phase margin of 70° and crossover frequency of 1.3 kHz, during both operating modes with no load.

At this point, it is possible to define the regulator Z_{iG} of the external grid current control loop. To this end, we refer to the external open loop transfer function without Z_{iG} :

$$\frac{H_{v*}^v}{Z_G} = \frac{Y_v W_{i*}^i G_i^v}{1 + Y_v W_{i*}^i G_i^v} \cdot \frac{1}{Z_G} = \frac{Y_v W_{i*}^i G_i^{iG}}{1 + Y_v W_{i*}^i G_i^v} \quad (5)$$

For the selection of the regulator, we note firstly that the considered control loop has to fulfill two targets. The main one is to control the power flow at PCC, which is accomplished by $PI(s) + R_1(s)$; the second, ancillary, is to compensate the harmonic currents at PCC in the steady-state, which is accomplished by $R_{2,3,4,5,7}(s)$. The implementation of this controller is shown in Figure 4 and has the form described in [20], yielding:

$$P(s) + I(s) + R(s) = K_p + \frac{K_{I0}}{s} + \sum_{h=1,2,3,4}^{5,7} \frac{K_{Ih} \cdot \omega_b \cdot s}{s^2 + 2\omega_b s + (h \cdot \omega_l^2)} \quad (6)$$

where ω_b is the resonant bandwidth. Note that ω_l can be adjusted to effectively tune the filter resonances to grid frequency. Figure 6 shows the open loop gain of the outer grid current control loop, where ω_b is set to 4.1 rad/s. The stability of the system can be verified by inspection of the Nyquist plot [22]. From this standpoint, it is important to take into account the effects of discretization method and computational delay on the implementation and performance of resonant controllers, since they are very sensitive to resonant frequency accuracy [23]. Appendix discusses the system stability in grid-connected operation for different values of Z_G .

C. Discussion of DC Side Design of UI

The DC side of an UI may be endowed with an ES unit (battery and/or super-capacitor) and, if needed, a backup generator (micro-turbine, fuel cell, diesel gen-set). The former is used for prompt and short-term response, whereas the latter is for prolonged islanded conditions. The design of the DC side resource is strictly related to the specific microgrid application, grid standard requirements, and user needs. On the basis of these specifications, the ES unit and backup generator of the UI can be properly designed. Due to its complexity, this aspect should be specifically tackled and it is not further addressed herein.

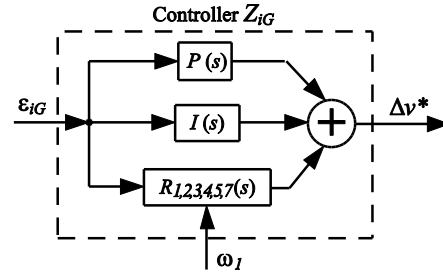


Fig. 4. Continuous time equivalent dynamic model of the adopted PI plus resonant controller.

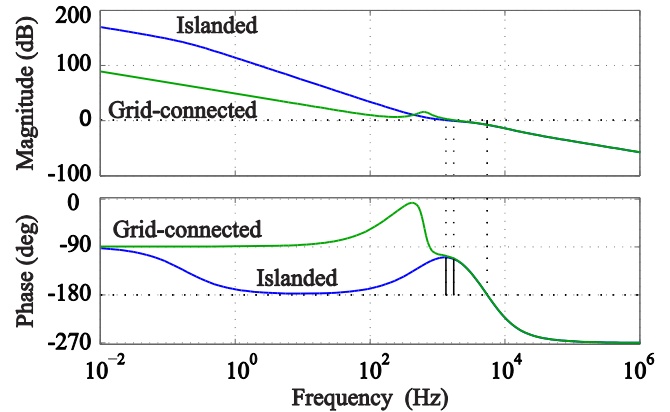


Fig. 5. Open loop gain of voltage control loop.

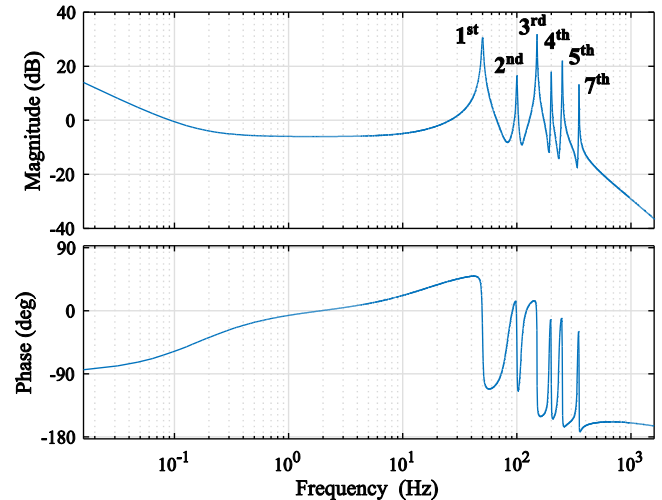


Fig. 6. Open loop gain of outer grid current control loop.

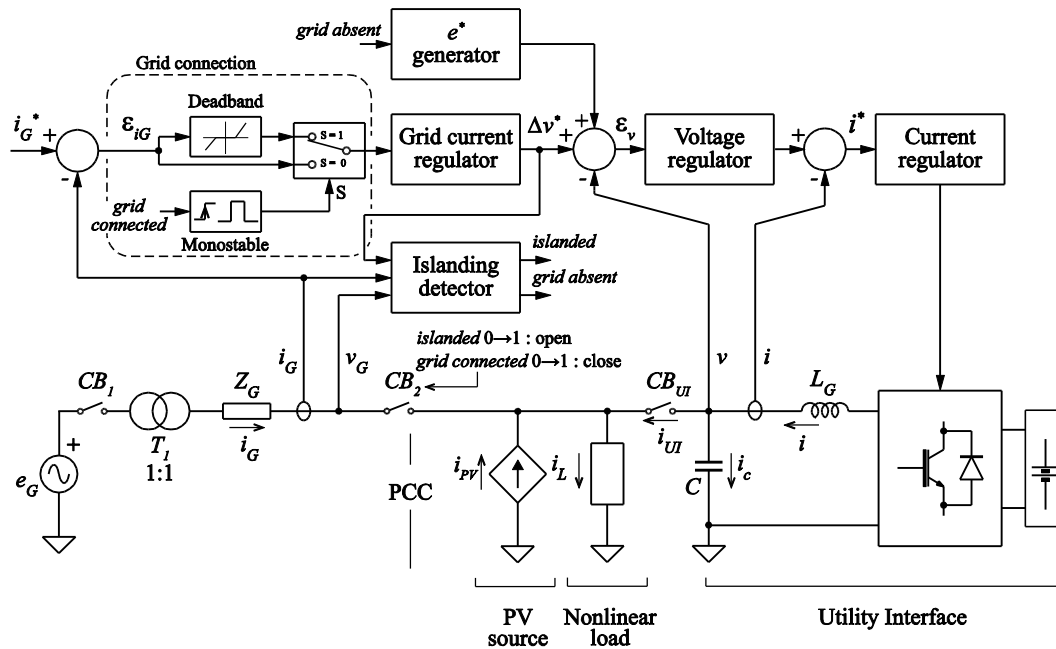


Fig. 7. Block diagram of the case study test-bench, with power circuit, control scheme and transition management.

V. CASE STUDY

Besides the inductor current, voltage and grid current regulators discussed in the previous sections, the final set-up of Figure 7 employs also an islanding detection and grid connection blocks. As usually done, the islanding detection senses utility grid disconnection or abnormal operation, while the grid connection block prevents high inrush currents at the connection process and guarantees a non-saturated operation of Z_{iG} . Indeed, while Z_{iG} should be active at the connection with the mains to keep control on grid current i_G , the actual status of the grid depends on the response delay of electromechanical circuit breaker CB_2 (typically ranging from tens to thousands of milliseconds), that is, generally unknown. During the clearing time, the regulator Z_{iG} operates in open loop: it reacts to spurious error signals introduced by the hardware, which can cause saturation. To alleviate these problems the connection block ignores the current error ε_{iG} below a suitable threshold, which is removed once the time response of CB_2 is elapsed. This allows both to limit inrush currents exceeding the deadband and to prevent spurious signals to perturb the regulator while CB_2 has not yet finalized the committed reclosure.

The waveform of the supply reference i_G^* is set to be proportional to v_G , performing a resistive load synthesis compensation, and to draw the full load power from the utility. The set-up parameters are detailed in Table I.

A. Experimental Results

An experimental realization of the case study shown in Figure 7 was developed to verify the actual behavior of the final system. Figure 8 shows a picture of the experimental laboratory-scale prototype of UI. The digital control scheme was implemented in a cRIO platform from National Instruments. These paragraphs report the obtained results. In particular, the system operation was investigated in the following operating conditions.

TABLE I
Testbed Circuit Parameters

Parameter	Description	Value
V_{rated}	Nominal grid voltage	230 V_{rms}
L_G	Grid inductance	0.60 mH
R_G	Grid resistance	0.15 Ω
f_{rated}	Nominal grid frequency	50 Hz
A_{UI}	UI power rating	3 kVA
L	LC filter inductance	1.20 mH
C	LC filter capacitance	100 μF
P_{Lrated}	Nominal load power	2 kW
CF_{iL}	Crest factor of load current	2 ---

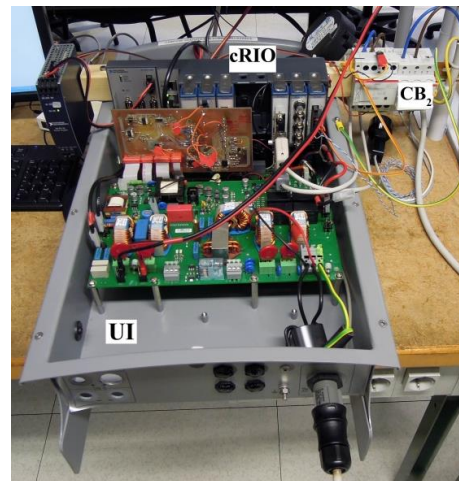


Fig. 8. Laboratory-scale prototype.

1) *Islanded operating mode* - A programmable electronic load absorbing 2.0 kW with crest factor $CF = 2$ is connected to the set-up. The photovoltaic (PV) source is not providing power, due to weather condition. Figure 9 shows grid voltage v_G , UI voltage v , and the current absorbed by the local load i_L in steady-state conditions. We notice that the UI manages to feed the load with an adequate voltage quality v ($THD_v = 2.6\%$) and synchronized with the grid voltage for a possible smooth and prompt transition to grid-connected operation.

2) *Grid-connected operating mode* - Figure 10 shows the system response at the connection of a nonlinear load during grid-connected operation with zero grid current reference ($I_G^* = 0$). In these conditions, an ideal operation would require a constant zero current flow at PCC. Due to the finite time response of grid current regulator Z_{iG} , the behavior shows a small transient on i_G during the connection.

The steady-state behavior during grid-connected operation is shown in Figure 11. The acquired waveforms of the voltage mains v_G , UI voltage v , current exchanged with the main grid i_G , and current exchanged with the UI i_{UI} are reported, while the current reference I_G^* is equal to $7.5 A_{RMS}$. The THD of the PCC voltage and the grid current are respectively, $THD_v = 0.6\%$ and $THD_{iG} = 2.8\%$.

The same measurement is performed also with 5% of third harmonic present on grid voltage v_G . As expected, in this situation, the grid current is correspondingly distorted due to the proportional relation between grid voltage and grid current (resistive load synthesis compensation). The acquired

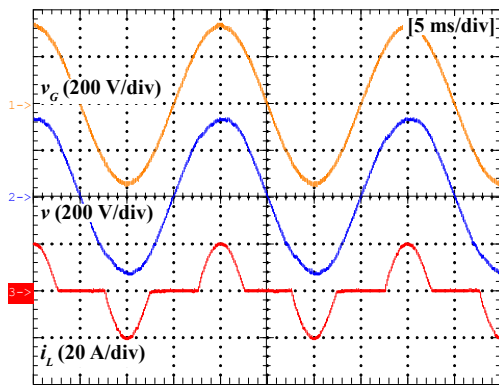


Fig. 9. Isolated operation with non-linear load.

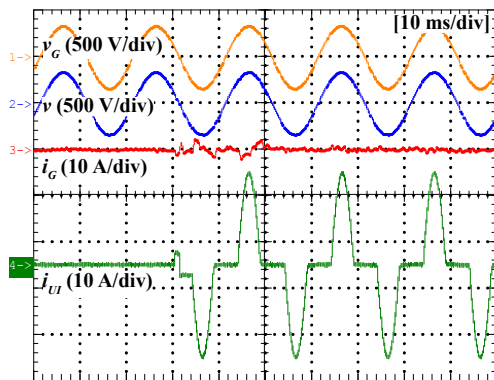


Fig. 10. Connection of non-linear load during grid-connected operation.

results are reported in Figure 12, whereas the steady-state amplitudes and THD levels are reported in Table II.

3) *Transition from islanded to grid-connected mode* - Figure 13 shows the behavior during a transition to grid-connected operating mode. In particular, grid voltage v_G , UI voltage v , UI current i_{UI} , and grid current i_G are shown along the main steps of the connection process. First, we remark the absence of any inrush current at the connection instant; due to the adopted deadband-based connection technique (see Figure 7). Secondly, the voltage provided by the UI is well synchronized with grid voltage, thus v maintains smooth and with desired amplitude around the transition. The grid connection process completes when the deadband period is elapsed. Finally, the amplitude of i_G^* is changed progressively with a suitable slew-rate. A zoomed-in view around the connection instant is reported in Figure 14. In the considered case, deadband duration is set equal to 1 s, though shortest values can be selected.

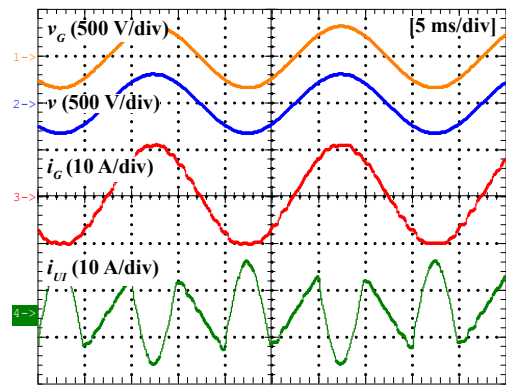


Fig. 11. Grid-connected operation with non-linear load ($THD_{vG} = 0.5\%$).

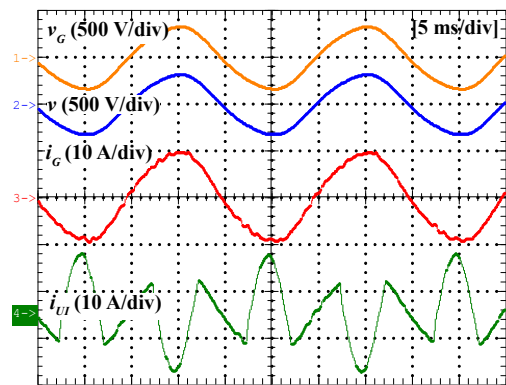


Fig. 12. Grid-connected operation with non-linear load ($THD_{vG} = 5\%$ of 3th harmonic).

TABLE II
Steady-state Results from Experimental Set-up

	Islanded, no load	Islanded, with load ⁽¹⁾	Grid conn., no load	Grid conn. + load ⁽¹⁾	Grid conn. + load ⁽¹⁾ + 5% 3 th harm.
v_G [V] / THD_{vG} [%]	237 / 0.5	237 / 0.5	244 / 0.5	232 / 0.6	233 / 4.6
i_G [A] / THD_{iG} [%]	0 / ---	0 / ---	10.3 / 1.8	7.5 / 2.8	6.7 / 7
v [V] / THD_v [%]	237 / 0.2	236 / 2.6	258 / 0.4	223 / 0.7	224 / 4.5
i_{UI} [A] / THD_{iUI} [%]	0 / ---	10.2 / 61.9	10.3 / 1.8	4.45 / 360	3.85 / 230
i_L [A] / THD_{iL} [%]	0 / ---	10.2 / 61.9	0 / ---	10.2 / 61.9	10.2 / 61.9

⁽¹⁾ Programmable electronic load absorbing 2 kW of active power with a crest factor of 2.

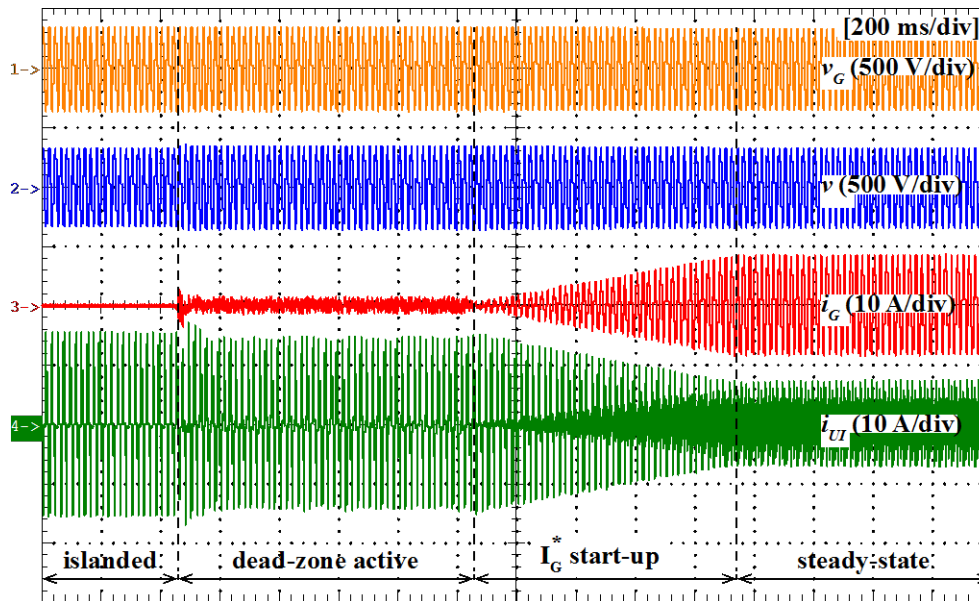


Fig. 13. Transition from islanded to grid-connected operating mode.

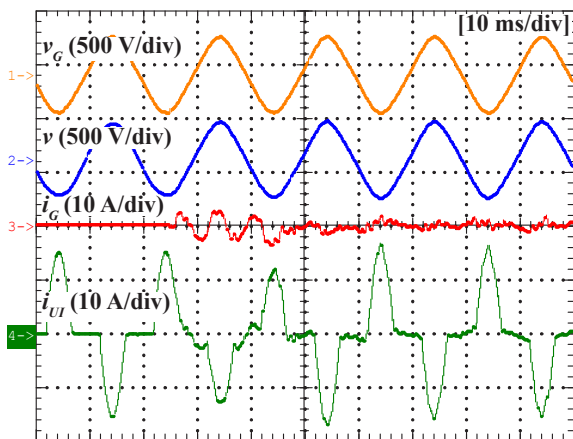


Fig. 14. Zoomed-in view around the connection showing in Fig. 13.

4) *Transition from grid-connected to islanded mode* - In this case, a commercial, fully compliant, PV inverter is connected to the PCC to verify that the management strategy of the UI succeeds in ensuring a seamless operation of small PV systems also under intentional and non-intentional islanding transitions.

In Figure 15, the PV source extracts approximately 0.4 kW from an array of PV panels and a programmable electronic load absorbs 1 kW with $CF = 2$. In this case, it is assumed that, due to a pre-scheduled procedure (e.g., microgrid maintenance) the UI undertakes an intentional islanding. The intentional islanding procedure commands the circuit breaker CB_2 to open and, simultaneously, sets the grid current reference to zero and activates the deadband control. After the circuit breaker CB_2 opens, the grid current regulators are reset to their initial condition till the arrival of a grid connection command. As can be observed in Figure 15, the intentional islanding happens seamlessly: the voltage provided by the UI adapts smoothly, so that the PV does not notice the transition, maintaining an unperturbed operation along the event.

We consider now the transition to islanded operation due to unpredictable events, (i.e., non-intentional islanding). In this case, the local nonlinear load absorbs 2 kW with $CF = 2$,

and the power injection from the PV inverter is nearly to 0.8 kW. Then, the circuit breaker CB_1 is opened and the microgrid loses the utility grid, undergoing a non-intentional islanding. In this condition, the UI must firstly detect the islanded operation and then, set I_G^* to zero. However, as it is always controlled as a voltage source, the UI automatically becomes the grid-forming device of the islanded microgrid, providing an adequate grid voltage for the islanded system.

The acquired waveforms are reported in Figure 16. Also in this case, we remark a seamless transition to islanded operation, that occurs unnoticed by the PV inverter. Table II allows to compare the results obtained from the experimental tests in terms of total harmonic distortion. The experimental results have shown acceptable distortion values, even under nonlinear load and distorted utility grid

VI. CONCLUSION

A control approach for the power converter (Utility Interface) interfacing the utility grid and the microgrid has been presented, which provides all needed operational features both in grid-connected and islanded operation. The control is devised to provide maximum power quality during grid-connected operation, effective voltage stabilization during islanded operation, and smooth transitions between the two operating modes. For these capabilities, the proposed solution meets the requirements of most demanding grid codes. As an additional benefit, the utility interface can also act as master controller for distributed power sources acting in a centralized microgrid. The proposed solution was experimentally tested through a prototype, and a basic application example was taken into account to show the control features in a significant case study. All tests have shown satisfactory results.

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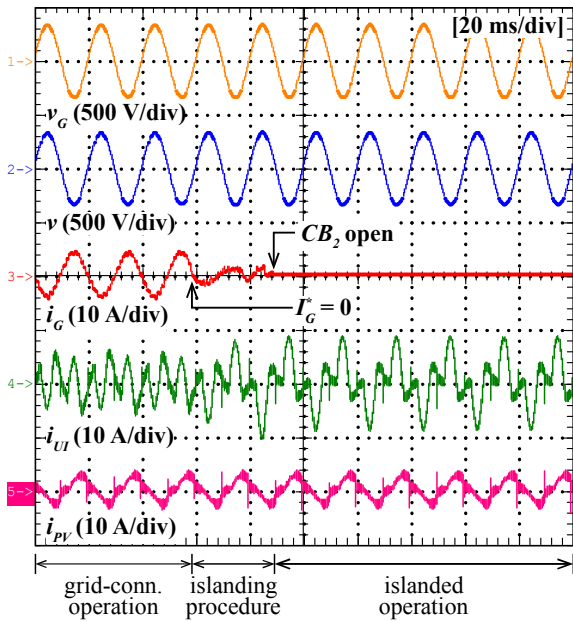


Fig. 15. Intentional transition to islanded operation.

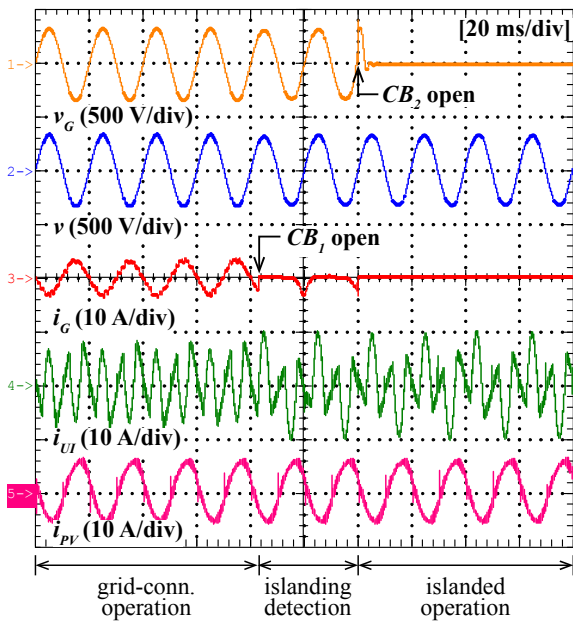


Fig. 16. Non-intentional transition to islanded operation.

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APPENDIX

A. System Stability in Islanded Operation

The effectiveness of the voltage control loop is crucial while the UI operates islanded from the mains. Therefore, the voltage control loop is here evaluated considering such mode of operation, in the worst loading condition (i.e., no-load). Figure 17 reports the poles and zeros of (3) assuming a low-pass filter behavior for W_{i*}^i . The poles and zeros are plotted for different values of static gain and cut-off frequency. The static gain assumes values from 0.5 to 1.5 with steps of 0.1, while the cut-off frequency assumes values, 1 kHz, 2 kHz, and 4 kHz. We observe that the static gain of W_{i*}^i affects the damping of the system, whereas that slower current controller's dynamics affect both damping and decay ratio. Noticeably, there are no poles at the right-half plane.

B. System Stability in Grid-connected Operation

To analyze the external grid current control loop, the poles and zeros of (4), varying L_G from 0.2 mH to 2 mH with steps of 0.2 mH and R_G from 0.1 Ω to 1 Ω with steps of 0.1 Ω , are shown in Figure 18. A zoomed-in view of Figure 18 is provided in Figure 19. No poles at the right-half plane are present for the considered range of values.

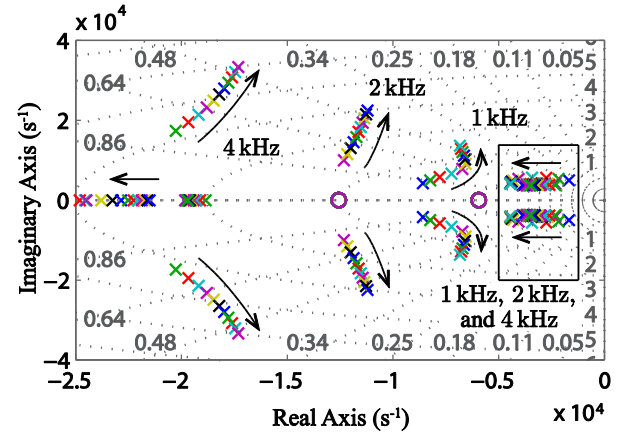


Fig. 17. Poles (crosses) and zeros (circles) of H_v^v in (3) with different static gains and dynamics for W_{i*}^i .

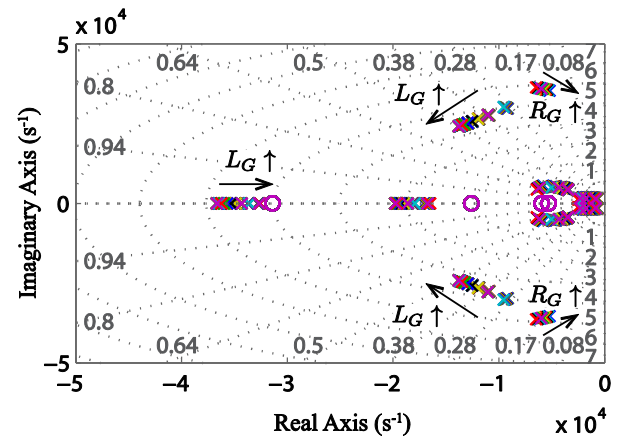


Fig. 18. Poles (crosses) and zeros (circles) of W_{i*}^{iG} in (4) for different values of L_G and R_G .

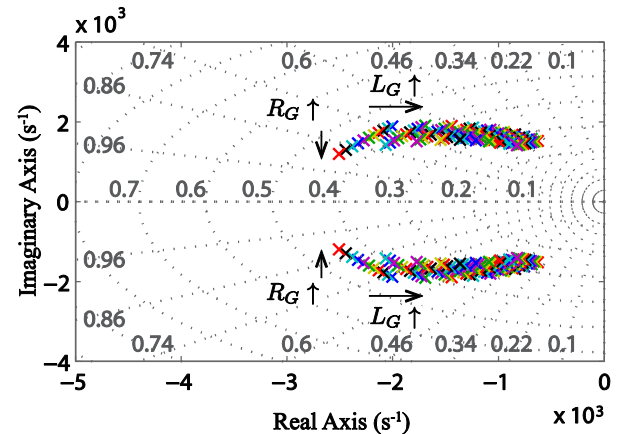


Fig. 19. Zoom-in view of resonant poles and zeros of Figure 18.

BIOGRAPHIES

Paolo Tenti is professor of Electronics at the Department of Information Engineering of the University of Padova, Italy. His main interests are industrial and power electronics and electromagnetic compatibility. His research focuses on application of modern control methods to power electronics, EMC analysis of electronic equipment and cooperative control of distributed electronic power processors in smart

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