THREE-PHASE ACTIVE POWER FILTER BASED ON THE FOUR STATES COMMUTATION CELL DC-AC CONVERTER: DESIGN AND IMPLEMENTATION

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***Abstract* — This work approaches the subject of Active Power Filtering for the cases where the current stress of the semiconductor devices is a point of major concern. Instead of the classic parallelism of inverters, a topology with coupled inductors is proposed to address this problem. In addition, this topology provides advantages from the point of view of the output current ripple, providing more flexibility on the design of the filter inductors. A more simple and cost-effective control strategy based on the sensing of the AC source currents is implemented using the Park transformation. Simulation and practical experiments are presented in order to prove the correct behavior of the system. The experimental set-up consists on a nonlinear load rated for 8 kVA connected to a 380 V (line-to-line) AC grid, through an isolation transformer. A Four States Commutation Cell, DC-AC Converter is connected as a shunt Active Power Filter with a DC link voltage of 600 V. The control algorithm is programmed on a DSP board TMS320F28335 from Texas Instruments.**

***Keywords* — Active Power Filtering, Coupled Inductors, Four State Commutation Cells.**

I.INTRODUCTION

In the last decades the number of nonlinear loads has increased with a very rapid rate. The use of electronic equipments, variable speed drives and others have played an important role in this scenario. From the utility point of view this means an increased reactive power and harmonic current circulation with several unwanted consequences. The most straightforward solution would be the use of passive filters; nonetheless there are a few characteristics that turn this into a costly and non-efficient solution. To name a few: volume, resonance issues and limited range of harmonic tuning capability. The Power Factor Correctors (PFC) are also implemented to mitigate the utility current degradation, specifically with electronic equipments where the use of rectifiers is mandatory. The PFC is an intermediate converter stage where the input AC current is shaped to follow a sinusoidal reference; this means the converter is on the path of the load power transfer so it must be rated for nominal parameters and its power losses must be seriously taken into account. The concept of Active Power Filtering (APF) represents a very popular counterpart to the passive filtering approach. The APF basic principle was originated as early as the 1970´s decade. Since that date a very wide range of publications has arises addressing this topic [1]-[7]. The shunt APF is probably the most widespread configuration [1]-[11]. As shown in Figure 1 the shunt APF consists on a converter which is modulated in order to inject a current containing the reactive and harmonic components, so the load/filter combination is seen from the grid as a resistor.

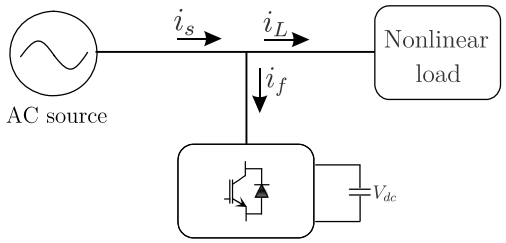

Fig. 1 Basic representation of the shunt APF connected to nonlinear balanced load.

The scenario where high power is transferred at medium and high voltage levels is very well documented on the use of multilevel topologies for these applications [12]-[18]. Less attention is paid to applications where the current stress of semiconductors is dominant [19], [20]. In [19] a topology based on parallel interleaved inverters is proposed, allowing reduced current stress in addition to reduced current ripple on the filter inductors. The problem of zero sequence current circulation due to parallelism of inverters is addressed by means of a common-mode inductor connection.

This paper shows a different approach in which the four-state commutation cells topology proposed in [21] is adopted. By means of this topology the current been conducted by the power switches is reduced to one-third of the total phase current, additionally the phase voltage of the inverter possesses three different levels and a commutation frequency equal to three times the carrier frequency, leading to a reduced size of the filter inductor. The control strategy is implemented on the dq0 axis sensing only the grid currents, this means that there is no need for reactive and harmonic current calculation. Such a strategy, compared with strategies where three more sensors are needed in order to generate

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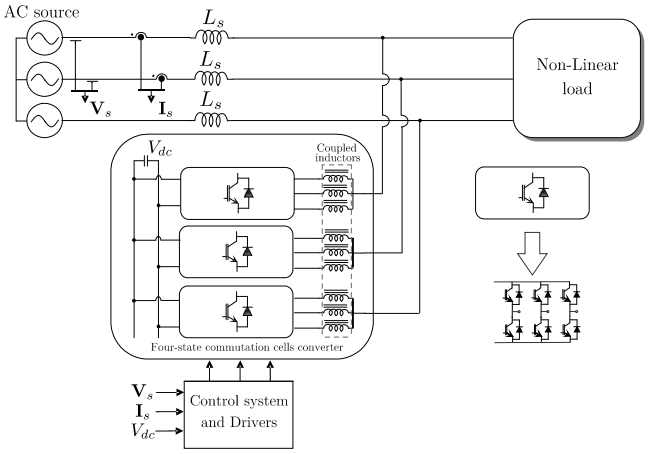

Fig. 2. Shunt APF with four-state commutation cell converter.

reference currents, allows not only simplicity and low computational effort, but also cost reduction. Figure 2 shows a general sketch of the system using the inverter with four-state commutation cell as APF.

II.THE FOUR-STATES COMMUTATION CELL INVERTER

A. Operation Description

The use of coupled inductors and interleaved PWM scheme is reported in [30]-[32]. The four-state commutation cell inverter, proposed in [21], is shown in Figure 3. This topology is composed of three cell-converters, one for each phase. It can be seen that Cell A, B and C corresponds with a three-phase bridge converter and at the output of every cell a three-phase coupled inductor is connected. The neutral point connection of the coupled inductors is used as the phase terminal. Every cell shares the same DC-link. The use of the three-phase coupled inductor allows the division of the load phase current through the switches, in a balanced way so that the current in each arm of the structure is equal to 1/3 of the load current in one phase, reducing the current values for the switches [33]. It is important to note that these coupled inductors are subject only to high-frequency flux, being zero the flux associated to the load current, this implies a reduced size of these elements. The modulator implemented for this topology is detailed in the next session.

Analyzing the eight possible switching states of each cell-converter is possible to obtain the corresponding voltage of each phase. This is shown in Figure 4 and summarized in Table I. As it can be seen from Table I, some of the eight switching states result in redundant voltage levels, therefore the number of different commutation states of each phase is four.

B. Modulator

Each PWM modulator is composed of three symmetric triangular carriers shifted by 120°, being compared with a sinusoidal modulating signal. The three modulating signals corresponding to each phase are shifted 120° among them. Figure 5 depicts the carrier and modulating signals, signals, in addition to the resulting gating signals and phase voltage.

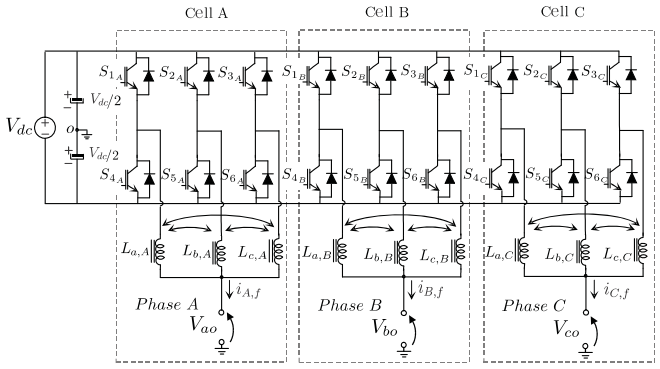

Fig. 3. The three-phase four-state commutation cell converter.

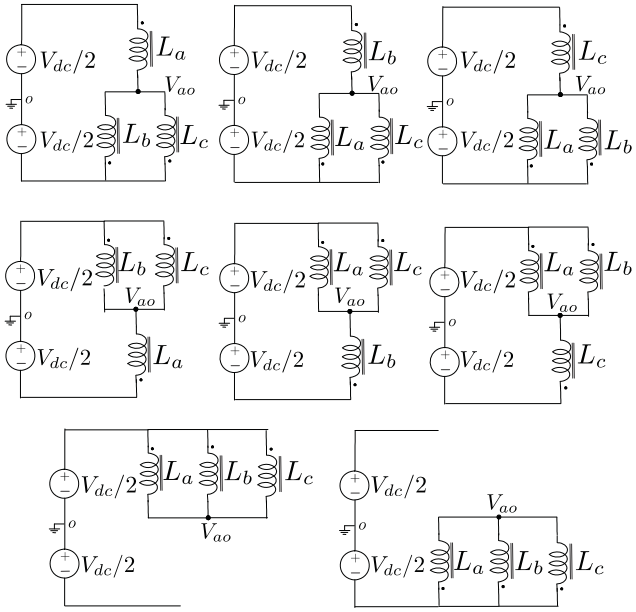

Fig. 4. Eight possible switching states of phase A.

TABLE I
Phase *a* Voltage for the Eight Switching States of the Inverter

Switching state	Coupled Inductors Voltage			
	v_{L_a}	v_{L_b}	v_{L_c}	V_{ao}
1	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-\frac{1}{6}V_{dc}$
2	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$-\frac{1}{6}V_{dc}$
3	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-\frac{1}{6}V_{dc}$
4	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{1}{6}V_{dc}$
5	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$\frac{1}{6}V_{dc}$
6	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{1}{6}V_{dc}$
7	0	0	0	$+\frac{1}{2}V_{dc}$
8	0	0	0	$-\frac{1}{2}V_{dc}$

It can be noticed that depending on the magnitude of the modulating signal, the converter operates in two different modes (valid for the positive half cycle). The first mode corresponds with Figure 5.a and in this case the phase voltage switches between $V_{dc}/6$ and $-V_{dc}/6$. The second mode corresponds with Figure 5.b and in this case the phase

voltage switches between $V_{dc}/2$ and $V_{dc}/6$.

In a sinusoidal PWM, the modulating signal is changing amplitude as a function of time, therefore the converter transitions from one operation mode to the other also as a function of time. The transition angle correspond to $\theta = \arcsin(\frac{1}{3M})$, where M is the modulation depth.

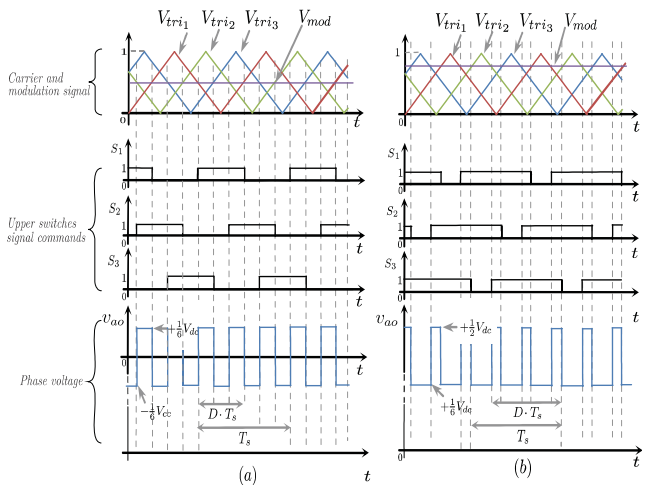

Fig. 5. Modulator, gate signals and phase voltage waveforms. (a) Operation Mode I. (b) Operation mode II.

III. DESIGN

A. Coupled Inductor

The most important aspect on the design of the coupled inductor is to obtain an inductance value in order to limit the magnetizing current ripple through these inductors. In consequence, a relationship between the magnetizing current ripple and the inductance should be found. Reference [22] describes a procedure based on averaging the coupled inductors voltage waveform (Figure 5), for both operation modes, during the positive cycle of the grid period. Afterwards, the averaged magnetizing current waveform is obtained and with this the current ripple can be calculated. The equations obtained are as follows:

$$\begin{cases} \Delta i_{Lm} = \dfrac{2V_{dc}}{9L_m f_s}, & \omega t < \theta \\ \Delta i_{Lm} = \dfrac{V_{dc}}{3L_m f_s}\left(1 - M\sin(\omega t)\right), & \theta < \omega t < \pi - \theta \end{cases} \quad (1)$$

where Δi_{Lm} is the ripple of the magnetizing current, L_m is the magnetizing inductance of the three-phase coupled inductors and f_s is the switching frequency.

If (1) is multiplied by the factor $\frac{L_m \cdot f_s}{V_{dc}}$ the normalized current ripple is obtained:

$$\begin{cases} \overline{\Delta i}_{Lm} = \dfrac{2}{9}, & \omega t < \theta \\ \overline{\Delta i}_{Lm} = \dfrac{1}{3}\left(1 - M\sin(\omega t)\right), & \theta < \omega t < \pi - \theta \end{cases} . \quad (2)$$

Figure 6 depicts the behavior of the envelope of current ripple on the three-phase coupled inductor for one-half of the line period with different modulation depth values. It is shown clearly that maximum current ripple occurs, for any value of modulation depth, when $\omega t < \theta$.

According to the previous analysis, the magnetization inductance should satisfy:

$$L_m = \frac{2}{9}\frac{V_{dc}}{\Delta I_{Lm,max} f_s} \quad (3)$$

where $\Delta I_{Lm,max}$ is the maximum allowed current ripple in these inductors.

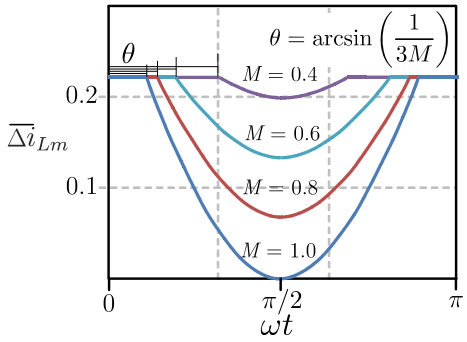

Fig. 6. Normalized envelope of magnetizing current ripple (variation for half a period of the line).

Another important issue on the inductor design is the one regarding the maximum flux-density variation, in order to avoid saturation of the magnetic core. The behavior of the flux density on the coupled inductors has the same format of the magnetizing current ripple. Thus this is only subjected to a high frequency component. Therefore, the expression of the peak-to-peak flux density ΔB_{max} corresponds with (4)

$$\Delta B_{max} = \frac{V_{dc}}{9NA_e f_s} \quad (4)$$

where A_e represents the cross-section area of the magnetic core and N is the number of turns.

B. Interface Filter Inductors L_s

The interface filter inductors play a key role on the APF. When facing the design of this element, a certain compromise must be reached. This inductor should be placed in series with grid. A very large inductor provides currents with reduced high frequency ripple but at the same time, the dynamic efforts are increased in order to follow rapid changes on the compensating currents reference and vice versa.

The multiple levels of the converter phase voltage, together with a phase voltage switching frequency of three times the PWM switching frequency (see Figure 5), allows for a considerable reduction of the filter inductors for the same requirements in terms of current ripple and dynamic response. In order to obtain the equations of the inductor current ripple, a procedure similar to the one previously described can be followed. The voltage applied to the filter inductor is dependant not only on the cell inverter phase

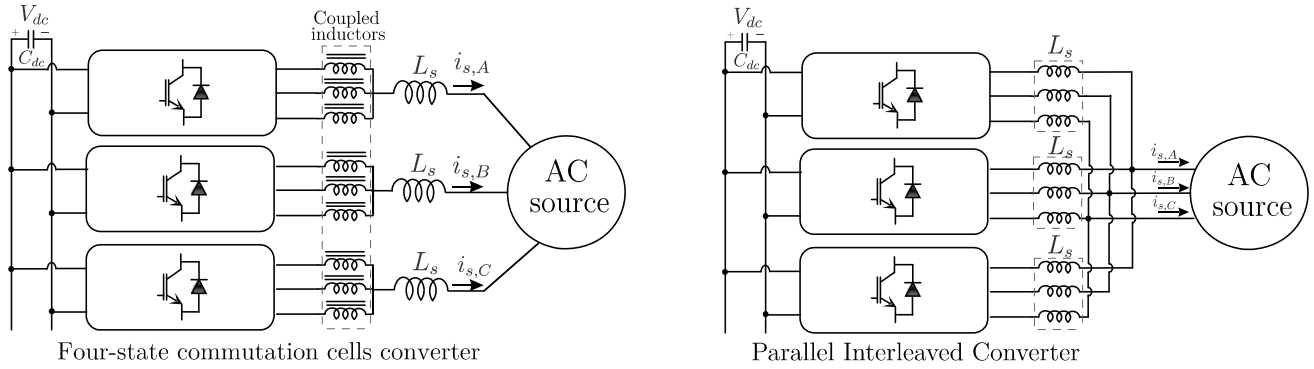

Fig. 7. Phase current ripple, case study topologies.

voltage but also on the three grid phase voltages. Equation (5) shows the inductance that limits the current ripple to a maximum value for three different modulation depth ranges, valid to sinusoidal modulation. It can be demonstrated that the maximum current ripple occurs for a modulation depth equals to 0.7698. If the inductance is calculated to limit the maximum ripple considering this value, then the condition will be satisfied for the entire range.

$$L_s = \begin{cases} \dfrac{V_{dc}}{\Delta I_{s,max} f_s} \dfrac{M}{24}(2-3M), & M \leq \dfrac{-2\sqrt{3}+6}{9} \\ \dfrac{V_{dc}}{\Delta I_{s,max} f_s} \dfrac{M}{36}\sqrt{3}, & \dfrac{-2\sqrt{3}+6}{9} < M < \dfrac{4}{9}\sqrt{3} \\ \dfrac{V_{dc}}{\Delta I_{s,max} f_s} \dfrac{(8-3\sqrt{3}M)}{108}, & \dfrac{4}{9}\sqrt{3} \leq M \leq 1\ . \end{cases} \quad (5)$$

In order to illustrate the advantage of this topology in terms of current ripple reduction, let us compare the high frequency components of the current being injected to the grid by the topologies shown in Figure 7. Clearly both topologies allows for a reduction of current stress which is a point of major concern. The simulation results are shown in Figure 8. In both cases SPWM is employed with the same modulation depth the same switching frequency and the same interface inductance L_s. For the case of three interleaved inverters, three symmetrical carriers shifted by 120° were compared with a set of three-phase modulating signals. $\bar{\Delta} i_{s,PIC}$ is the normalized current ripple of the Parallel Interleaved

Converter and $\bar{\Delta} i_{s,FSCC}$ is the normalized current ripple of the Four-State Commutation Cells Converter. With the described modulation strategies, both topologies present the same current-ripple waveform, only differing the amplitudes. A clear reduction of one-third of the current ripple can be observed for the Four-State Commutation Cells Converter.

It is important to clarify that even though the Four-State Commutation Cells Converter (FSCC) reduces the current ripple for the same inductance value, the inductor size would be higher if compared with the Parallel Interleaved Converter (PIC) because the current is three-times higher. Nonetheless, the total number of interface inductors is reduced to three.

An interesting aspect of the FSCC when compared with the PIC is the auto protection against cross-current phenomena among converters. It is widely reported on the literature the cross-current problem caused on the PIC by determined commutation states [19], increasing the semiconductor's losses. These currents are limited by the inductance L_s and the switching times on the PIC. For applications in active filtering a small inductance L_s value is required in order to compensate high di/dt in the drained currents by the load, however it increases the problem of cross-current on the PIC. The insertion of common-mode inductors reduces the circulating currents among the inverters; such a solution is described on [19].

Circulating currents also appears through the switches of adjacent branches connected to the same phase on the FSCC. However, these currents are limited by the self-inductance of the coupled inductors L_p. As the coupled inductor is built on a high permeability core without airgap, the obtained self-inductance is quite high, limiting the magnetizing current to a small value. Overall, the coupled inductors guarantee losses reduction without compromising the dynamic response of the system.

Figure 9 depicts the principle of current circulation in both topologies. Observing both the converters on this figure, it can be noticed that both operates under the same principle, differing only on the inductance which limits the circulating current. The magnetizing inductance of the coupled inductors in the FSCC is very large when compared to interface inductance in the PIC. It limits the effect of cross-current flow between the arms of the converters (see figure 9.). Therefore, there is a reduction of losses in semiconductors when the arms operate in interleaved.

C. DC-link Capacitor

The control strategy of the DC-link capacitor voltage is implemented in such a fashion that transient changes in the instantaneous power absorbed by the load generate does not produce substantial voltage fluctuations across DC capacitor [23]. It means that the capacitor must be chosen properly in order to limit this voltage fluctuation. In [19] and [23] expression for the capacitance is obtained following this criteria. In [24] the capacitance is calculated based on the reactive power been consumed by the load, switching frequency and maximum voltage ripple. Besides the capacitance value, voltage and current ratings of the capacitor must be properly evaluated. The RMS value of the current circulating through this capacitor is a very important quantity in order to estimate its useful life. There are three converters

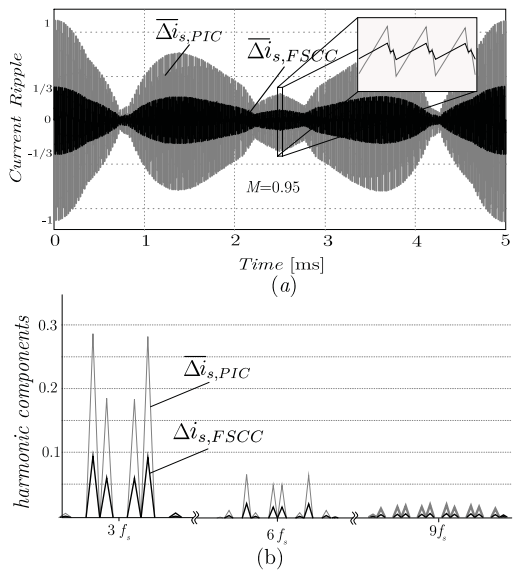

Fig. 8. (a) Normalized phase current ripple and (b) harmonic components for both Parallel Interleaved Converter and Four-State Commutation Cells Converter.

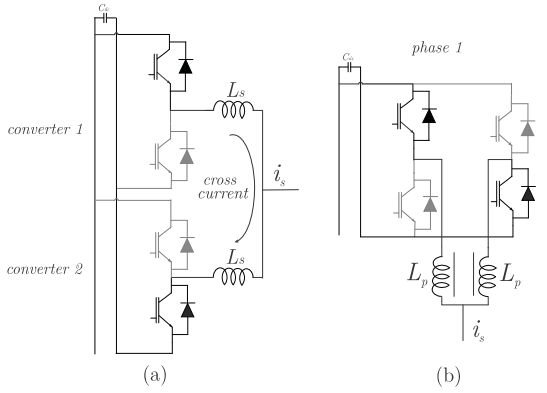

Fig. 9. Principle of cross current flow in both converters (a) PIC (b) Four States Commutation Cell (case of four switches per phase).

connected to the same DC link in this topology, so the total RMS current is the addition of each of the three inverters RMS dc-link currents. Complex analytical methods [22] or simulation might be adopted in order to reach this goal. In [25] a very straightforward procedure with purposes of estimating the capacitor useful life is described.

IV. CONTROL STRATEGY

Figure 10 shows the block diagram of the control strategy for both the voltage and current loops. As stated before, the current control is implemented based on grid-currents measurement, instead of the most popular filter-and-load currents measurement methods. This allows for a considerable reduction of computational efforts and cost. In [26] and [27] this strategy is implemented for a single-phase APF, in [28] and [29] is extended for a three-phase APF. One important characteristic of this method is the fact that even under unbalanced or distorted grid phase-voltage, the current withdrawn from the grid remains sinusoidal [28].

Nonetheless, in case of a short circuit on the load, the APF would tend to supply a very high current therefore this current should not be unattended. However, the required sensor for this protection will not be as expensive as the required one for control purposes.

This work presents an approach based on the currents transformation to dq0 magnitudes. As can be seen from Figure 10 the DC-link capacitor voltage is sensed and compared with the reference value. The error signal feeds the PI voltage controller and the output signal of the controller constitute the d-axis reference current. The q-axis current reference is kept to zero in order to guarantee high power factor current injection.

A. Current-loop Control

The inner control loop is in charge of the current control in both d and q axis. This implies that the sensed A, B and C current magnitudes must be transformed to these axis. The transformation matrix $\mathbf{T}$ and $\mathbf{T}^{-1}$correspond with (6) and (7) respectively:

$$\mathbf{T} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \\ -\sin(\omega t) & -\sin(\omega t - 2\pi/3) & -\sin(\omega t + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \quad (6)$$

$$\mathbf{T}^{-1} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) & 1/\sqrt{2} \\ \cos(\omega t - 2\pi/3) & -\sin(\omega t - 2\pi/3) & 1/\sqrt{2} \\ \cos(\omega t + 2\pi/3) & -\sin(\omega t + 2\pi/3) & 1/\sqrt{2} \end{bmatrix} \quad (7)$$

where $\mathbf{X}_{abc} = \mathbf{T}^{-1} \cdot \mathbf{X_{dq0}}, \mathbf{X}_{dq0} = \mathbf{T} \cdot \mathbf{X_{abc}}$,

with $\mathbf{X}_{abc} = \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix}, \mathbf{X}_{dq0} = \begin{bmatrix} X_d \\ X_q \\ X_0 \end{bmatrix}$.

After transformation and linearization of the model, the duty ratio to grid current transfer functions in dq0 coordinates are obtained as follows:

$$\begin{cases} G_{id}(s) = \dfrac{\hat{i}_d(s)}{\hat{d}_d(s)} = -\dfrac{V_{dc}}{sL_s} \\ \\ G_{iq}(s) = \dfrac{\hat{i}_q(s)}{\hat{d}_q(s)} = -\dfrac{V_{dc}}{sL_s} \end{cases} . \quad (8)$$

B. Voltage-loop Control

It is considered that the active power transferred through the APF inverter is the one supplied from the grid in order to compensate the power losses. If these losses are neglected the DC-link voltage model is given by:

$$G_{v,dq0}(s) = \frac{\hat{v}_{dc}(s)}{\hat{i}_d(s)} = \frac{\sqrt{\frac{3}{2}} V_{s,pk}}{sC_{dc}V_{dc}} \quad (9)$$

where $V_{s,pk}$ represents the peak value of the AC source phase voltage and C_{dc} represents the capacitance of the DC link.

C. Digital Implementation

The whole control algorithm was programmed on a DSP TMS320F28335 from Texas Instruments. Figure 11 shows the block diagram of both current and voltage control loops. Aspects related to the digital implementation like transport delay associated to sampling, ADC converters gain and anti-aliasing filters are included on the feedback transfer functions $H_i(s)$ and $H_v(s)$. The controllers for both loops were tuned on the continuous time domain and later on discretized by means of bi-linear transformation. The Phase Locked Loop (PLL) was also programmed on the DSP.

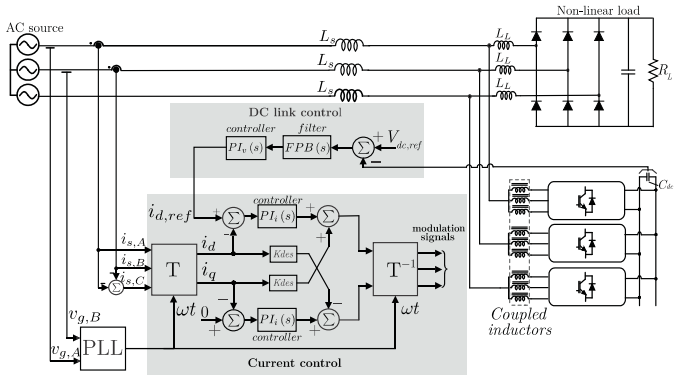

Fig. 10. Dq0 axis control strategy

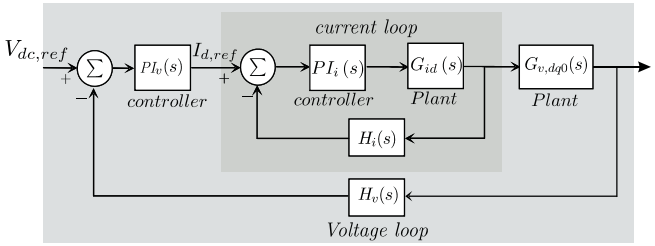

Fig. 11. Block diagram of the control loops containing the transfer functions involved in both control loops related to d-axis.

V. SIMULATIONS AND EXPERIMENTAL RESULTS

In order to test the control algorithm to be programmed on the DSP board, a simulation was carried out using the software PSIM with a C-block containing the control routine.

The parameters of the simulated and afterwards experimentally tested system are as follows:

Nonlinear Load Power P: 8 kVA

AC Source Line Voltage V_s: 380 V (the system was interfaced via an isolation transformer with a 1.22 turn-ratio)

DC Link Voltage V_{dc}: 600 V

Interface Filter Inductor L_s: 800 µH

Coupled Inductor Magnetizing Inductance L_m: 7 mH

Coupled Inductor Self Inductance: 4.7 mH

Coupled Inductor Mutual Inductance: 2.35 mH

DC Link Equivalent Capacitor: 4400 µF

Switching Frequency f_s: 15 kHz

Sampling Frequency f_a: 90 kHz

As a nonlinear load, a three-phase diode bridge rectifier with capacitive output filter was used. Figure 12 and 13 show the phase current and AC source voltage waveforms obtained from simulation and experiments. It can be noticed that the current being drained from the source, has a low harmonic distortion and it is practically in phase with the corresponding phase voltage. Figure 14 and 15 also show a comparison of simulation and experiments results. In this case the nonlinear load current and filter phase current are presented together with the filter phase voltage. The harmonic cancelation provided by the filter can be clearly appreciated from this figure. The fact of multiple voltage levels on the inverter phase voltage is also verified. Finally, Figure 16 and 17 show the currents through the three coupled inductors of one phase of the filter. It can be observed that these currents are balanced and in phase, if they are compared with the filter current from Figure 15 the amplitude reduction is verified, thus providing a lower current stress. It can be noticed on Figure 13 some remaining distortion on the grid current. A very important factor which influences this, besides the grid-voltage distortion and dead-time between gate signals of the same branch, is the leakage inductance of the coupled inductors. This leakage inductance is not modeled; therefore its effect will not be compensated properly.

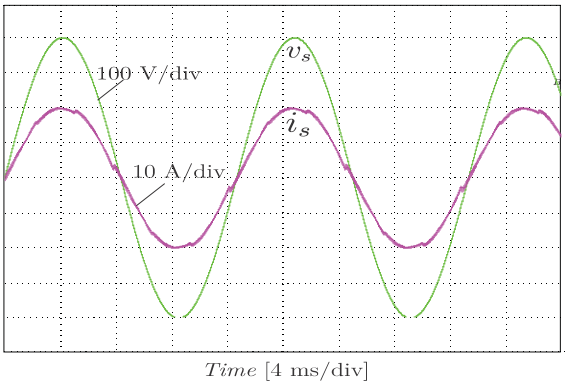

Fig. 12. Simulation results: AC source phase voltage (v_s) and current (i_s).

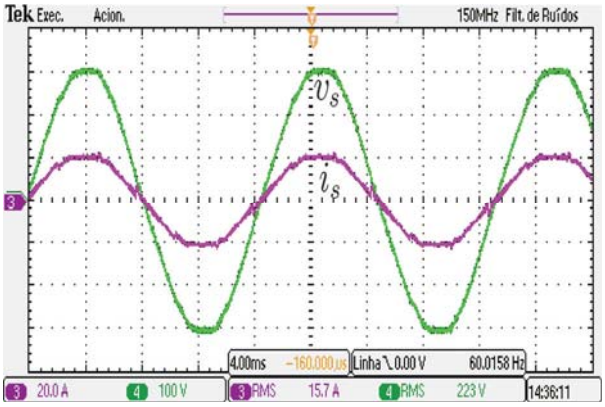

Fig. 13. Experimental results: AC source phase voltage (v_s) and current (i_s).

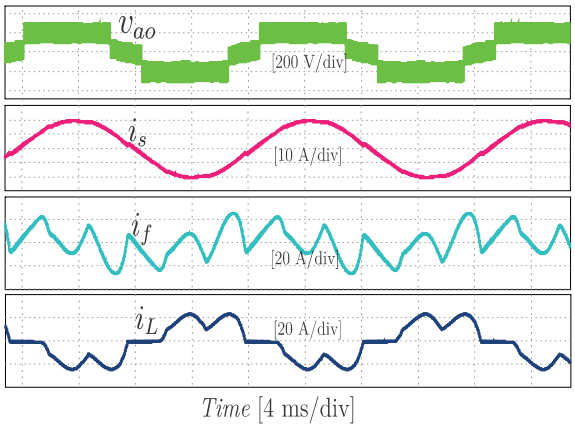

Fig. 14. Simulation results: Four states commutation cell converter phase voltage (v_{ao}), AC source phase current (i_s), filter current (i_f) and nonlinear load current.

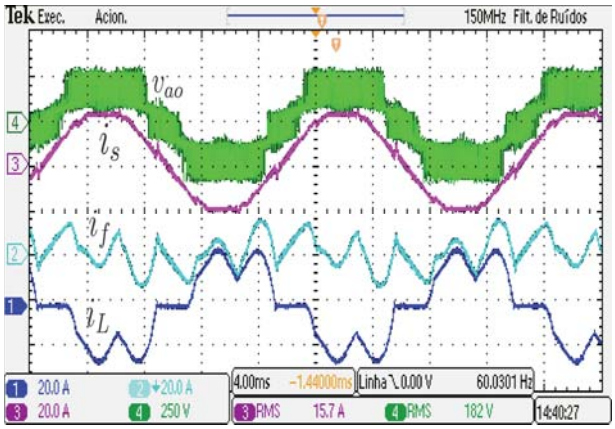

Fig. 15. Experimental results: Four states commutation cell converter phase voltage (v_{ao}), AC source phase current (i_s), filter current (i_f) and nonlinear load current.

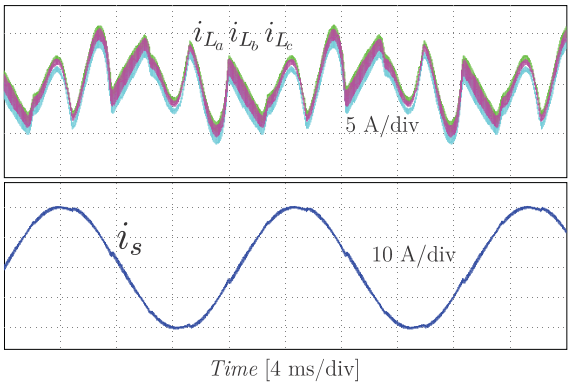

Fig. 16. Simulation results: AC source phase current (i_s), three-phase coupled inductors current (i_{L_a},i_{L_b} ,i_{L_c}).

VI.CONCLUSIONS

This work approaches the subject of Active Power Filtering, for the cases where the current stress of the semiconductor devices is a point of major concern. Instead of

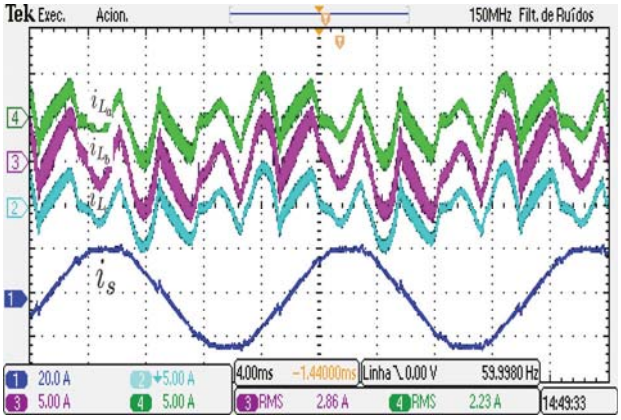

Fig. 17. Experimental results: AC source phase current (i_s), three-phase coupled inductors current (i_{L_a}, i_{L_b}, i_{L_c}).

the classic parallelism of inverters, a topology with coupled inductors is proposed to address this problem. In addition this topology provides advantages from the point of view of the output current ripple, providing more flexibility on the design of the filter inductors. A simpler and cost-effective control strategy based on the sensing of the AC source currents was implemented. The guidelines for the design of the key elements of the proposed APF system were presented. The control strategy in dq0 axes was described. Simulation and practical experiments were carried out in order to prove the correct behavior of the system. The results obtained showed the effective cancelation of harmonics by the APF being the current drained from the grid sinusoidal and practically in phase with the voltage.

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