STATE SPACE DECOUPLING CONTROL DESIGN METHODOLOGY FOR SWITCHING CONVERTERS

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***Abstract* – This paper derives an approach for analyzing dc-dc converters for feedback control design. The control-to-output voltage transfer function of the converters, usually predicted by averaging models, and the classical feedback control techniques is replaced by the state space average block diagram analysis. These state block diagrams are obtained from state space averaging matrixes of the converters combined with their continuous conduction mode differential equations. This decoupling technique yields first order control transfer functions allowing easier synthesis of controllers. The disturbance rejection properties of the controller are analyzed and improved by disturbance input decoupling. The technique is applied to the design of buck converters controllers, and the simulation and experimental results demonstrate good transient response when compared to classical voltage controllers. The structure is easy to implement with relevant applications in integrated circuit manufacturing and general industrial environments.**

***Keywords* - DC-DC Converter, State Space Control, Voltage Regulators, Disturbance Input Decoupling.**

I. INTRODUCTION

DC-DC converters with pulse width modulation are time varying, non-linear circuits that are usually modeled by small-signal averaging models. The state-space representation combined with the average technique results in the state-space averaging modeling [1]. The advantage of this approach is the inclusion of LC output filter in modeling process. The *PWM Switch* is a methodology similar to linear amplifier circuit that the basic idea is modeling only the switching elements of the power stage to obtain an equivalent circuit of these elements called the *PWM Switch Model* [2]. These models were developed for continuous and discontinuous conduction operation, and the continuous conduction mode (CCM) model is often used for control design.

After having formed the small signal representation of the power stage [3], the feedback controller that regulate the output voltage can be designed to attain the following objectives: zero steady state error, fast response to changes in the input voltage and the output load, low overshoot, and noise immunity.

Voltage mode control and current mode control are two traditional control techniques [4],[5]. The transient response of voltage mode control exhibits good noise immunity. However, its dynamic behavior is governed by complex poles. Current mode control improves the transient response characteristics by feeding back the inductor current. Two types of control have been established: 1) Peak current mode control that is popular and has been used for decades; 2) average current-mode control. The drawbacks of the former are its inherent instability when the duty ratio is greater than one half and the need for a stabilizing ramp to overcome the problem. The advantages of average current-mode control are the ability to control the average inductor current, the improvement of noise immunity, the lack of need for an additional stability ramp circuit [7]. Both peak current-mode control and average current-mode control structures are more difficult and expensive to implement compared to voltage mode control. In addition, the classical definition of bandwidth is not clear in the design of these controllers [7], [8].

The averaging models predict a control-to-output voltage transfer function with a complex pole pair (resonance) whose analysis for design of a suitable controller become a challenge based on a trial-and-error procedure. The k-factor is a simple and effective method for dealing with plants having complex dynamic behavior. It is a mathematical tool that eliminates the trial-and-error process to tune the controller as is normally done in classical controllers designed with the root locus method. To use this method, stability criteria must be reviewed since the concepts of phase boost and bandwidth are treated as fundamental variables to obtain stability [9].

Mixed voltage–current mode control has already been developed and it has given better control performance than the standard PI voltage control approaches. It was shown in [10],[11] that using a state block diagram to represent the dynamic behavior of a system, one can readily identify how the state variables are cross-coupled and how it is possible to decouple, i.e. cancel the effects of these variables on each other. Such state space decoupling controllers become easier to synthesize and they can be completely designed based on

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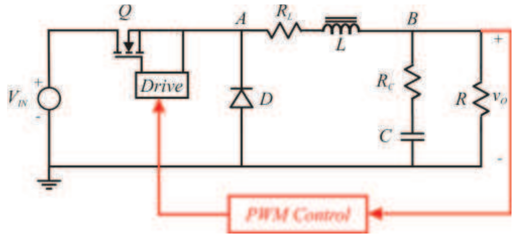
ɔntroller and digital adaptive control techniques [17],[18] 'ere proposed for reducing settling times and improving fast ep-load transient responses, however they are still limited y their complexity, by the A/D converters speeds and ɔnversions times. For these reasons they are beyond the :ope of this paper.

The subject of this paper is propose a systematic state ɔace decoupling control structure, with easy nplementation, moderate cost and satisfactory dynamic :sponses, based on bandwidth. The technique proposed ɛrein describes the behavior of the converter by its block iagram, presenting how the states are cross-coupled instead f the complexity of its transfer function. Based on this :presentation a state decoupling is arranged so that the /stems poles can assume positions where the controller /nthesis is not difficult to be realized. To design the ɔntrollers, a state block diagram of the converters was ɛrived. In [18], [19] the authors showed the basic principles f the proposed technique applied to buck converters, and a ɔmparison to the classical k-factor approach showed a faster ansient response with lower overshoot and no oscillation. In ıis paper the proposed technique is applied to the buck ɔnverter operating in continuous and discontinuous ɔnduction modes, and the disturbance rejection properties 'e analyzed. It is also shown how the disturbance rejection improved by using disturbance input decoupling.

The main contribution of this paper are: i) derive the block iagram of basic DC-DC converters, and understand how the ates are coupled; ii) use the block diagram to perform state ɔace decoupling; iii) design controllers based on simple ıalytic expressions for decoupled systems that behaves as rst order systems; iv) decoupled the output disturbance to ıve a system with better disturbance rejection properties.

II. SMALL SIGNAL ANALYSIS OF BASIC SECOND ORDER DC-DC CONVERTERS

The buck converter power stage with pulse width ıodulator is depicted in Figure 1. During normal operation, ıe switch Q is repeatedly switched on and off with the on ıd off times governed by the control circuit. This switch :tion causes a train of pulses at point A which is filtered by ıe LC output filter to produce a dc output voltage. R_C and $_L$ are parasitic elements representing the equivalent series :sistances (ESR) of the capacitor and inductor, respectively.



ːg. 1. Buck converter power stage schematic

The duration of the ON and OFF states in continuous ɔnduction mode (CCM) is given by (1) and (2), where D is ıe duty cycle set by the control circuit, and T_s is the time of ıe complete switch cycle.

$$T_{off} = (1 - D)T_s \quad (2$$

Applying the principles of steady-state converter analysi [4] and assuming that switch, diode and inductor resistanc voltage drops are small enough to be ignored, the voltag conversion relationship for output voltage V_O can b determined by (3), where V_{IN} is the input voltage of the buc converter.

$$V_O = DV_{IN} \quad (3)$$

The steps to do small signal analysis of the system fo small changes around the dc steady state operating point t obtain the buck converter transfer function using state-spac averaging approach are detailed in [3]. These steps ar summarized as:

(a) State-variable description for each circuit state;
(b) Averaging the state-variable description using th duty ratio;
(c) Introducing small ac perturbations and separatio into ac and dc components;
(d) Determination of the operating point and transfe function.

Utilizing the four steps above, the control-to-outpu voltage transfer function of the buck converter can b obtained and expressed by (4).

$$G_{PS}(s) = \frac{\tilde{v}_o}{\tilde{d}} = V_{IN} \cdot \frac{R}{R + R_L} \cdot \frac{1 + sR_C C}{\alpha s^2 + \beta s + 1} \quad (4$$

where:

$$\alpha = LC\frac{R + R_c}{R + R_L} \; and \; \beta = C\left(R_c + \frac{RR_L}{R + R_L}\right) + \frac{L}{R + R_L}$$

Repeating the previous steps for boost and buck-boos converters, one obtains the control-to-output voltage transfe functions presented in Table I.

TABLE I
Control-to-output voltage transfer functions of (a) boost and (b) buck-boost Converters.

$G_{PS}(s) = \frac{V_{IN}}{(1-D)^2} \frac{\left(1 - \frac{L_e}{R}s\right)(1 + R_C Cs)}{L_e C\left[s^2 + \left(\frac{R_C}{L_e(1-D)} + \frac{1}{RC}\right)s + \frac{1}{L_e C}\right]}$	(A)
$G_{PS}(s) = \frac{V_{IN}}{(1-D)^2} \frac{\left(1 - \frac{DL_e}{R}s\right)(1 + R_C Cs)}{L_e C\left[s^2 + \left(\frac{R_C}{L_e(1-D)} + \frac{1}{RC}\right)s + \frac{1}{L_e C}\right]}$	(B)

where $L_e = \frac{L}{(1-D)^2}$.

The general approach to design a voltage regulator for dc dc converters is to define the compensator necessary t obtain the desired phase margin and crossover frequency fo the closed loop system. This design is based on the transfe functions of the converters, and, in general, results i compensators with second or third order transfer function: One of the classical tools used to design voltage regulator

III. STATE SPACE DESIGN USING DECOUPLING

Another way to design a regulator for a system is to analyze its state space block diagram instead of its transfer function. The state space block diagram shows explicitly how the state variables are cross-coupled, and this is important when designing a controller exploiting the physical features of the system.

A. State Block Diagrams of Basic 2nd Order Converters

To obtain the average model, state block diagram of a buck converter, one uses the state space average matrixes for each state (on and off) of the power switch in CCM [13]. The differential equations written from these matrixes, including small variations of the load, are given by (5), (6) and (7).

$$L\frac{d\tilde{\imath}_L}{dt} = -R_1\tilde{\imath}_L - G_1\tilde{v}_C + \tilde{d}V_{IN} - R_2\tilde{\imath}_o \tag{5}$$

$$C\frac{d\tilde{v}_C}{dt} = G_1\tilde{\imath}_L - \frac{1}{R_3}\tilde{v}_C + G_1\tilde{\imath}_o \tag{6}$$

$$\tilde{v}_o = R_2\tilde{\imath}_L + G_1\tilde{v}_C + R_2\tilde{\imath}_o \tag{7}$$

Where $\tilde{\imath}_L$, $\tilde{\imath}_o$ represent small variations around the operating point of the inductor current, and load/output current (disturbance), respectively; $\tilde{v}_C$, $\tilde{v}_o$ represent small variations around the operating point of the capacitor voltage, and output voltage, respectively. The parameters and gains are defined in Table II.

TABLE II
Parameters of the Buck Average Model, State Space Block diagram

$R_1 = \frac{RR_C + RR_L + R_CR_L}{R + R_C} \cong R_C + R_L$	$G_1 = \frac{R}{R + R_C} \cong 1$
$R_2 = \frac{RR_C}{R + R_C} \cong R_C$	$R_3 = R + R_C \cong R$

Using (5) – (7) the buck average state block diagram, including the load current disturbance represented by $\tilde{\imath}_o$, can be depicted as shown in Figure 2. It must be noted that $\tilde{\imath}_o$ is included to aid in the analysis of the disturbance rejection. For the design of the regulator, it is set to zero.

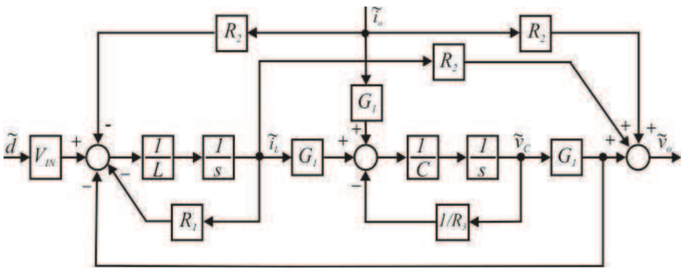


Fig. 2. Average model, state space block diagram of buck converter, including disturbance.

Using the same procedure, and defining the parameters and gains showed in Table III, the average model, state space block diagrams of boost and buck-boost converters can be a block with the duty cycle D must be placed before the inp showed in Figure 3.

The same procedure can be used to derive the state spac block diagram of any converter. For example, the state bloc diagram of the forward converter is similar to that depicted Figure 2, except that the turns ratio of the transformer mu be included.

TABLE III
Parameters of the Boost Average Model, State Space Block Diagrams

$G_2 = \frac{R[R(1-D)+R_C]}{RR_L + R_LR_C + RR_C(1-D) + R^2(1-D)^2}$	
$G_3 = \frac{R}{R + R_C}(1-D)$	$R_4 = R_L + \frac{RR_C}{R + R_C}(1-D)$
$R_5 = \frac{RR_C}{R + R_C}(1-D)$	$R_6 = R(1-D) + R_C$

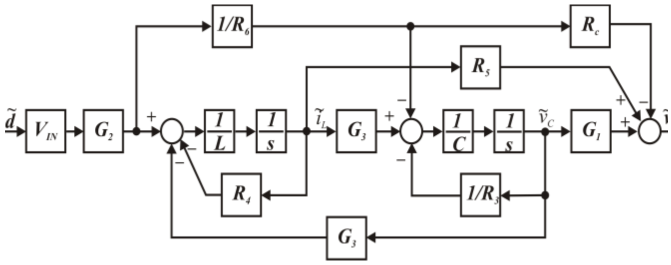


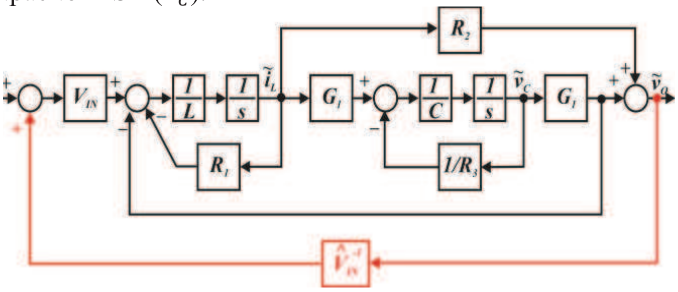
Fig. 3. Average model, state space block diagram of boo converter.

B. State Space Decoupling

State space decoupling is a technique that uses state spac feedback to decouple the cross-coupling among state resulting, in general, systems with better dynamic properti [9],[10],[13]. It will be used in this paper in the design controllers for dc-dc converters.

As an example, by analyzing the state block diagram the buck converter (see Figure 2) it is clear that the capacit voltage and inductor current states are cross-coupled. If it possible to measure the capacitor voltage, this cross-couplir could be eliminated. However, it is impossible to exact decouple it because the only variable that can be measured the output voltage, instead of the true capacitor voltag Applying a positive feedback as depicted in Figure 4, it still possible to decouple, i.e. cancel the cross-couplir between the voltage and current states. For the purpose controller design and cross-coupling decoupling the outp load variation $\tilde{\imath}_o$ is removed from the block diagram show in Figure 4. In this figure $\hat{V}_{IN}$ represents the estimated valu of the input voltage. For analog controller as the or presented in this paper this value will be the nominal value the input voltage, and it will never change even if th voltage changes. For discrete-time controllers this value ca be updated based on the measured value output voltage ar the duty cycle.

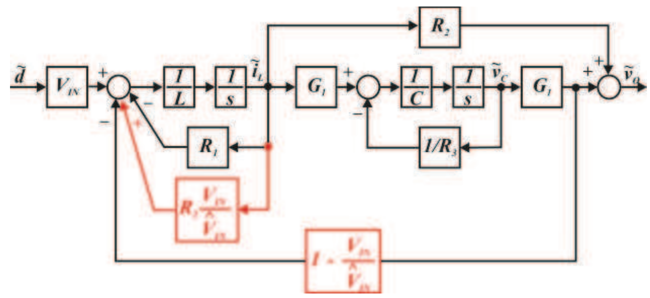
The block diagram of Figure 4 can be redrawn as show in Figure 5 to explicitly demonstrate the effect of non-ide cross-coupling decoupling. The inductor current sta feedback is a combination of two equivalent resistances, (8 ı this case there is a perfect decoupling. Furthermore, the ·oss-coupling decoupling is completely independent of the ıpacitor ESR (R_C).



ig. 4. Average state space block diagram of buck converter ıowing state space decoupling.

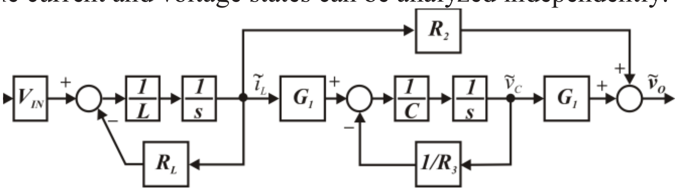
$$R_1 - R_2\frac{V_{IN}}{\hat{V}_{IN}} = \frac{RR_C + RR_L + R_CR_L}{R + R_C} - \frac{RR_C}{R + R_C}\frac{V_{IN}}{\hat{V}_{IN}} \cong R_L \qquad (8)$$

$$1 - \frac{V_{IN}}{\hat{V}_{IN}} \cong 0 \qquad (9)$$



ig. 5. Equivalent state space block diagram of buck converter after ate space decoupling.

After ideal decoupling the system state space block iagram can be depicted as shown in Figure 6. The system ɔles, initially complex, move to the real axis, located at ı $= -\frac{R_L}{L}$ and $p_2 = -\frac{1}{CR_3}$. In general, R_L (equivalent series ːsistance of the inductor) is a small value (parasitic ement), and the dominant pole (p_1), related to the inductor ırrent, moved to a position closer to the origin of the ɔmplex plane. This is because of the link between $\tilde{\imath}_L$ and $\tilde{v}_o$ ırough the resistor R_2. This is an interesting feature of doing ıe decoupling by using the output voltage, and emphasizes ıe potential use of a simple proportional controller for ırrent, especially for the cases where $R_L \cong 0$. Furthermore, ıe current and voltage states can be analyzed independently.



ig. 6. Average block diagram of the buck converter with exact ate space decoupling.

It is important to notice that even with the state space ecoupling of Figure 6, the use of just a PI regulator for the ɪtput voltage loop does not improve the performance of the osed loop system. In general, a PI regulator for the output ɔltage control results in complex closed loop poles. To whose bandwidth is much larger (at least one decade) tha the voltage one, the system bandwidth could be locate wherever desired by defining the voltage outer loc bandwidth since the current regulator block could ŀ considered approximately ideal.

C. State Space Controller Serial Tuning

Because it is possible to analyze each state independentl (after decoupling the cross-coupling), the block diagram use to tune the inner current controller loop is shown in Figure As noted earlier, a P regulator can be used for this state. I this case, $G_c(s) = K_{pc}$. By defining this controll bandwidth as B_{wc}(Hz), the gain K_{pc} can be calculated usin (10).

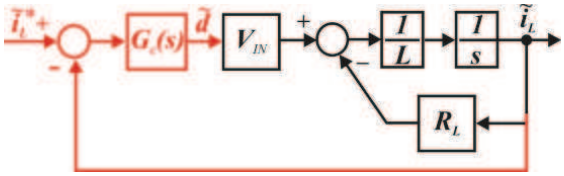


Fig. 7. Block diagram used to tune the current loop.

$$K_{pc} = \frac{2\pi B_{wc}\hat{L} - \hat{R}_L}{\hat{V}_{IN}} \qquad (1($$

The current loop transfer function is given by (11). Tl steady state error (e_{ss}) for dc values ($s = 0$) is shown in (12 For sufficient high bandwidth the effect of output voltag (2nd term of 11 and 12) in the current control is practicall negligible, even with non-ideal cross-coupling decouplin This emphasizes that is not necessary to exactly decouple tl states. For ideal cross-coupling decoupling the output voltag has no influence on the current loop.

$$\tilde{\imath}_L = \frac{K_{pc}V_{IN}}{Ls + (R_L + K_{pc}V_{IN})}\tilde{\imath}_L^* - \frac{G_1(1 - V_{IN}/\hat{V}_{IN})}{Ls + (R_L + K_{pc}V_{IN})}\tilde{v}_o \qquad (11$$

$$e_{ss} = \frac{R_L}{(R_L + K_{pc}V_{IN})}\tilde{\imath}_L^* + \frac{G_1(1 - V_{IN}/\hat{V}_{IN})}{(R_L + K_{pc}V_{IN})}\tilde{v}_o \qquad (12$$

When the current inner loop is tuned for much high bandwidth than the voltage outer loop, its dynamics aı nearly independent of the voltage loop, making it possible t tune the voltage loop using the simplified state bloc diagram shown in Figure 8. The current loop is approximate by a unity gain, and a PI voltage controller is used.

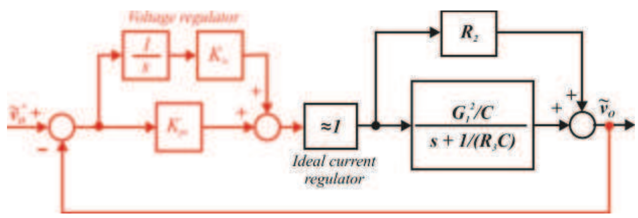


Fig. 8. Block diagram used for serial tuning of the voltage loop.

To design the voltage regulator, the PI controller zeı ($\boldsymbol{K_{iv}/K_{pv}}$) must be selected. One commonly used approac is to cancel the plant pole, in this case $\boldsymbol{p_2}$. Using this choic

$$K_{pv} = \frac{2\pi B_{wv}}{\widehat{G_1^2}/C - R_2 p_2 - 2\pi B_{wv} R_2} \quad (13)$$

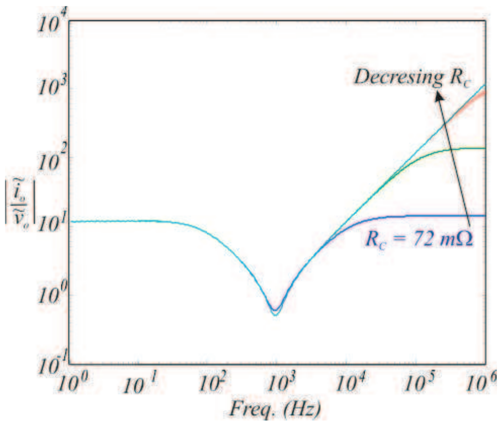
$$K_{iv} = -K_{pv} p_2 \quad (14)$$

IV. DISTURBANCE REJECTION PROPERTIES

One way to analyze the disturbance rejection properties of converter is to plot the magnitude of the output admittance equency response, $|\tilde{i}_o/\tilde{v}_o|$. This frequency response is ɔrmally called dynamic stiffness [11-16]. From Figure 2, e dynamic stiffness for the average operating point model the buck converter is described by (16). It is desired for a ystem to have infinite dynamic stiffness (DS), in other ords the system completely reject any load variation. In eneral this is true at high frequencies since most of the ıysical systems do not respond to fast disturbance ıriations. For the case of the buck converter the dynamic at gh frequencies is a combination of the load level epresented by the load resistor R) and the ESR of the ıpacitor (R_C). Specifically its value tends toward $(R + _C)/(RR_C) \cong 1/R_C$, and will be infinite only if $R_C = 0$. At w frequencies the DS tends toward $(R + R_L)/(RR_L) \cong /R_L$. For the converter parameters and operating point ıown in Table IV, the DS is plotted in Figure 10. In order to ject any low frequency disturbance, the regulator must be ɛsigned in order to improve the DS in the low frequency gion.

$$\frac{\tilde{i}_o}{\tilde{v}_o} = \frac{LC(R+R_C)s^2+[L+RC(R_C+R_L)+CR_CR_L]s+R+R_L}{LCRR_Cs^2+(LR+RCR_CR_L)s+RR_L} \quad (16)$$

In order to verify the effect of the regulators on the DS of e buck converter the regulators were design with the inner ırrent loop bandwidth set to *10 kHz*, and the outer voltage op bandwidth set to *1 kHz*. The result is plotted in Figure l along with other controllers for comparison. The ıprovement is the DS at low frequency is evident (curve ıck + regulators) and is infinite at zero frequency.



g. 9. Dynamic stiffness of buck converter showing the influence the ESR of the capacitor (R_C).

input decoupling (DID) [13-16]. Disturbance inpu decoupling simply uses the fact that if a disturbance inpu can be measured or estimated, then it is generally possible t decouple (null) that effective input before errors in th controlled states occur. This improves the dynamic stiffnes without any need to increase the state feedback gains. Th idea can be better understood by looking at the generic bloc diagram of Figure 11. This figure illustrates a generic plan with a disturbance, and a controller. If the disturbance can b measured, it can be decoupled as illustrated in the sam figure (blue lines and blocks). The block that represents th disturbance decoupling is $G_{DID}(s)$. And for this generic plan with a controller $G_c(s)$, the transfer function that performs th exact decoupling is given by (15).

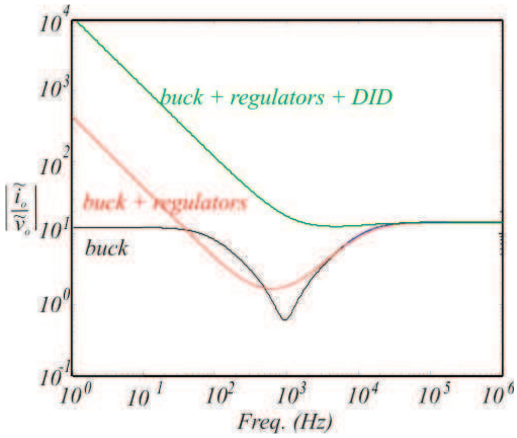


Fig. 10. Dynamic stiffness of buck converter with controllers.

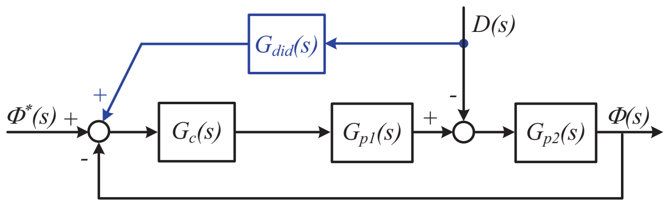
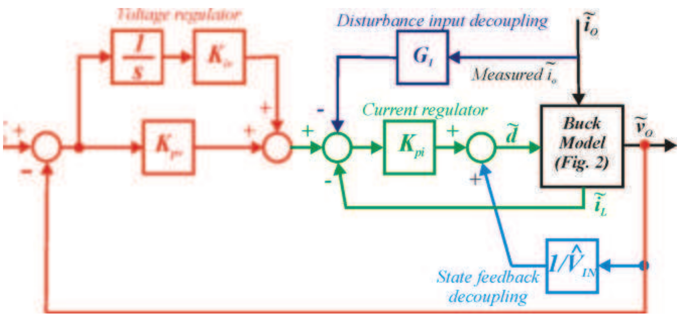


Fig. 11. Generic plant with DID implemented.

$$G_{DID}(s) = G_c(s)^{-1} G_{p1}(s)^{-1} \quad (1\!5$$

For the case of the buck converter, if it is economicall feasible to measure the load current then with a hig bandwidth current loop, its variation (disturbance input) ca readily be decoupled, i.e. achieving DID. In general, the loa current is measured in converters in order to protect again short circuit. Figure 12 shows one form to implement loa current disturbance decoupling. In this case, it is necessary t measure the load current variation around the operatin point. The DID is implemented using the load curre variation as an additional input to the current regulato Because the current regulator bandwidth is very fast, in th case its dynamic was ignored in the DID implementation. A a result the transfer function that represents the DID is ju the gain G_I. So the system will be able to reject loa disturbances up to the current regulator bandwidth. The D of the converter with the regulators and DID is also presente equency range up to the current regulator bandwidth.



ig. 12. Block diagram of buck converter with state space ecoupling, current and voltage regulators and DID.

V. SIMULATION RESULTS

In order to evaluate the performance of the state space ontroller proposed in this paper, a set of simulation xperiments were carried out using the buck converter with ıe parameters and specifications showed in Table IV. The ross-coupling decoupling shown in Figure 4 was done using ıe rated input voltage of 12 V. Several situations were mulated: 1) influence of non-ideal decoupling; 2) input oltage variation; 3) load current variation.

TABLE IV
Parameters of the Buck Converter Used in The Simulation

Output voltage (v_o):	*5 V*
Ripple in $v_o(\Delta v_o)$:	*50 mV (1 %)*
Input voltage (V_{IN}):	$9\ V \le V_{IN} \le 15\ V$
Ripple in $i_L(\Delta i_L)$:	*20 %*
Rated output current (i_o):	*2 A*
Switching frequency (f_s):	*50 kHz*
Output Capacitor (C)	*188 µF*
Output Capacitor ESR (R_C):	*72 mΩ*
Inductor (L):	*150 µH*
Inductor ESR (R_L):	85 *mΩ*

It was shown in (11) that the cross-coupling decoupling is function of the estimated input voltage. Figure 13 shows ıe dominant closed loop eigenvalue migration as a function f $\hat{V}_{IN}$. As shown in (11) the fastest eigenvalue, related to the ırrent loop dynamic, is not a function of $\hat{V}_{IN}$, and it is not ıown in Figure 13. For this figure the variation range 'as $0.2V_{IN} \le \hat{V}_{IN} \le 1.4V_{IN}$. The arrows show the direction of ıigration as $\hat{V}_{IN}$ decreases. One can be observed that values f $\hat{V}_{IN}$ much smaller than the rated value (for this converter $_{IN} \le 0.3V_{IN}$), the system poles tend to be complex. For alues of $\hat{V}_{IN}$ higher than the rated value the system poles emain in the real axis but moves toward the origin ecreasing the system bandwidth with respect to the designed ne.

Another way to analyze the influence of non-ideal

as a function of V_{IN} using the same variation range as show in Figure 13. For values of $\hat{V}_{IN} < V_{IN}$ the system tends to b more under damped. Increasing the value of $\hat{V}_{IN}$ with respe to V_{IN}, this increase has the effect of adding active dampir to the system, and decreases the system bandwidth. As result the system disturbance rejection will be worse for hig values of $\hat{V}_{IN}$. Even though it is not shown, the effect of no ideal decoupling will be more significant than the resul presented in Figure 13 and Figure 14 for smaller current loc bandwidths.

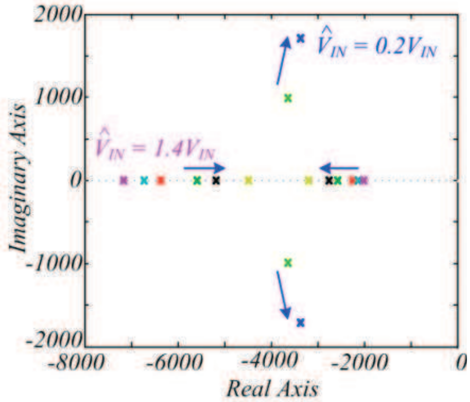


Fig. 13. Eigenvalue migration as a function of the estimated valı of input voltage.

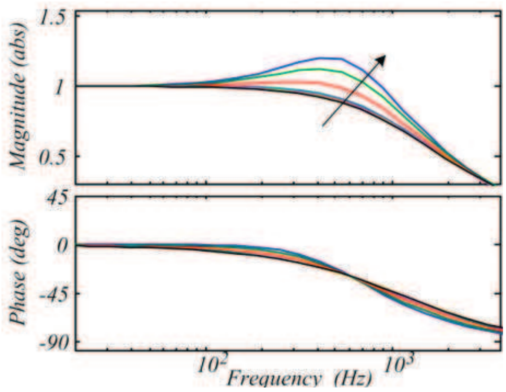


Fig. 14. Frequency response of the closed loop system as a functio of $\hat{V}_{IN}$.

Figure 15 shows the results for a step change in the inp voltage. The step amplitude variation was ΔV_{IN} = *- 25% (1 V → 9 V)* at *t = 8 ms*, ΔV_{IN} = *+ 25% (9 V → 12 V)* at *t 16ms*. The state space controller is practically insensitive input voltage variations, despite the fact that the cros coupling decoupling was done using the rated input voltag This voltage is not measured, and therefore it cannot b dynamically updated in the analog circuitry used for tl decoupling. The settling time t_s = *0* because the voltaş change was smaller than 2 % of the final value.

Figure 16 shows the results for a step change in the loa The step amplitude variation was Δi_o = *+50 % (1 A → 2* at *t = 2.5ms*. Actually, another resistor was switched on parallel to the load resistor R, and the equivalent outp resistor value was decreased to half of its original valu Because the load current is a function of the output voltag the load variation was not exactly a step variation. Instea the variation is similar to those observed in the outp voltage and current variations with (regulators + DID) and without DID. As expected the settling time t_s = *800 μs* when DID is not implemented. However, it is clear the improvement in the disturbance rejection when DID is implemented. The output voltage is almost insensitive to the load variation. The $t_s = 0$ because the voltage change was smaller than 2 % of the final value.

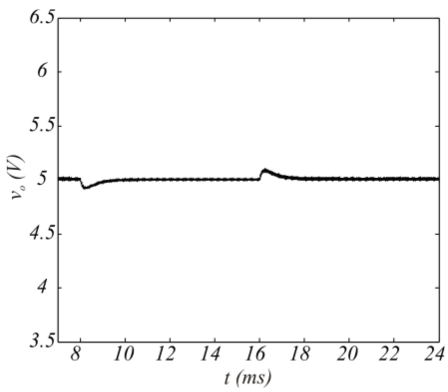


Fig. 15. Response to a step change in the input voltage (ΔV_{IN} = ±25%).

The simulation results showed that the proposed state space controller has the expected behavior. Because the current and voltage states were decoupled, it was possible to design the two loops to nearly independently control each state. A proportional controller was used for the inner current loop, and a PI controller for the voltage outer loop. The combination results in the system possessing dominant 1st order dynamics. Furthermore, the dynamic stiffness of the system is improved when DID is implemented.

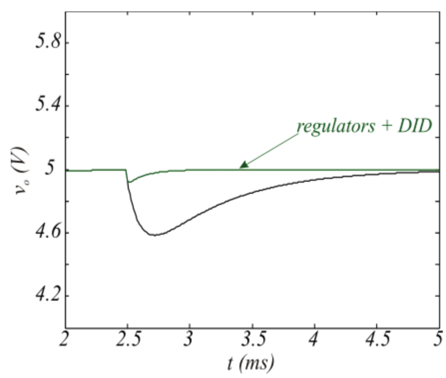


Fig. 16. Response to a step change in the load current(Δi_o = ±50%).

VI. EXPERIMENTAL RESULTS

The experimental results were carried out using a prototype with similar parameters to those used in the simulation. Except for the parasitic elements of the inductor, capacitor, MOSFET, and diode, the fundamental parameters were the same. However, the measured ESR of the inductor and capacitor, at *20 kHz*, were the same as those presented in Table IV ($R_L = 85\ m\Omega$ and $R_C = 72\ m\Omega$). The LCR meter used for the measurements operates at specific frequencies, and *20 kHz* was the closest to the switching frequency used in the circuit. Three tests were performed: 1) startup; 2) input voltage variation; 3) load variation with and without DID.

The state space controller for the buck converter was

current measurements are based on a Hall effect senso whose outputs are represented in Figure 17 by v_I for th inductor current, and v_{Io} for the output current variations. Th components used in the experimental setup are presented i Table V.

TABLE V
Parameters of the Experimental Setup

Operational amplifiers	*OPA2132*
Differential amplifiers	*INA128*
SCHOTTKY diode	*MBD360*
MOSFET	*IRF540*
Inductor	*Murata 1415440C*
Hall effect sensors	*LA100-P*

The measured voltage is represented by v_o and th reference voltage by v_o^*. The current loop bandwidth was se to *10 kHz*, and the voltage loop bandwidth was set to *1 kH* Using these bandwidths and the circuit componen presented in Table IV, the controller parameters wer calculated and are shown in Table VI. The resistors R_1, R $R_{11}$and R_{16} are selected to reduce the effects of input bia current of the op-amps.

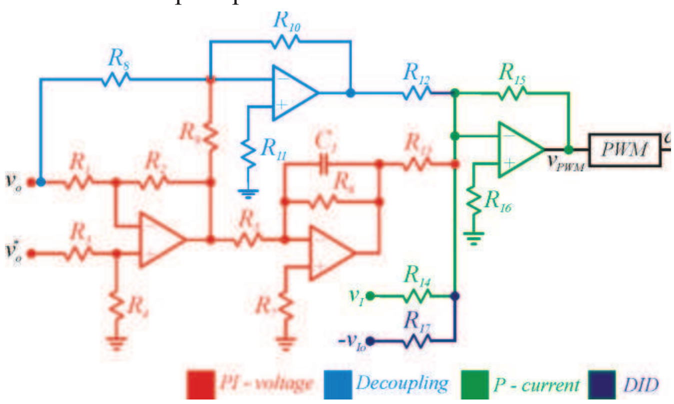


Fig. 17. State Space controller with cross-coupling decoupling.

Figure 18 shows the experimental results during startup c the buck converter. The figure shows the reference voltag (CH4) and the output voltage (CH1). The first conclusion : that the behavior is similar to the simulation results, and th settling time was $t_s \cong 320\ \mu s$.

TABLE VI
Parameters of the State Space Controller

$R_1 = R_2 = R_3 = R_4 = 40.2\ k\Omega$	$R_5 = R_7 = 27\ k\Omega$
$R_6 = 680\ k\Omega$; $R8 = 604\ k\Omega$	$R_9 = R_{13} = 41.2\ k\Omega$
$R_{10} = R_{12} = R_{15} = 100\ k\Omega$	$R_{11} = R_{16} = 9.3\ k\Omega$
R_{14} = 68,1 $k\Omega$	$C_1 = 20nF$

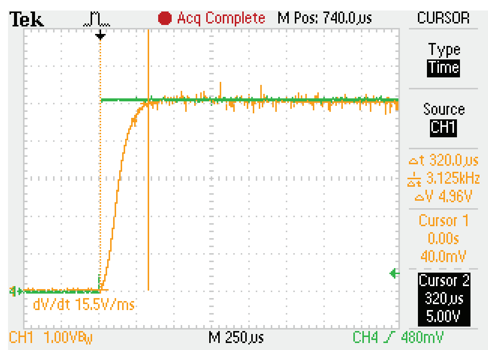
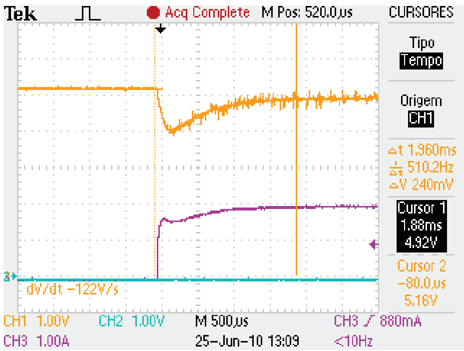
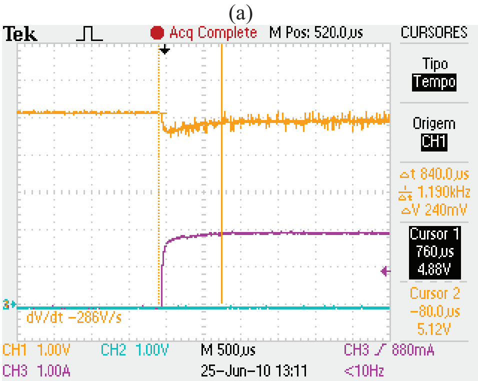


Figure 19 shows the experimental results for a 100% step change in the load current. The load variation was implemented by switching another resistor in parallel with the load. Both figures present the output voltage (CH1) and output current variation around the operating point (CH3).

Figure 19a shows the behavior of the state space controller without DID, and Figure 19b shows the results with DID implemented. The behavior of both cases is similar to that of the simulation results, the state space controller with DID having significantly better disturbance rejection properties. The output voltage variation was approximately -20% with a settling time of $t_s \cong 900\ \mu s$ for the state space controller without DID (Figure 19a), and approximately -8% with a settling time of $t_s \cong 500\ \mu s$ when DID was implemented (Figure 19b). As predicted in the simulation results, the load current variation is not exactly a step change because it is a function of the output voltage. Since the output voltage variation is more significant when DID is not implemented, the load variation in this case (Figure 19a) is initially smaller than the case where DID was implemented. However, even with an initially bigger load variation the controller response with DID presents better disturbance rejection properties.



(a)



(b)

Fig. 19. Response to a step change in the load current(Δi_o = $+100\%$): (a) controller without DID; (b) controller with DID. CH1 – output voltage; CH3 – output current variation.

The third test was a step change in the input voltage. Figure 20 shows experimental results for this case. The figure presents the output voltage (CH1) and input voltage (CH2). The noise shown in the input voltage is due to removal of the input filter of the converter. This was necessary to experimentally implement the step change in the input voltage. Otherwise this type of variation would not be possible. The step amplitude variation was ΔV_{IN} = $+\ 25\%$ $(12\ V \rightarrow 15\ V)$. Similar to the simulation results, the state space controller is almost insensitive to input voltag variations.

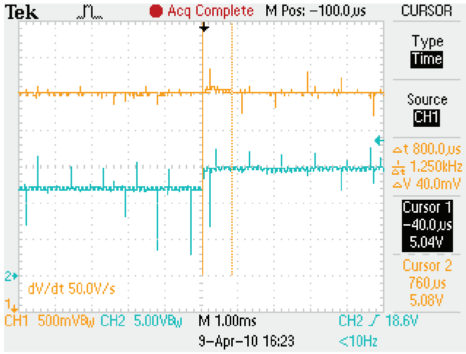


Fig. 20. Response to a step change in the input voltage (ΔV_{IN} = $+\ 25\%$ CH1 – output voltage; CH2 – input voltage.

VII. CONCLUSION

In this paper, a state space decoupling control techniqu for dc-dc converters was presented. Using small sign analysis, the equations of the converters were obtained. Wit the state space average differential equations of th converter, the average model, state space block diagram were developed. These block diagrams show, in a globa manner, how the state variables (capacitor voltage an inductor current) are cross-coupled and how it is possible t decouple the interaction between states and thus simplif design of robust converter controllers.

State space decoupling was applied to a buck converte resulting in a system with real poles. With these pol locations and the decoupled cross-coupling, the controlle design for the voltage and current loops were shown to b nearly independent.

The dynamic stiffness of the converter was presented an DID was shown to be a systematic approach to improve it.

Simulation and experimental results showed that the stat space controller response possessed good immunity to inpu voltage variation, a transient response with low overshoo and no oscillation during load variations.

The results suggest that the state space controller wit cross-coupling decoupling, and DID can be applied to othe converters as well.

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Dr. Lorenz is a Registered Professional Engineer in the States of New York and Wisconsin. He is also a member of the American Society of Mechanical Engineers, Instrument Society of America, and The International Society for Optical Engineers. He was IEEE Division II Director for 2005/2006, was the IEEE Industry Applications Society (IAS) President for 2001, a Distinguished Lecturer of the IEEE IAS for 2000/2001, past Chair of the IAS Awards Department, past Chairman of the IAS Industrial Drives Committee, and is a member of the IAS Industrial Drives, Electric Machines, Industrial Power Converter, and Industrial Automation and Control Committees. He is immediate past Chair of the Periodicals Committee and current Chair of the Periodicals Review Committee for the IEEE Technical Activities Board. He is a member of the IEEE Sensors Council AdCom. He is a long-time member of the EPE International Steering Committee and, in 2006, he received the EPE PEMC Outstanding Achievement Award. He has won 22 prize paper awards. He was awarded the 2003 IEEE IAS Outstanding Achievement Award, which honors his