AN FPGA-BASED SINGLE-PHASE INTERLEAVED BOOST-TYPE PFC RECTIFIER EMPLOYING GAN HEMT DEVICES

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***Abstract* - The recent development of higher blocking voltage gallium nitride (GaN) power FETs has the potential to enhance the power density of future power electronic converters. However, the new generation power semiconductors create new challenges to Power Electronics design that include: circuit layout to reduce parasitics, very high frequency digital control implementation, electromagnetic compatibility, passive components design, among others. In this work, GaN devices are used to assemble a 100 W single-phase two-channel interleaved boost-type power factor correction converter in order to evaluate some of the GaN devices challenges. The constructed hardware is able to operate with a switching frequency up to 1 MHz per channel, and hence a 2 MHz effective ripple frequency at the input and output terminals of the interleaved system. Furthermore, in order to cope with the high frequency requirements an average current mode control strategy is implemented in an FPGA device. Finally, experimental results verify the feasibility of the developed digital feedback control scheme and laboratory prototype.**

***Keywords* – Digital control implementation, Gallium Nitride semiconductors, Power factor correction, Very high switching frequency.**

I. INTRODUCTION

The progress of Power Electronics technology and the prospect of realizing very compact power converters lead to the use of new materials into power switching devices [1]. In this context, gallium nitride (GaN) power FETs can provide significant power density benefits over their silicon counterparts. GaN based converters with efficiency over 99% have been reported [2] and comparison of devices have demonstrated that first generation GaN devices are better than the silicon (Si) state-of-the-art devices [3]. Furthermore, GaN power devices present the potential to be less costly than silicon carbide (SiC) ones [4], [5] in low voltage applications.

The use in Power Electronics of wide bandgap materials impacts not only the electrical performance of power converters but also changes the way converters are designed. This is clear from the switched currents and voltages slopes, which increase and allow for higher switching frequencies to be used. In short, the switching losses are dramatically reduced and the switching frequency can be higher than what is typical today. Increasing the switching frequency leads to important challenges in fields such as circuit layout, magnetic components design, electromagnetic compatibility (EMC), gate drivers and, very important, the control and modulation devices.

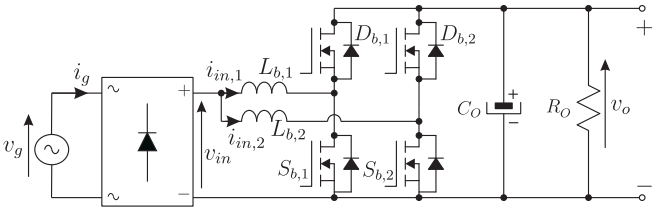

Fig. 1. Single-phase two-channel interleaved PFC boost-type rectifier employing GaN HEMT devices.

Today there is a wide field of applications that profit from digital processing devices to implement the supervision, control, protection, communication and pulse width modulation (PWM). Some of the most used devices being the digital signal processors (DSP) and controllers (DSC). However, such devices are dimensioned to typical power converter switching frequencies, which today range from 1 kHz up to 150 kHz. The most used DSPs and DSCs for Power Electronics would have a very difficult time when employed in very high switching frequency ($f_s \geq 200$ kHz) applications. Therefore, DSP based solutions will probably evolve to cope with higher switching frequency requirements. In the mean time programmable logic devices (CPLDs – Complex Programmable Logic Device and FPGAs – (Field Programmable Gate Array) appear as an alternative to the digital control of very high frequency PWM converters. Unfortunately, these typically present higher cost than DSPs/DSCs. Nevertheless, today these are perhaps the most fitted devices to implement all digital functions required by a power converter [6]. This work discusses the use of an

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FPGA to implement the control, protection and modulation tasks of a GaN based power factor correction (PFC) rectifier in addition to a vision of the status of GaN technology in PFC applications.

The first part of this work presents a panorama of GaN devices and reviews their capabilities and main characteristics. In addition, a comparison with state-of-the-art silicon and silicon carbide transistors is presented to show the potential of GaN devices regarding switching losses. A PFC rectifier topology featuring modular interleavead half-bridge converters (cf. Figure 1) is chosen and its design is discussed in Section III. The main challenges of implementing a current control strategy are discussed in Section IV along with the proposal for the implementation of an average current mode PFC control strategy for the chosen topology. Finally, experimental results illustrate the performance of the GaN based rectifier and conclusions are presented.

II. GALLIUM NITRIDE POWER FETS

Semiconductor devices based on silicon are quickly approaching their physical limitations. Wide bandgap semiconductor devices are being researched to allow further improvements in the field of Power Electronics with the new materials [4], [5].

Gallium nitride is a wide bandgap semiconductor of the III-V nitride group. Wide bandgap semiconductors, such as GaN and SiC, present many interesting properties that make them more attractive over the industry-established silicon. High breakdown voltages of 1.6 kV have been reported in AlGaN/GaN HEMT (High Electron Mobility Transistors) in 2006 [7]. Operating temperatures in excess of 300°C have been demonstrated since 1999 [8]. Very high switching frequencies and low on-state resistance can be obtained in GaN devices due to its high electron mobility.

The HEMT have been constructed with GaN as an interesting alternative to more conventional devices design. This structure is used today by different GaN devices manufacturers as the basis for their high performance power transistors design. GaN HEMTs work by forming a two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction interface, which leads to very high conductivity between source and drain. The operation of GaN HEMTs is somewhat similar to MOSFETs, in that the conductivity is controllable by the gate-source voltage. AlGaN/GaN HEMTs on silicon substrates also incorporate an intrinsic internal body diode that presents no reverse recovery. On the other hand, it has a much higher forward conduction voltage drop compared to normal silicon FETs.

Initially, the research on GaN devices focused on depletion mode HEMTs. Enhanced mode devices were later developed due to the need for safer switches.

In fact, GaN devices are still in an early stage of large-scale production. Companies currently offering commercial GaN solutions include Efficient Power Conversion (EPC), Transphorm, HRL Laboratories, International Rectifier, and GaN Systems, among others. The commercially available devices are today limited to blocking voltages up to 200 V. Another challenge to the successful production of GaN FETs is that these devices are more sensitive to gate ruptures than Si FETs [9].

TABLE I
Recent Results Based on GaN Devices in PFC Rectifiers

Research Group	η	P_o	f_s	V_o	Mode	Year
Semicond. Co. [10]	94.2%	122 W	1 MHz	350 V	Depl.	2008
Transphorm Inc. [11]	97.8%	300 W	1 MHz	350 V	Depl.	2008
K.U. Leuven [12]	96.0%	106 W	512 kHz	142 V	Enhan.	2010
HRL Laboratories [13]	95.0%	425 W	1 MHz	351 V	Enhan.	2011
HRL Laboratories [14]	94.0%	1.2 kW	1 MHz	300 V	Enhan.	2012
Fujitsu Laboratories [15]	94.3%	2.5 kW	70 kHz	380 V	Enhan.	2013

In the construction of static power switches, the widespread use of GaN substrates have been prohibitively high-priced. However, epitaxial process allows for volume deposition of GaN based material on low cost silicon wafers, costing about 100 times less than SiC. This makes GaN power devices a very attractive solution for the future of Power Electronics.

A. Research Results

Table I shows the results of some recent researches focused on PFC assembled with GaN devices. These reports have used research stage GaN devices of up to 600 V. It is clear that the listed converter systems present higher than usual Si-based converters efficiency given the respective switching frequencies. Another trend is to the latter use of enhancement mode GaN devices and the increased power ratings.

B. State-of-the-art Power Switches Comparison

Single-phase PFC applications typically employ 600-V switches whenever a power supply is rated close to 220 V. In this context, the performance of different types of state-of-the-art semiconductor switches are compared in the following.

The considered devices are: Transphorm GaN switch TPH3006PS [16], GeneSiC SiC switch 2N7639-GA [17], Infineon Si MOSFET IPP60R190P6 [18], and ST Si MOSFET STP20NM60 [19]. Datasheet parameters for the considered devices are listed in Table II. It is clear that the switching times associated to the GaN device are shorter than the other devices. The turn-on resistance is lower for the SiC device that, in addition, presents the capability to operate with higher junction temperature.

The focus of the comparison in on high switching frequency applications. Thus, the switching losses are chosen as the figure of merit for the proposed comparison. Fixed switching

TABLE II
Properties of Different Type of Power Switches

Property	Transphorm TPH3006PS	GeneSiC 2N7639-GA	ST STP20NM60	INFINEON IPP60R190P6
Technology	GaN Power	SiC	Si @ MDmesh	Si @ CoolMOS
continuous I_D @ 25°C	17A	-	20A	20.2A
continuous I_D @ 100°C	12A	15A @150°C	12.6A	12.7A
drain source voltage	600V	650V	600V	600V
resistance $R_{ds,on}$ $[m\Omega]$	150@25°C 330@175°C -	105@25°C 180@175°C 290@250°C	250@25°C - -	171@25°C 445@175°C -
Capacitance C_{iss}	740pF	1534pF	1500pF	1750pF
Capacitance C_{oss}	133pF	157pF	350pF	76pF
Capacitance C_{rss}	3.6pF	157pF	35pF	-
t_{rise}	3.1ns	37ns	20ns	8ns
t_{fall}	5.2ns	78ns	11ns	7ns

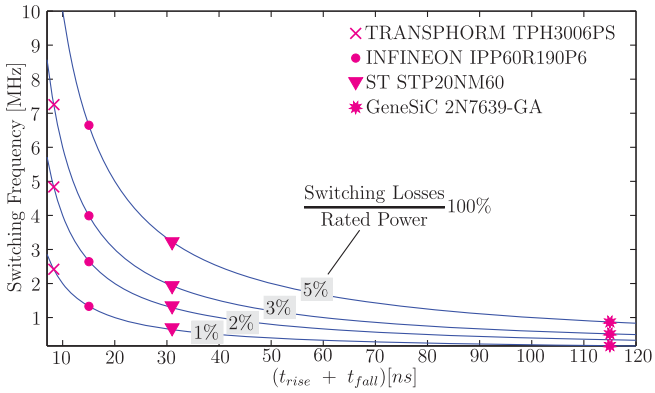

Fig. 2. Relationships between the switching frequency and the total switching time interval $(t_{rise}+t_{fall})$ for given switching losses percentile of the rated power.

losses levels define curves that relate to the datasheet rise (t_{rise}) and fall (t_{fall}) times and the switching frequency with which the device achieves the given switching loss level. Switching losses for a given device are computed with

$$P_{sw} = \frac{1}{2} I_D V_{DS} \left(t_{rise} + t_{fall}\right) f_{sw} + \frac{1}{2} C_{oss} V_{DS}^2 f_{sw} \quad (1)$$

where: C_{oss} [F] is the transistor output capacitance, P_{sw} [W] are the switching power losses, I_D [A] is the considered drain switched current, V_{DS} [V] is the switched drain to source voltage, and f_{sw} [Hz] is the switching frequency. Equation (1) is a simplified expression since the actual switching losses would depend on extraneous parameters such as layout parasitic inductances, gate driver circuits and diode characteristics. The assumed switched voltage is $V_{DS} = 400$ V, while the switched current is $I_D = 0.5$ A. The assumed rated power is $P_{\text{rated}} = 200$ W. The curves shown in Figure 2 are plotted assuming the according permissible switching power loss levels calculated with (1). The SiC transistor is not optimized for fast switching times. This limits the switching frequency to less than 1 MHz even if the switching losses are permitted to achieve 5% of the rated losses. Therefore, a maximum 5% switching losses level is chosen as the maximum acceptable level. With this, the Si devices enable switching frequencies up to approximately 7 MHz with 5% switching losses. Finally, the GaN device is able to achieve less than 3% loss at the same switching frequency. Thus, this first generation GaN device presents the potential to drastically reduce switching losses. Furthermore, the on-state resistance is also reduced when compared to the Si MOSFETs.

III. POWER CONVERTER DESIGN

A PFC rectifier prototype was designed and built in order to evaluate the performance of commercially available GaN devices. The chosen topology is a single-phase two-channel ($N=2$) interleaved boost converter [20]-[25]. As known from literature [20], the converter channels should be preferably operated with a phase-shift $\Delta\varphi = 180^{\text{o}}$ (in general $\Delta\varphi = 360^{\text{o}}/N$) phase shift. The main power circuit is seen in Figure 1, in which $S_{b,1-2}$ and $D_{b,1-2}$ are implemented through HEMT GaN power FETs. The chosen topology allows one to investigate the synchronous rectification [26] features of the GaN devices. This is very important to reduce losses as the forward conduction voltage drop of the body diode in these devices is high. Therefore, a power converter can profit from the nonexistent reverse recovery of the body diode and still have low conduction losses by activating the device channel whenever the body diode should be conducting.

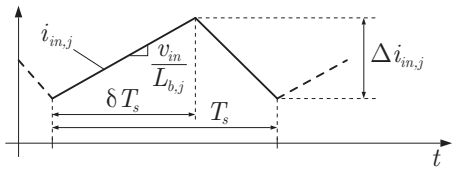

Fig. 3. Detail of the instantaneous current in one of the boost inductors.

Another reason to choose this topology to evaluate the GaN devices is that the losses can be distributed through four devices instead of two in a single channel topology. According to losses and thermal computation based on the loss data presented in [27], this structure is able to deliver an output power of $P_o \approx 100$ W with a fully surface mount devices (SMD)-based assembly. This is very important since GaN FETs are very sensitive to layout [9].

The losses are computed considering the inductors high frequency ripple (cf. Figure 3) and assuming that it is piecewise linear, i.e., assuming that the switching frequency f_{sw} is much larger than the mains frequency ($2\pi f_{sw} >> \omega$). Thus, the per period averaged rms value of the currents in the main converter components are given by

$$\langle i_{in,j}^{\text{rms}} \rangle^2 = \langle i_{in,j} \rangle^2 + \frac{\Delta i_{in,j}^2}{12} \quad (2)$$

$$\langle i_{Sb,j}^{\text{rms}} \rangle^2 = \delta \frac{12 i_{in,j}^2 + \Delta i_{in,j}^2}{12} \quad (3)$$

$$\langle i_{Db,j}^{\text{rms}} \rangle^2 = (1-\delta) \frac{12 i_{in,j}^2 + \Delta i_{in,j}^2}{12} \quad (4)$$

where $\langle x^{\text{rms}} \rangle$ is the rms value of x within a switching period, j, with $j = 1..N$, is the index that specifies which semiconductor leg is being referred within the N interleaved legs, δ is the duty-cycle of the switches $S_{b,j}$ and, $\Delta i_{in,j}$ is the peak-to-peak value of the j^{th} boost inductor current within a switching period, which is found with

$$\Delta i_{in,j} = \frac{\delta v_{in}}{L_{b,j} f_s}. \quad (5)$$

Assuming that the input voltage and current are

$$v_{in} = \hat{V} \sin(\omega t) \quad (6)$$

$$\langle i_{in} \rangle = \hat{I} \sin(\omega t) \quad (7)$$

and that the rms value of the currents through a component X is found with,

$$I_X^{\text{rms}} = \frac{1}{T_s}\int_{t-T}^{T} \langle i_X^{\text{rms}} \rangle d\tau \tag{8}$$

the resulting converter current efforts are

$$I_{L_b,j}^{\text{rms}} = \sqrt{\frac{\hat{I}^2}{2N^2} + \frac{\hat{V}^2}{L_b^2 f_s^2 M}\left(\frac{M}{24} + \frac{1}{32M} - \frac{2}{9\pi}\right)} \tag{9}$$

$$I_{Sb,j}^{\text{rms}} = \sqrt{\lambda_1 + \lambda_2} \tag{10}$$

where,

$$\lambda_1 = \frac{\hat{I}^2}{N^2}\left(\frac{1}{2} - \frac{4}{3\pi M}\right) \tag{11}$$

$$\lambda_2 = \frac{\hat{V}^2}{L_b^2 f_s^2}\left(\frac{1}{24} - \frac{1}{3\pi M} + \frac{3}{32M^2} - \frac{4}{45\pi M^3}\right) \tag{12}$$

$$M = \frac{\hat{V}}{v_o} \tag{13}$$

and

$$I_{Db,j}^{\text{rms}} = \frac{\sqrt{5}}{60}\sqrt{\frac{960\hat{I}^2}{\pi M N^2} + \frac{(80M^2 - 45M\pi + 64)\hat{V}^2}{\pi M^3 N^2 L_b^2 {f_s}^2}}. \tag{14}$$

Employing the same procedure to find the boost diode average current value leads to

$$I_{Db,j}^{\text{avg}} = \frac{P_o}{V_o N}. \tag{15}$$

Thus, the computed current stress across the GaN devices are

$$I_{Sb,j}^{\text{rms}} \approx 0.763\,\text{A} \tag{16}$$

$$I_{Db,j}^{\text{rms}} \approx 0.492\,\text{A} \tag{17}$$

$$I_{Db,j}^{\text{avg}} \approx 0.625\,\text{A}. \tag{18}$$

The loss characteristics fitting parameters extracted from the device EPC2010 datasheet [28] are: GaN HEMT on-state resistance at 100ºC $r_{on} = 1.45 \cdot 25\ \text{m}\Omega \approx 36.25\ \text{m}\Omega$ and the forward voltage drop of the body diode $V_{TO} = 1.8$ V. Assuming that the conduction losses are given by

$$P_D = V_{TO} I_{Db,j}^{\text{avg}} \tag{19}$$

$$P_S = r_{on} {I_{Db,j}^{\text{rms}}}^2 \tag{20}$$

where P_D are the conduction losses of an intrinsic diode and P_S of a switch, leads to the following conduction losses

$$P_{cond,\text{diode}} \approx 4.542\,\text{W} \tag{21}$$

$$P_{cond,\text{sync-rect}} \approx 59.77\,\text{mW} \tag{22}$$

where $P_{cond,\text{diode}}$ is the total GaN devices conduction loss without synchronous rectification and $P_{cond,\text{sync-rect}}$ is the loss considering ideal synchronous rectification. From these results it becomes clear that the backward conduction in GaN HEMT devices is advantageous for a high efficiency design.

The switching losses P_{sw} are computed with the integration of a loss energy function w_{sw},

$$P_{sw} = \frac{f_s}{2\pi}\int_0^{2\pi} w_{sw}\, d\omega t \tag{23}$$

where

$$w_{sw} = K_0 + K_1\, i_{sw} + K_2\, i_{sw}^2 \tag{24}$$

and i_{sw} is the value of the switched current, i.e. the per switching period averaged mean value of the boost inductor current added to the high frequency ripple. The polynomial switching loss coefficients are taken from [27]: $K_0 = 1.8319\,\mu$J; $K_1 = 1.9227\,\mu$J/A; and, $K_2 = 24.5990$ nJ/A^2. The total switching losses P_{sw} for the GaN devices with the converter switching at $f_s = 250$ kHz are,

$$P_{sw} = N f_s\left(K_0 + \frac{2K_1\hat{I}}{\pi} + \frac{K_2\hat{I}^2}{2}\right) \approx 1.462\,\text{W} \tag{25}$$

where the switching losses are mainly due to the parallel capacitance of the devices, i.e., K_0 is dominant in (25).

Finally, the computed efficiency considering only the power semiconductors losses is

$$\eta_{GaN} = \frac{P_o}{P_o + P_{cond} + P_{sw}} \approx 98.1\% \text{ for } f_s = 250 \text{ kHz}. \tag{26}$$

This is reduced to $\eta_{GaN} \approx 96.7\%$ for $f_s = 500$ kHz and $\eta_{GaN} \approx 94.1\%$ for $f_s = 1$ MHz. In case a four-channel interleaved PFC were used the new converter efficiency would be $\eta_{GaN} \approx 99.5\%$ for $f_s = 250$ kHz, $\eta_{GaN} \approx 98.9\%$ for $f_s = 500$ kHz, and $\eta_{GaN} \approx 97.9\%$ for $f_s = 1$ MHz.

In order to make a brief comparison, state-of-the-art Si MOSFET model FDP18N20F that presents similar voltage and current ratings as the used GaN device would lead to a 5 to 10 times larger PCB area to provide the necessary cooling effect. The efficiency for a two-channel converter with Si MOSFETs technology is close to $\eta_{GaN} \approx 91.9\%$ with $f_s = 500$ kHz.

IV. CONTROL STRATEGY

As seen in Table I, the reported switching frequencies for research PFC rectifiers employing GaN devices are typically higher than $f_s \approx 500$ kHz. This illustrates the potential for such devices as it does show the need for high frequency control/modulation/protection auxiliary circuitry. The control circuits of choice today being analog integrated circuits (ICs) and DSPs, both of which do not have many options for switching frequencies above 500 kHz. Analog ICs are only recently being developed for use with GaN devices [29]. Typical DSPs used in Power Electronics are not designed to provide closed loop control and modulation functions at such high frequencies. Thus, this work employs an FPGA solution for the control and modulation functions of a GaN-based single-phase PFC rectifier.

The implemented control strategy is the average current mode control, largely employed in PFC converters operating in continuous conduction mode (CCM) [30]. It is implemented in an FPGA device through hardware description language

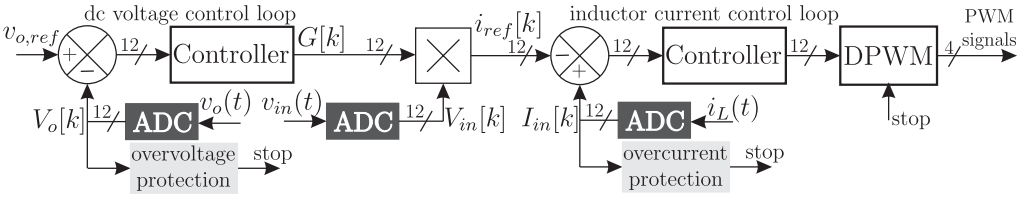

Fig. 4. : Block Diagram of feedback control strategy implemented in an FPGA. Three sensed variables are required by the control system: i_{in}, v_{in} and v_o. The analog-to-digital conversion of these measured variables is performed by three Analog-to-Digital Converter (ADC) devices, AD 7276, operating in parallel and independently.

(VHDL) within the development environment Quartus II Web Edition [31]. As shown in Figure 4, three sensed variables are required by the control system, namely: the inductor current i_{in}, the ac voltage v_{in} and the output dc voltage v_o. The analog-to-digital conversion of these measured variables is performed by three Analog-to-Digital Converter (ADC) devices, Analog Device AD 7276, operating in parallel and independently. The interface employed between each ADC and FPGA is based on an SPI – *Serial Peripheral Interface* protocol at a sampling frequency of 1 MHz and a 16 MHz clock signal.

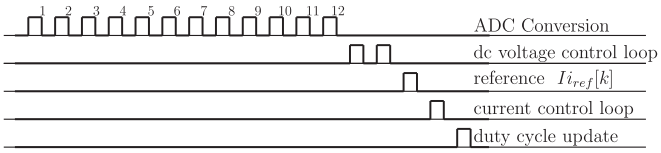

Fig. 5. Timeline of events in the control strategy implemented in an FPGA.

Figure 5 shows the time diagram with the main events within the proposed control strategy. The state machine starts a counter, which implements a sawtooth carrier for a digital pulse width modulator (DPWM). At the same instant, a signal initializes the analog to digital conversion at each ADC. After a clock cycle, the ADC processed data is sent to the FPGA. After 12 clock cycles the measured input voltage, inductor current and output dc voltage are available to the PFC control processing. These data are transferred through the SPI interface. A Proportional-Integral (PI) controller is employed in the output dc voltage control loop to guarantee good voltage regulation. On other hand, in the input current control loop a Proportional (P) controller is implemented. The duty-cycle is updated to the PWM modulator after all control laws are computed. As previously discussed, the input current i_{in} and the dc voltage v_o are sampled at every 1 μs. Therefore, a moving average filter with 16 samples of these variables is used in the protection tripping logic in order to avoid untimely activation of the software system protection.

V. EXPERIMENTAL RESULTS

In order to verify the feasibility of the proposed digital control strategy, which is well suited for high frequency Power Electronics converters, a laboratory prototype of the single-phase PFC system depicted in Figure 6 has been built. The hardware implementation is shown in Figure 7. The power stage of the prototype comprises an EMC input filter, a diode bridge, a two-channel interleaved GaN boost-type converter and a dc-link SMD capacitor bank. As commercial 600 V GaN turn-off devices are not readily available at the moment, the converter was assembled with reduced voltage specifications in order to be able to use the 200 V GaN devices from EPC.

TABLE III
Prototype Specifications

Specification	Symbol	Value
Input voltage RMS value	$V_{g,rms}$	40 V
Input voltage frequency	f_g	50 Hz
Output voltage dc value	v_O	80 V
Switching frequency range	f_s	250, 500 and 10^3 kHz
Gan devices	S_b, D_b	EPC2010
GaN devices gate drivers	–	LM5113
GaN devices gate resistance	R_g	0 Ω
Inductance value (dc and no current)	L_b	100 μH
Dc capacitance	C_O	1100 μF
Shunt Resistance	R_{sh}	0.1 Ω

The prototype specifications are listed in Table III. A relatively large output capacitance is used to limit the dc-link voltage ripple due to the double mains frquency oscillating power component typical for the single-phase PFC application. Even though, the ac voltage is reduced when compared to typical PFC applications, all control and supervision functionality of a PFC rectifier were implemented within an FPGA kit in a DE0-Nano Board [32]. This FPGA development platform includes: an Altera Cyclone IV EP4CE22F17C6N FPGA; 153 FPGA pins used as digital logical inputs/outputs; on-board USB-Blaster circuit for programming; a memory with 32 MB SDRAM; and an on-board 50 MHz clock oscillator.

The switching behavior of the GaN devices is shown in Figure 8 when these devices are switched at 1000 kHz. Switching transitions of approximately 80 V occur in less than 5 ns leading to a dv/dt of more than 18 kV/μs during the turn on or turn off processes. Such times make it clear that the devices can be operated at very high switching frequencies. The experimental results in Figure 8 were performed with the prototype operating as a dc-dc boost interleaved converter with an output dc voltage V_{dc}=80 V; dead-time t_d= 10 ns, switching frequency f_s= 1 MHz, and an output power of P_o= 50 W. The results in Figure 8 are acquired with a 1 GHz oscilloscope at a sampling rate of 2 GS/s, i.e., there is enough precision to

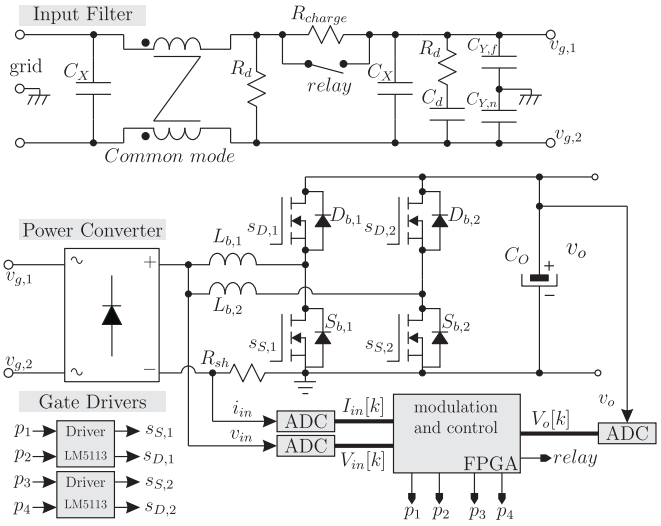

Fig. 6. Schematics and feedback control scheme of a single-phase two-channel interleaved boost-type PFC rectifier.

Fig. 7. Hardware implementation of fully digital high switching frequency single-phase interleaved boost-type PFC rectifier.

observe the rise and fall edges of the switched voltages. No relevant overvoltage is observed mainly due to the use of very small packages for, both, GaN HEMTs and their gate drivers, in addition to a extremely tight layout, where SMD decoupling capacitors were used. A total parasitic inductance lower than $L_\sigma \leq 0.7$ nH is estimated for the switched power loop and a similar quantity for the gate driver loop.

The thermal mesurements were performed with a FLIR A645 SC Infrared Camera with High-resolution 640 × 480, 17 micron pixel detector. This provides plenty of image detail and small hot spots can be accurately measured. The temperature range is 20°C up to +650°C.

The prototype was supplied from a programmable ac power supply made by Agilent Technologies model 6813B *AC Power*

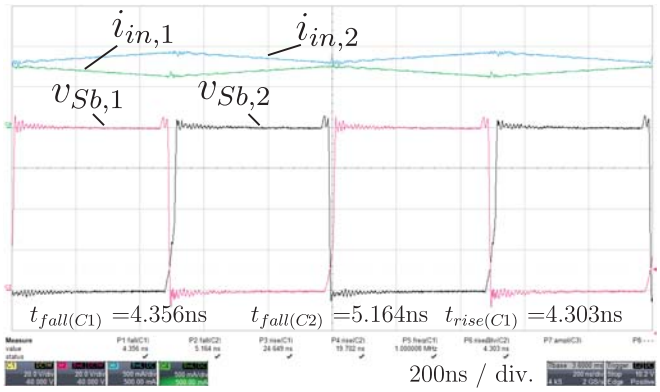

Fig. 8. Experimental results showing the switching transitions of the EPC2010 GaN HEMTs with a switching frequency per leg of f_s= 1000 kHz. Time scale [200 ns/div.], switch voltage [20 V/div.] and inductor current [500 mA/div.].

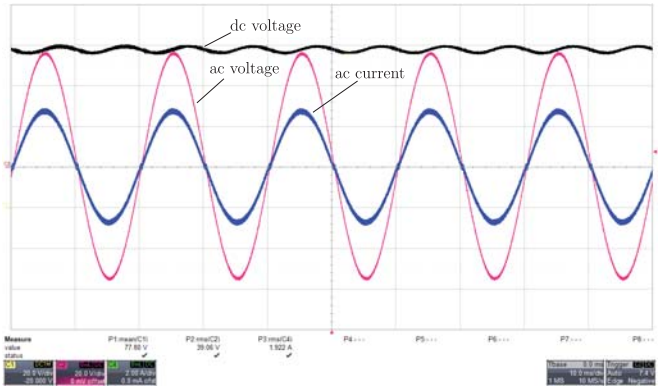

Fig. 9. Experimental results of the assembled PFC rectifier at P_o = 75 W. Ac voltage [20 V/div.], input current [2 A/div.], dc voltage [20 V/div.] and time scale [100 ms/div.].

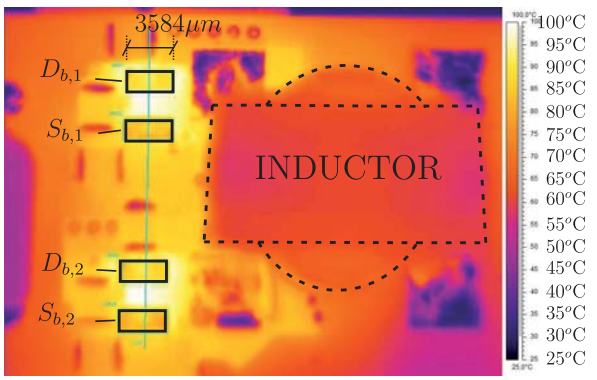

Fig. 10. Thermal measurements showing the GaN HEMT devices and the boost inductor for the PFC rectifier operation with 250 kHz per channel and hence 500 kHz effective switching frequency value. No external cooling mechanism was used.

TABLE IV
Experimental Thermal Results

Device	$f_s = 250$ kHz	$f_s = 500$ kHz
$D_{b,1}$	90.3°C	92.6°C
$S_{b,1}$	85.1°C	86.6°C
$D_{b,2}$	88.6°C	90.6°C
$S_{b,2}$	84.2°C	85.0°C

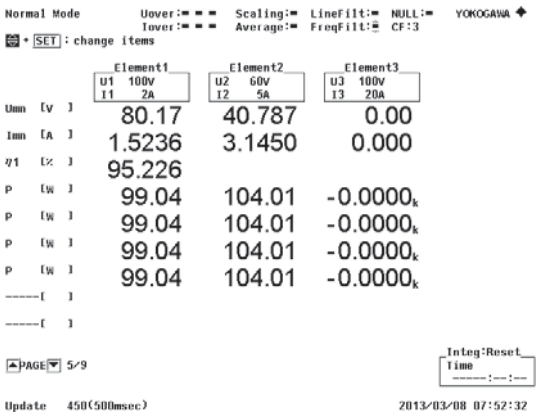

Fig. 11. Measured efficiency of the prototype operating with partial interleaved subcircuit switching frequency of $f_s = 250$ kHz.

Source – Analyzer, and the main external waveforms are shown in Figure 9. The control effectiveness is observed as the input ac current closely follows the sinusoidal input voltage even with a relatively low modulation index.

The switching frequency of the converter was varied in order to verify the influence of this parameter on the temperature of the GaN devices. Two switching frequencies were tested: 250 kHz and 500 kHz. The thermal results are presented in Figure 10, where the infrared image shows the temperature at the main power components for the 250 kHz operation. There, the output power was set to $P_o \approx 75$ W and the maximum measured temperature at the GaN devices surface was 90.3°C. At $f_s = 500$ kHz the output power was also set to $P_o = 75$ W and the maximum measured temperature was 92.6°C, as demonstrated in Table IV. In Figure 11 the efficiency of the prototype operating at $P_o \cong 75$ W with $f_s = 250$ kHz was measured with a Yokogawa power analyzer leading to $\eta \cong 95.23\%$. This measurement includes the losses of the semiconductor and passive devices including the EMI filter components and the dc-link capacitors.

The harmonic spectrum of the filtered phase ac current measured at the input of the built prototype operating with f_s=250 kHz (per device) and consequently f_s=500 kHz effective ripple frequency is shown in Figure 12.

VI. CONCLUSIONS

Wide bandgap semiconductor materials greatly impact Power Electronics converters due to improved electrical performance regarding voltage drops and switching transition times. In addition, such materials are changing the way power

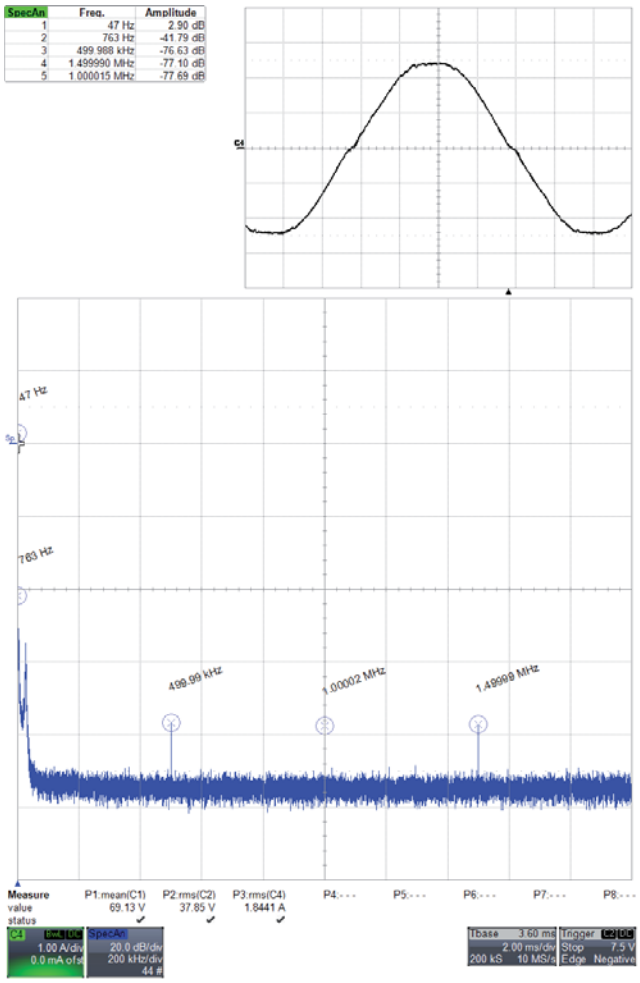

Fig. 12. Measured spectrum harmonics of the current in an interleaved bridge-leg for operation with effective switching frequency of 500 kHz (250 kHz per power device). In this test the PFC rectifier was fed by an auto-transformer connected to a 220 V/60 Hz power mains to avoid the switching noise of the ac power supply.

converters are designed. In this work, a discussion on the status of GaN power devices for PFC rectification applications was presented to introduce the requirements regarding the switching frequency. A brief comparison was carried out at three different switching frequency values (250 kHz, 500 kHz and 1 MHz) showing that PCB area, losses and cooling can be highly improved with GaN devices. The feasibility of very high switching frequencies was identified and the challenges faced by today's most deployed control/modulation solutions, i.e. analog ICs and DSPs, were highlighted. In this context, a very high switching frequency digital control/modulation platform was developed to allow the implementation of a 1 MHz GaN HEMTs-based single-phase two-channel interleaved boost-type PFC rectifier. This was done based on an FPGA. The choice of an FPGA device was made based on the very high switching frequency and the advantages of a digital control implementation. However, as analog ICs and DSPs become appropriate for such frequencies the use of an FPGA will depend on how prices evolve.

Because of the use of two converter channels, the turn-off one of them at light load operation is possible, reducing gate driver and magnetic core losses or a very high efficiency can be attained even at light loads. Experimental results have attested the feasibility of this solution and shown the potential for high efficiency designs even at relatively low converter rated power.

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