ISOLATED SINGLE-PHASE HIGH POWER FACTOR RECTIFIER USING ZETA CONVERTER OPERATING IN DCM WITH NON-DISSIPATIVE SNUBBER

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***Abstract*—This paper presents the study of a single-stage, single-phase, unity power factor converter, isolated by a high frequency transformer, based on a Zeta converter operating in discontinuous conduction mode (DCM). The main feature of the proposed converter is its ability to naturally emulate an apparent resistance to the ac input source, without current sensor or current controller. Circuit operation, theoretical analysis and design example are included in this paper, along with experimental results taken from a laboratory prototype rated at 400W, input voltage equal to 127 V, output voltage equal to 200 V, switching frequency of 25 kHz and efficiency of 92%. In order to reduce the commutation losses and limit the peak voltage across the power semiconductors, a non-dissipative snubber has been included in the laboratory prototype. With the advent of new low losses power semiconductor technologies, such as SiC and GaN, power converters operating in DCM will become very attractive, due to their simplicity and robustness, even for high power applications. This is the main motivation of the study presented hereafter.**

***Keywords* – Ac-dc Converter, Discontinuous Conduction Mode, High-Frequency Insulation, Power Factor Correction (PFC), Single-Stage, Zeta Converter**

I. INTRODUCTION

Two stages power supplies, consisting of a unity power factor front-end rectifier, followed by an isolated high-frequency dc-dc converter. It is the usual architecture in the design of single-phase off-line power supply to power, the vast majority of electronic equipments.

The most popular front-end high power factor single-phase topologies consist of a full-bridge diode rectifier, followed by a dc-dc boost converter [1] and [2] with a current control that makes the input current follows the voltage, resulting in an apparent resistive load.

It is also well known that is possible to emulate a resistive load and a consequent unity power factor without current sensor and current controller, provided that the converter operates in discontinuous current mode (DCM) [3] and [4]. Moreover, some of the basic dc-dc converters, such as flyback, SEPIC and Zeta are isolated by high frequency transformers [5] and [6]. Therefore, these converters are suitable for the design of isolated single-phase high power factor rectifiers or ac-dc converters. The study of these power supplies based on the flyback and SEPIC converters have been already reported in the literature and in some way are becoming popular.

However, the utilization of the Zeta converter in the design of single-stage high power factor isolated power supplies has not been found in the literature so far and this is the main contribution in this paper.

Engineers usually argue that DCM operation causes excessive conduction losses and consequently low efficient and heavy power supplies. However, with the emerging of new power semiconductor technologies, such as SiC and GaN, the conduction losses are becoming very small in comparison with Si based power semiconductors, allowing the design of compact, more efficient and less expensive power supplies operating in DCM.

II. PROPOSED CIRCUIT AND PRINCIPLE OF OPERATION

A. Circuit Description

Figure 1 shows the proposed topology for a single-phase rectifier using a Zeta converter. The circuit is composed by a LC snubber with two diodes (D_{s1} and D_{s2}), an inductor (L_s), and a capacitor (C_s).

The snubber circuit [2], shown in Figure 1, is used to absorb the energy from the leakage inductance (L_{lk}), and reduce the overvoltage across the switch S. Therefore, the transformer should be designed with a leakage inductance as small as possible, to minimize the snubber actuation time.

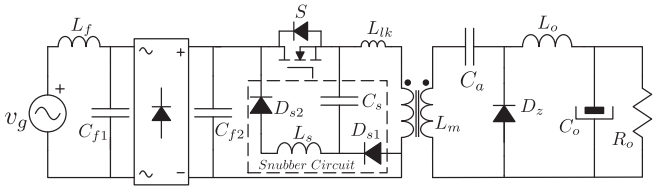

Fig. 1. Proposed circuit using a Zeta rectifier and a LC snubber.

To improve the converter efficiency, the energy absorbed by the snubber circuit, should be regenerated to the input source. However, because the diode bridge is unidirectional, it is not possible to send the energy back to v_g. Therefore, the input filter capacitor has to be divided in two capacitors (C_{f1} and C_{f2}), as shown by Figure 1. The capacitor C_{f2} must be smaller but with sufficient capacitance to maintain the voltage equalization in both filter capacitors, during the energy recovery. The capacitance values were adjusted by simulation to minimize the input current distortion, which resulted in $400\ nF$ and $150\ nF$ respectively, for $L_f = 2\ mH$.

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B. Topological Stages for the Switching Period

Figure 2 shows the topological stages for a switching period on the positive half-cycle of the grid. The circuit stages, common to the standard operation of Zeta dc-dc converter [7], are shown in Figure 2.

The main theoretical waveforms for the switching period at the peak of the input voltage V_p, are shown in Figure 3.

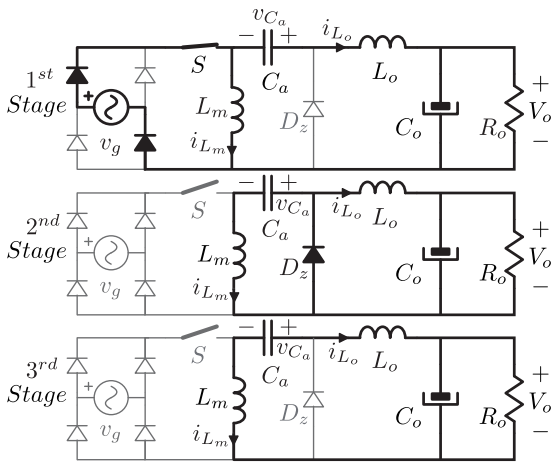


Fig. 2. Topological stages for a switching period; (1^{st}) Magnetizing stage; (2^{nd}) Demagnetizing stage; (3^{rd}) Constant current stage.

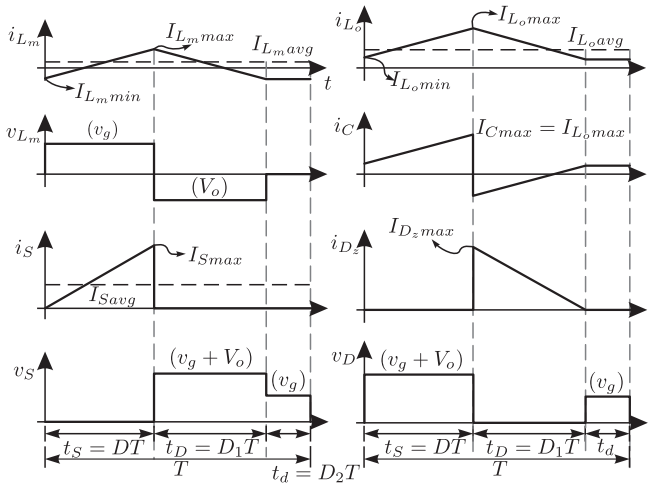


Fig. 3. Main theoretical high frequency waveforms.

C. Topological Stages for the Grid Frequency Period

Figure 4 shows the current and voltage in the switch S and currents through the inductors L_m and L_o, for one grid cycle. These waveforms follow the sinusoidal behavior of the input voltage, therefore, the maximum current and voltage on the switch S occurs at the peak V_p, assuming

$$v_g = V_p \sin(\omega t). \tag{1}$$

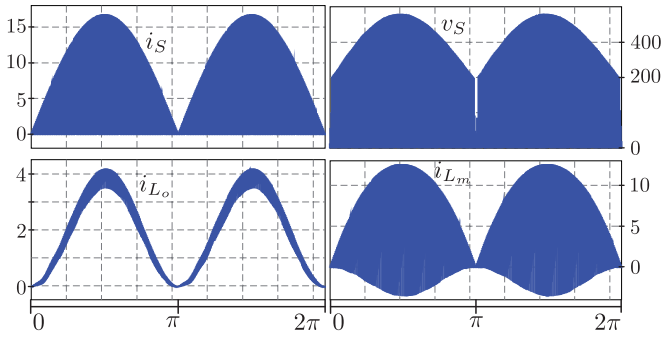


Fig. 4. Waveforms for one grid cycle.

III. MATHEMATICAL ANALYSIS

A. Input Current

Figure 5a shows the input current of the converter, for the positive half-cycle of the grid, which is the same current through the switch S, as shown in Figure 5b. Therefore, for a switching period, the maximum power semiconductor current is defined by

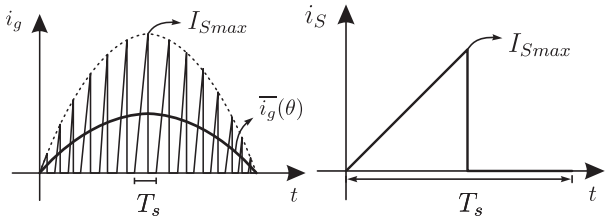
$$I_{Smax} = \frac{V_p}{L_{eq}} DT_s \tag{2}$$

where L_{eq} is the parallel association of L_m and L_o.

On the grid period, the quasi-instantaneous average current value is defined by

$$\overline{i_g}(\theta) = \frac{V_p D^2}{2 L_{eq} f_s} \sin(\theta) \tag{3}$$

where its maximum value occurs when $\theta = \pi/2$.



(a) Input current. (b) Semiconductor current.

Fig. 5. Theoretical waveforms of the input current.

B. Input Converter Characteristic

As previously stated, in DCM this converter has the ability to naturally emulate an apparent resistance. This characteristic can be proved by analyzing the relation between input current and voltage.

The maximum value of the input quasi-instantaneous average current is defined by

$$\overline{I_{g,pk}} = \frac{V_p D^2}{2 L_{eq} f_s}. \tag{4}$$

The apparent resistance seen by the power source is given by

$$R_{in} = \frac{V_p}{\overline{I_{g,pk}}} = \frac{2 f_s L_{eq}}{D^2}. \tag{5}$$

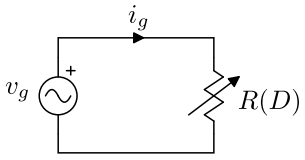


Fig. 6. Apparent resistance seen by the input power source v_g.

The numerator of (5) can be written as an equivalent impedance in function of L_{eq}, therefore, the apparent resistance can be rewritten as

$$R_{in} = \frac{X_{eq}}{D^2\pi}. \tag{6}$$

Based on this analysis, the equivalent circuit can be drawn as shown in Figure 6. The apparent resistance emulated by this converter, depends only of the duty cycle D. The apparent resistance described by (6) proves that this converter operates with natural input power factor correction.

C. Output Converter Characteristic

The output characteristic study of the ca-cc zeta converter is based on the load current parametrization, which is presented by

$$I_o^{'} = \frac{D^2}{G} = \frac{4L_{eq}f_sI_o}{aV_p}. \tag{7}$$

From (7), the static gain of the converter can be written as a function of the duty cycle and the parameterized output current, given by

$$G = \frac{D^2}{I_o^{'}}. \tag{8}$$

The boundaries for the discontinuous conduction mode are given by

$$I_o^{'} = \frac{G}{(1+G)^2} \tag{9}$$

and shown in Figure 7 by the dashed curve. Finally, in Figure 7 is illustrated the behavior of output characteristic, given by (8), for some values of the duty cycle D.

The converter design methodology is based mainly on the abacus shown in Figure 7. With the input and output voltages, the converter gain G can be plotted. On this line, the operating point is chosen, and. from the x axis, the normalized current $I_o^{'}$ is defined. From 7 the converter equivalent inductance L_{eq} is calculated. The L_o inductance is designed for its critical condition, that is at the peak of the input voltage source, therefore

$$L_o = \frac{V_pD}{a\Delta I_{L_o}f_s} \tag{10}$$

where a is the transformer relation and ΔI_{L_o} is the maximum current variation on L_o. Then, the transformer magnetizing inductance L_m is obtained, because L_{eq} is the parallel association of both L_m and L_o, as previously stated.

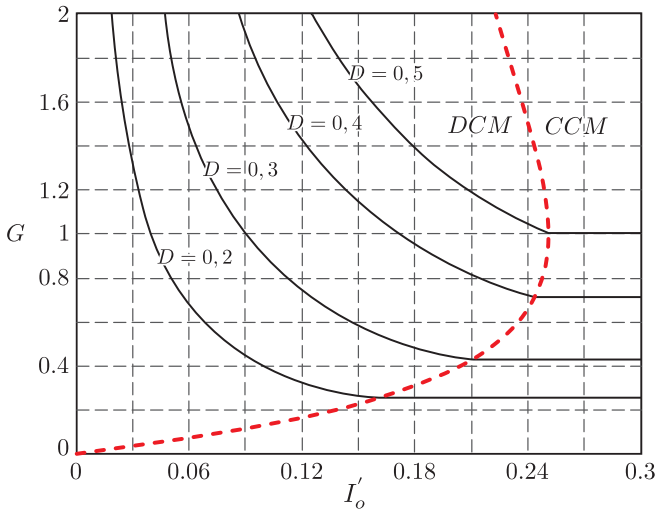


Fig. 7. Output converter characteristic.

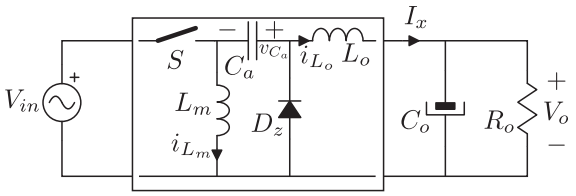


Fig. 8. Equivalent circuit for the converter dynamic model analysis.

D. Converter Dynamic Model

This section analyzes the dynamic response of the output voltage, v_o, for a perturbation on the duty cycle. Figure 8 shows the equivalent circuit used to find the transfer function. Assuming ideal components, the average input power is equal to the output power, described by

$$P_g = \frac{V_pI_{g,pk}}{2} = I_xV_o = P_o. \tag{11}$$

From (11) the current I_x can be calculated. It is equivalent to the sum of the currents through C_o and R_o, in accordance with

$$I_x = \frac{V_p^2D^2}{2L_{eq}f_sv_o} = C_o\frac{\delta v_o}{\delta t} + \frac{v_o}{R_o}. \tag{12}$$

By applying a small perturbation in v_o and D and then linearizing (12) in the operation point, the transfer function for the output voltage control loop can be written as

$$G_v(s) = \frac{\widehat{v_o}(s)}{\widehat{d}(s)} = \frac{2R_oP_{in}}{DV_o}\frac{1}{2+R_oC_os}. \tag{13}$$

The dynamic behavior of (13) is compared with the converter simulation when a small perturbation is applied on the duty cycle, as shown in Figure 9.

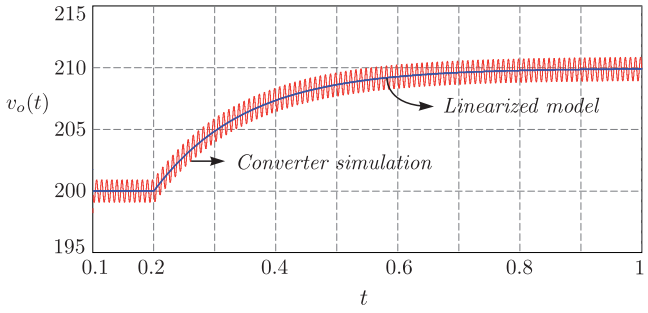


Fig. 9. Dynamic response of the simulated converter and linearized model for a small signal perturbation in D.

IV. SNUBBER CIRCUIT ANALYSIS

A. *Topological Stages Including the Snubber Circuit*

First Stage: When the switch S turns on, the polarity of the voltage on C_s capacitor is inverted and the current i_{C_s} behavior can be determined by

$$i_{C_s} = \frac{V_{C_s}}{\sqrt{L_s/C_s}} \sin(\omega_1 t) \;\; where, \;\; \omega_1 = \frac{1}{\sqrt{L_s C_s}}. \qquad (14)$$

Second Stage: When the current i_{C_s} reaches zero the diode D_{s2} turns off. In this stage the snubber circuit has no actuation on the power circuit of the converter .

Third Stage: As shown in Figure 11, the diode D_{s1} turns on (when $v_{C_f} = v_{C_s}$) and the voltage across the snubber capacitor is decreased, equalizing the voltage in both capacitors (C_f and C_s), connected in parallel.

Fourth Stage: The peak input current will charge the C_s capacitor negatively, through the diode D_{s1}, until

$$V_{C_s} = -V_{C_a min}. \qquad (15)$$

Fifth Stage: This is the resonant stage when the energy storage at the transformer leakage inductance (L_{lk}) is transfered to the snubber capacitor (C_s). The voltage across C_s will increase to its maximum value, given by

$$V_{C_s max} = V_{C_a min} + \Delta VC_s. \qquad (16)$$

In accordance with

$$\Delta VC_s = I_{Smax}\sqrt{\frac{L_{lk}}{C_s}} \qquad (17)$$

the maximum value of v_{C_s} depends on the L_{lk}, so the transformer design and assembly must be optimized to reduce the leakage inductance. The transformer leakage inductance was measured in the laboratory and it was equal to 700 nH.

The voltage over the switch, v_s, in Figure 10, on the fifth stage, has a maximum value which is given by

$$V_{Smax} = V_{C_f min} + V_{C_a min} + \Delta VC_s. \qquad (18)$$

Using (18), the voltage variation across the snubber capacitor can be written as a function of the maximum desired voltage over the switch (V_{Smax}), and the minimum voltages on the capacitors C_f and C_a, accordingly with

$$\Delta VC_s = V_{Smax} - V_{C_f min} - V_{C_a min}. \qquad (19)$$

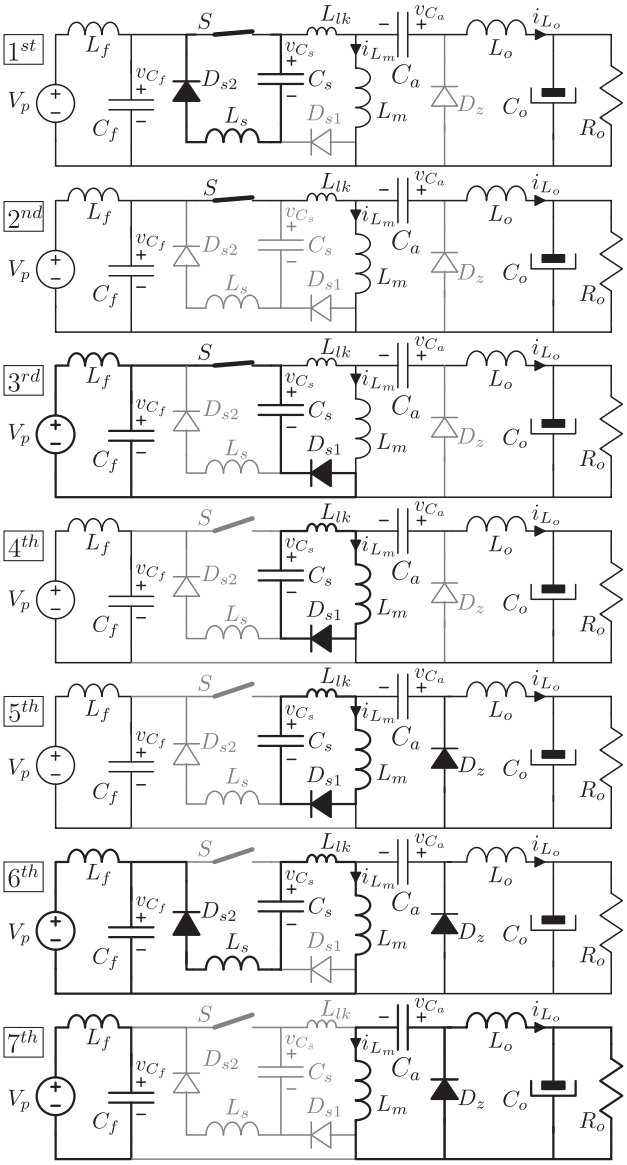


Fig. 10. Topological stages of Zeta rectifier with snubber circuit.

Therefore, based on the principle of energy conservation, the minimum snubber capacitance required is given by

$$C_s = L_{lk}\left(\frac{I_{Smax}}{\Delta VC_s}\right)^2. \qquad (20)$$

As shown in Figure 11, on the fifth stage the diode D_z starts to conduct the load current.

Sixth Stage: When the current through C_s reaches zero the diode D_{s1} is turned off and D_{s2} turns on. The equivalent circuit for this stage is shown in Figure 12.

The energy stored on the previous stage in the capacitor C_s will be now regenerated to the input filter capacitors through diode D_{s2}. The condition to make all the energy from leakage inductance to be regenerated to $C_{f,eq}$ is defined by

$$V_{C_f min} = \frac{\Delta V_{C_s}}{2}. \qquad (21)$$

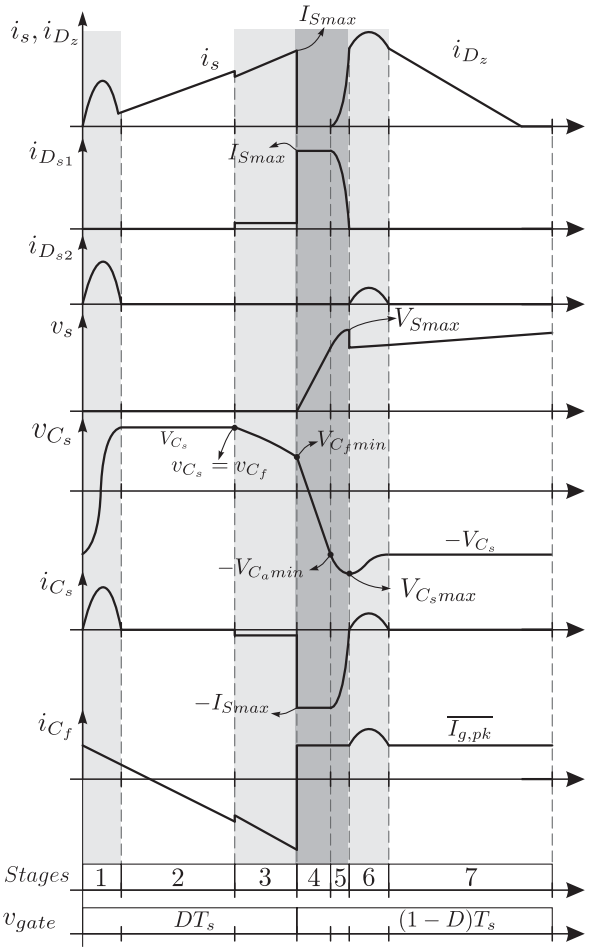


Fig. 11. Main waveforms of converter with the snubber circuit.

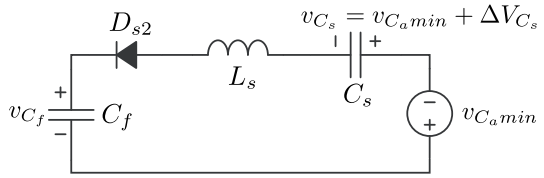


Fig. 12. Equivalent circuit for the sixth stage.

By replacing (21) into (18) results in

$$\Delta V_{C_s max} = \frac{2}{3}(V_{Smax} - V_{C_a min}) \tag{22}$$

for the maximum voltage variation across C_s.

When the current in D_{s2} reaches zero, it is turned off, and the sixth stage is finished.

Seventh Stage: In this stage the snubber circuit has no actuation on the power circuit, and it is equivalent to the third stage on a conventional Zeta converter. Replacing (22) into (20), the minimum capacitance for the snubber circuit is defined by

$$C_{s,min} = L_{lk}\left[\frac{3I_{Smax}}{2(V_{Smax} - V_{C_a min})}\right]^2. \tag{23}$$

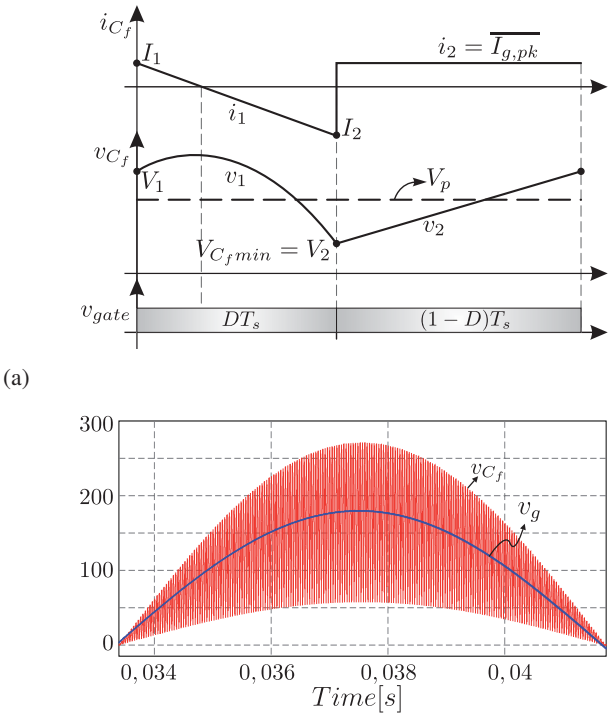


Fig. 13. Theoretical waveforms of the input current. (a) C_f current and voltage on a commutation period, (b) Input source voltage and C_f voltage on the grid period.

The value of the inductance L_s in (14), must be designed to limit the current through the switch S at the first stage. Additionally, when the absolute value of the currents in L_m and L_o become equal, the diode D_z blocks, which characterizes the discontinuous conduction mode.

B. Voltage Analysis on C_f and C_a

As shown in previous analysis, the study of the voltage on the input filter capacitor C_f and the coupling capacitor C_a is very important for the design of the snubber circuit.

The equation for the minimum value of v_{C_f} can be found using the integral boundary condition in the v_{C_f} waveform, on the peak of the input voltage shown in Figure 13b.

Therefore, the minimum value of v_{C_f} is given by

$$V_{C_f min} = V_p - \frac{3I_1 - I_{Smax}D^2}{6C_f f_s}. \tag{24}$$

This study can be extended for the capacitor C_a, that results in

$$V_{C_a min} = V_o - \frac{6I_o - I_{Dmax}(1-D)^2}{6C_a f_s}. \tag{25}$$

With the analysis of the voltage on C_f and C_a the expression for capacitance C_s can be written as

$$C_s = L_d\left[\frac{9C_aV_pD/L_{eq}}{(V_{Smax} - V_o)6C_af_s + 6I_o - (\frac{V_pD}{f_sL_{eq}})(1-D)^2}\right]^2. \tag{26}$$

TABLE I.
Main passive elements of converter.

Transformer inductance	L_m	$212\ \mu$H
Output inductance	L_o	$4,85\ m$H
Capacitor	C_a	$4,38\ \mu$F
Capacitor	C_o	$2,97\ m$F
Filter inductance	L_f	$2\ m$H
Filter capacitor	C_{f1}	$400\ n$F
Filter capacitor	C_{f2}	$150\ n$F
Snubber capacitor	C_s	$15\ n$F
Snubber inductor	L_s	$5\ \mu$H

It is important to mention that the snubber circuit operation does not affect the average voltage in capacitor C_a. However, it will cause a duty-cycle loss that must be considered during the converter design.

V. EXPERIMENTAL RESULTS

Once the theoretical analysis, design and simulation are completed, a prototype was built to verify the operation and performance of the proposed converter. The main components and specifications of the implemented converter are presented on Table I, and a photo of the prototype is shown in Figure 14.

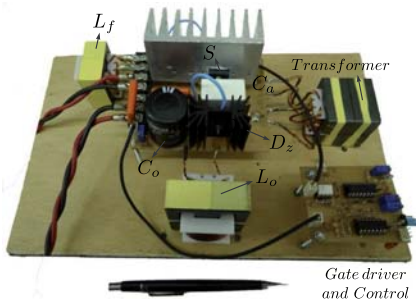


Fig. 14. Proposed converter prototype.

Figure 15 shows the waveforms of current and voltage over the switch S. These waveforms evidence the snubber circuit actuation when the switch turns off, limiting its overvoltage.

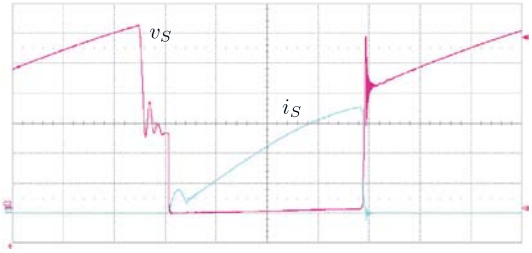


Fig. 15. Current and voltage over the power semiconductor, $v_S = 50$ V/div, $i_S = 5$ A/div, sweep: $50\mu s/div$.

Step load tests of 50% to 100% and 100% to 50% are shown in Figures 16 and 17, respectively. The output voltage step response v_o has a low dynamic, because C_o was designed with a large value to decrease the output voltage ripple, at 120 Hz.

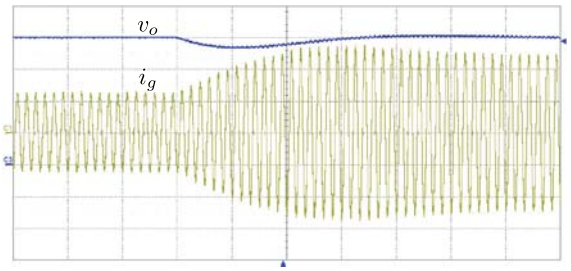


Fig. 16. Transient performance during step change in load of 50% to 100%, $v_o = 50$ V/div, $i_g = 2$ A/div, sweep: 100 ms/div.

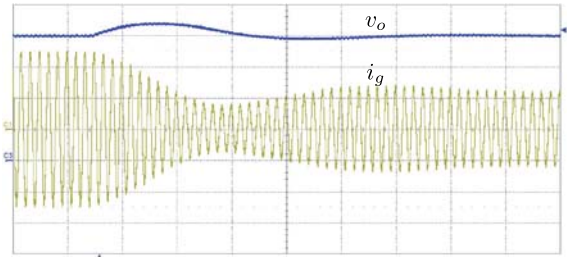


Fig. 17. Transient performance during step change in load of 100% to 50%, $v_o = 50$ V/div, $i_g = 2$ A/div, sweep: $100ms/div$.

Figure 18 shows the input current and voltage at power source, where clearly can be concluded that this converter operates naturally with unity power factor.

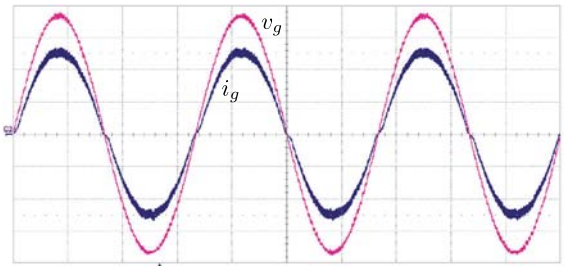


Fig. 18. Current and voltage at the input power source. v_g 50 V/div, i_g 2 A/div, sweep: $5ms/div$.

Figure 19 shows the values of power factor in function of the load. It can be seen that even at low load conditions the power factor stay close to the unity.

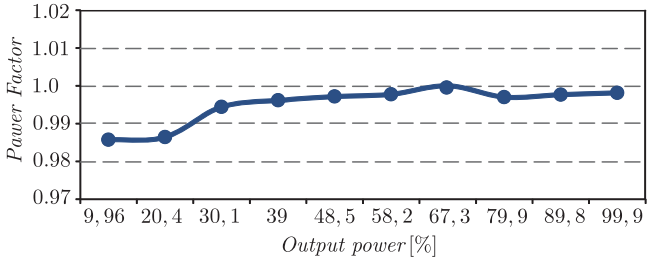


Fig. 19. Power factor in function of the load.

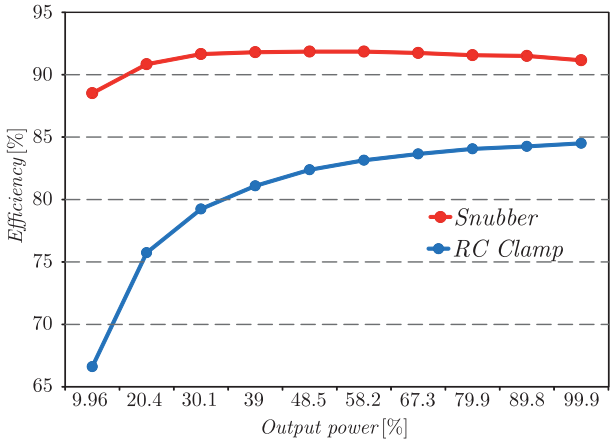


Fig. 20. Measured efficiency with LC snubber and RC dissipative voltage clamp.

Finally, in Figure 20 is shown the improvement of the converter efficiency using a non-dissipative snubber, compared with a dissipative RC clamp circuit.

VI. Conclusion

In this paper it is introduced a single-stage, single-phase, unity power factor isolated power supply, based on the Zeta converter operating in DCM (discontinuous conduction mode). From the theoretical and experimental studies reported in herein, we can draw the conclusions as follows.

- The DCM propitiates resistance emulation, without current sensor or current controllers;
- the theoretical analysis has been validated by the experimental results;
- high efficiency has been obtained in the laboratory, using a non-dissipative snubber, and conventional silicon based mosfet and diodes;
- the proposed converter is suitable for replacing the well known two stage architecture, in many applications, including telecommunication power supplies, domestic electric appliances, battery charges, UPS's, etc.

The proposed converter, despite operating in discontinuous current mode (DCM), with the employment of the emerging silicon carbide based power semiconductors can reach very high efficiency and high power density.

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