SPACE VECTOR MODULATION TECHNIQUES FOR COMMON-MODE VOLTAGE REDUCTION IN THREE-PHASE TRANSFORMERLESS SPLIT-SOURCE INVERTERS

Diego Brum Chaves, Felipe Bovolini Grigoletto

Federal University of Pampa, Laboratory of Energy Processing and Control, Alegrete - RS, Brazil

e-mails: diegobchaves29@gmail.com, grigoletto@gmail.com

Abstract **– Photovoltaic (PV) systems with low input voltage usually employ an input boost converter and an output inverter. Regarding to this issue, the split-source inverter (SSI) provides a single power conversion stage which aggregates boost capability with low switch count. On the other hand, conventional modulation strategies applied to the grid-connected SSI can result in large high-frequency common-mode voltage (CMV). Depending on the parasitic path, the CMV synthesized by the inverter can give rise to large leakage current which must be limited for security reasons. This paper proposes two space vector modulation (SVM) strategies to provide the reduction of high-frequency CMV in transformerles SSI. The first strategy is based on the selection of specific voltage vectors whereas the second strategy employs virtual vectors which correspond to the combination of existing voltage vectors. Furthermore, it is performed an analysis in terms of CMV, leakage current, total harmonic distortion of line-to-line voltages and the maximum achievable modulation index. In addition, a comparison with existing techniques is presented to demonstrate the features of the proposed strategies. Finally, simulations and hardware-in-the-loop results demonstrate the benefits of the proposed techniques.**

Keywords **– Common-Mode Voltage, Leakage Current, Space Vector Modulation, Split-Source Inverter.**

I. INTRODUCTION

Transformerless grid-connected PV inverters have received great attention in recent years [1]–[3]. These systems have interesting advantages such as high efficiency, low cost and reduced size/weight. However, for non-isolated PV systems where the metallic surfaces of PV arrays are grounded, the CMV synthesized by the inverter can originate leakage currents. In its turn, the leakage current increases the grid current distortion, as well as it increments the power losses and makes it difficult to detect ground currents by protective devices [4].

The leakage current in transformerless systems is directly related to the CMV [5] and the path originated mainly by filters and parasitic elements. In order to reduce or eliminate the leakage current, several authors propose different solutions such as converter topologies [6]–[9], CM filters [10], [11] and modulation strategies [12]–[15]. A variety of active and passive filters have been proposed to reduce the CMV [16]–[18]; however, these solutions are often bulky or complex.

A new conversion topology that requires 2 extra switches and 12 extra diodes was proposed in [6]. These additional components significantly increase the cost, the losses, and the size of the conversion system. In [7] an H8 inverter with zero CMV is presented; however, the topology requires additional active and passive elements. Furthermore, this strategy results in low-frequency ripple on the output currents at low modulation index.

Pulse-width modulation (PWM) strategies have been proposed to reduce the CMV in conventional topologies. A modified space vector modulation (SVM) which excludes null vectors in the space vector (SV) diagram was proposed in [13]; the strategy reduces the CMV, however the modulation index is limited within the interval 2/3 to 1. The virtual vectors approach is proposed in [14] to reduce the CMV and to eliminate the third-order component in the CMV. This strategy limits the inverter operation under modulation indices below $\sqrt{3}/2$. In [5], the authors propose a modification in the SV diagram that eliminates the high-frequency CMV. However, the strategy results in a limited modulation index of $\sqrt{3}/3$. In [15], the authors propose a SV modulation for CMV reduction which excludes one of the zero vectors, however the technique is specifically applied to the H7 inverter.

A drawback of the mentioned topologies and modulation strategies is that they need a high input voltage to comply with required grid voltages. To increase the dc-link voltage, conventional architectures include two stages: a boost converter and an inverter [19]. On the other hand, several topologies have been developed to eliminate the dependence on the boost converter [20]. The impedance source inverter (ZSI) proposed in [21] aggregates boost capability to the inverter with reduced switch count. In order to employ the ZSI in transformerless PV applications, in [22] it was proposed a modulation strategy and a topology improvement. Despite this technique mitigate the leakage current, it results in a limited modulation index and a high boosting ratio. On the other hand, in [23] the authors propose a carrier-based modulation strategy to the ZSI. This strategy results in constant CMV, however it is required a four-legs inverter, aggregating more active elements to the power conversion system.

Recently, the SSI proposed in [24] is an interesting topology which merges the boost stage and the inverter stage in a single dc-ac power stage. The SSI employs a conventional inverter bridge and three additional diodes. Furthermore, the SSI does not use the shoot-through states and it employs less passive elements when compared to the ZSI. Some topological

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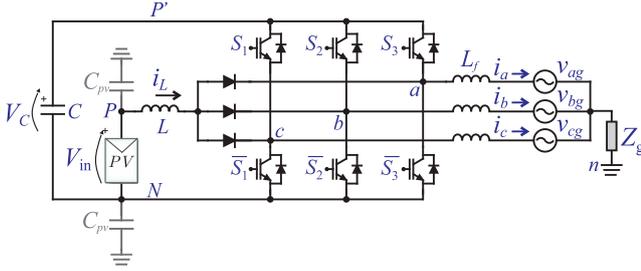Eletrôn. Potên., Fortaleza, v. 25, n. 1, p. 30-40, jan./mar. 2020

Fig. 1. Three-Phase Split-Source Inverter (SSI).

modifications were proposed for the SSI in [25]–[27]. In [28], [29] the authors propose a discontinuous PWM (DPWM) strategy for CMV reduction applied to the SSI. However, this strategy does not result in significant CMV reduction. Moreover, the technique results in low-frequency ripple on the input current and on the dc-link voltage. Thus, until now the analysis and proposition of modulation strategies for CMV reduction in split-source inverters is an open topic that needs to be further investigated.

This paper proposes two space vector modulation strategies for the SSI in order to reduce the CMV and consequently to minimize the leakage current. The first strategy is based on the selection of specific voltage vectors with similar CMV. On the other hand, the second strategy employs virtual vectors in order to expand the linear operating region of the inverter. Furthermore, it is performed an analysis in terms of leakage current, total harmonic distortion of the output voltages and maximum achievable modulation index. Moreover, this paper expands the prior analysis presented in conference paper [30]. This paper is organized as follows: Section II reviews the operation of the SSI, as well as it explains the CMV and leakage current. Section III shows the modulation strategies proposed in [24], [28], [29] and the proposed strategies in this paper. Section IV is dedicated to reporting a comparative analysis whereas Section V brings the hardware-in-loop (HIL) results to validate the theoretical analysis. Finally, section VI presents the conclusion of the paper where it is summarized the features of the proposed strategies.

II. ANALYSIS OF COMOM-MODE VOLTAGE IN SSI

The split-source inverter proposed in [24] is shown in Figure 1. The SSI has eight operating states as conventional full-bridge inverters. Table I shows the inverter states and the corresponding voltages in α-β coordinate frames. When at least one of the lower switches is ON, which corresponds to inverter states V_0 to V_6, the inductor L accumulates energy from the input source. When all the upper switches are ON, which corresponds to the state V_7, the inductor L transfers energy to the capacitor C. Defining the duty cycle as $D = 1 - \Delta t_7/T_s$, where Δt_7 is the dwell time of the state V_7 and T_s is the switching period, the inverter voltage gain can be written as

$$\frac{V_C}{V_{in}} = \frac{1}{1-D}. \tag{1}$$

The term $\Delta t_7/T_s$ corresponds to the normalized dwell time of the vector V_7, and it will be treated as d_7. It is important to mention that some modulation strategies applied to the SSI

can result in oscillatory inverter gain which is dependent on the angle of the voltage reference [24]. Considering this fact, the modulation strategies proposed in this paper keep the dwell time d_7 constant over a fundamental period.

TABLE I
Inverter States, Output Voltage and Common-Mode Voltage

Vectors	S_1	S_2	S_3	v_α	v_β	V_{cm}
V_0	0	0	0	0	0	0
V_1	1	0	0	$\frac{2}{3}$	0	$V_C/3$
V_2	1	1	0	$\frac{1}{3}$	$\frac{\sqrt{3}}{3}$	$2V_C/3$
V_3	0	1	0	$-\frac{1}{3}$	$\frac{\sqrt{3}}{3}$	$V_C/3$
V_4	0	1	1	$-\frac{2}{3}$	0	$2V_C/3$
V_5	0	0	1	$-\frac{1}{3}$	$-\frac{\sqrt{3}}{3}$	$V_C/3$
V_6	1	0	1	$\frac{1}{3}$	$-\frac{\sqrt{3}}{3}$	$2V_C/3$
V_7	1	1	1	0	0	V_C

For security reasons, the metallic surfaces of the PV panels are generally grounded. However, the stray capacitances can offer a path for leakage current which must be limited according to [31], [32]. Furthermore, the CMV synthesized by the inverter excites the leakage current. Therefore, it is very important to quantify the CMV generated the inverter as described in this section.

From the circuit of Figure 1 it is possible to state the voltage between the negative input terminal N and the grounded neutral n by applying voltage Kirchoff law as

$$-v_{Nn} - v_{xN} + v_{xn} = 0. \tag{2}$$

where $x = \{a, b, c\}$. By summing all instances in (2) it can be written

$$v_{Nn} = \frac{1}{3} \sum_{x=\{a,b,c\}} (-v_{xN} + v_{xn}). \tag{3}$$

On the other hand, the voltage between the positive input terminal P and the grounded neutral n can be defined as

$$v_{Pn} = \frac{1}{3} \sum_{x=\{a,b,c\}} (v_{PN} - v_{P'N} - v_{xP'} + v_{xn}). \tag{4}$$

For three-wire balanced circuit, the sum of the line-to-neutral inverter voltages is zero, i.e.

$$v_{an} + v_{bn} + v_{cn} = 0. \tag{5}$$

Furthermore, the voltage $v_{xP'}$ can be written as

$$v_{xP'} = v_{xN} + v_{P'N}. \tag{6}$$

Substituting (5)-(6) in (2)-(3), the common-mode voltage can be written as

$$V_{cm} = -\frac{v_{Nn} + v_{Pn}}{2} = \frac{v_{aN} + v_{bN} + v_{cN}}{3} + \frac{v_{PN}}{2}. \tag{7}$$

As the input can be considered constant, the CMV can be shifted by $V_{in}/2$. Thus, the CMV generated by the inverter is defined in (8), where S_1, S_2 and S_3 represent the switch state

of the inverter.

$$V_{cm} = \frac{V_C(S_1 + S_2 + S_3)}{3}. \tag{8}$$

Figure 2 shows a simplified circuit for the CM path for three-phase inverters, where C_{pv} is the parasitic capacitance of the PV panels, L_f represents the phase output inductive filter and Z_g is the grounding impedance.
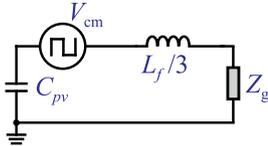

Fig. 2. Simplified CM circuit for the SSI three-phase inverter.

In [33], [34], the CM model for conventional full-bridge topology is covered in detail. As shown in Figure 2, the leakage current flows through the resonant circuit. Hence, the magnitude of the leakage current including the ground impedance Z_g can be defined as

$$|I_{cm}| = \frac{3|V_{cm}|}{\left| \frac{3}{j2\pi f C_{pv}} + j2\pi f L_f + Z_g \right|}. \tag{9}$$

Since the CMV generated by the inverter has a square wave shape with multiple harmonic frequencies, the total leakage current is the sum of all components of the spectrum. Furthermore, the leakage current increases as the switching frequency approach to the resonant frequency of the LC circuit.

III. DESCRIPTION OF THE MODULATION STRATEGIES

A. Modified Space Vector Modulation (MSVM) [24]

The MSVM strategy proposed in [24] is characterized by the use of all vectors in the SV diagram, as shown in Figure 3a.. In this strategy, the dwell time d_7 is constant, avoiding oscillatory gain. This is possible because the state V_0 and V_7 are redundant vectors and their dwell times can be conveniently distributed throughout the switching sequence. The inductance L and capacitance C values can be determined considering only the high-frequency ripple, as

$$L = \frac{DV_{in}}{f_s \Delta I_L}. \tag{10}$$

$$C = \frac{(1-D)I_{in}}{f_s \Delta V_C}. \tag{11}$$

As the dwell time d_7 increases, the maximum modulation index decreases, as demonstrated in (12),

$$m \leq 1 - d_7. \tag{12}$$

On the other hand, a switching sequence is generally designed to result in (i) low output distortion, (ii) a low number of commutations and (iii) easy implementation. Figure 4 shows the drive signals for a switching sequence (sector A) for the MSVM strategy, where d_Z is the total dwell time of the null vectors. Furthermore, Figure 4 presents the common-mode voltage V_{cm}. It can be noted that the CMV assumes all
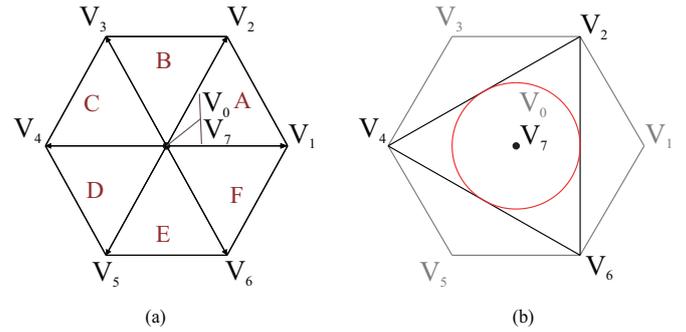

(a)   (b)

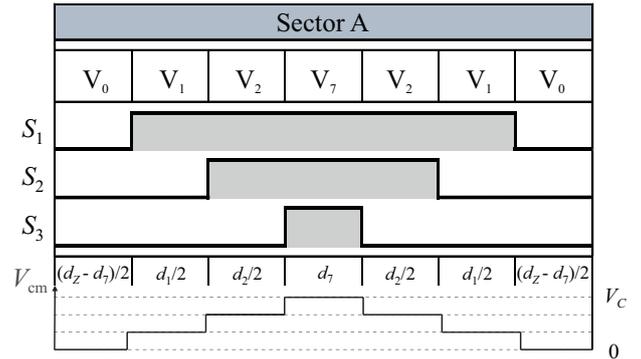Fig. 3. Space Vector diagrams. (a) MSVM. (b) Proposed SSVM.

Fig. 4. Switching sequence for the MSVM.

voltage levels between zero and V_C.

B. Discontinuous PWM (DPWM) [28]

In [28], the authors proposed a modulation strategy that excludes the vector V_0 in order to reduce the CMV. In this way, the voltage V_{cm} presents three levels between $V_C/3$ and V_C. It is important to point out that the modulation strategy results in low-frequency ripple on the input current and dc-link voltage, which increases the required inductance L and capacitance C [24]. Figure 5 illustrates the carrier signals for the DPWM strategy. Considering the region comprised by the interval $0 \leq \theta \leq \frac{\pi}{3}$, the duty cycle can be expressed as

$$D(\theta) = m\cos\left(\theta - \frac{\pi}{6}\right), \tag{13}$$

where $d_7 = 1 - D(\theta)$. The duty cycle variation of the DPWM is bounded by D_{min} and D_{max} given by

$$D_{min} = \frac{\sqrt{3}m}{2}; \quad D_{max} = m. \tag{14}$$

From (13), the average duty cycle can be defined as

$$D_{avg} = \frac{3m}{\pi}. \tag{15}$$

Replacing (15) in (1), the inverter gain as function of the modulation index m is obtained according to (16).

$$\frac{V_C}{V_{in}} = \frac{\pi}{\pi - 3m}. \tag{16}$$

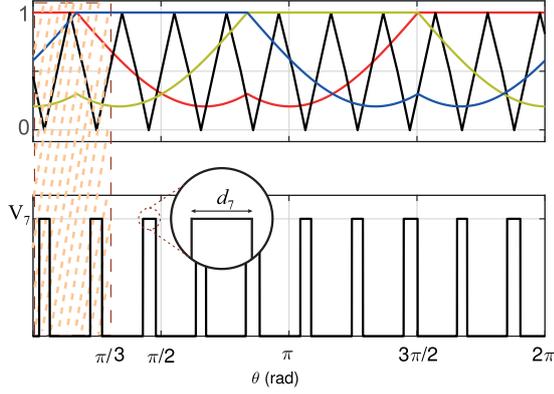The modulation index as function of the peak line-to-neutral voltage and the input voltage is defined as

Fig. 5. Modulating and carrier signals for one fundamental cycle for DPWM strategy, where $m = 0.7$.

$$m = \frac{\sqrt{3}\pi.V_{\phi1}}{3\sqrt{3}.V_{\phi1} + \pi.V_{in}}. \quad (17)$$

where $V_{\phi1}$ is the fundamental component of the line-to-neutral voltage. The low-frequency terms in i_L and V_C are caused by the oscillatory duty cycle modulation. In order to estimate the low-frequency ripple components, only the fundamental terms of $|V_{C1}|$ and $|I_{L1}|$ are considered. They are proportional to the fundamental term of Fourier series of $D(\theta)$ as

$$D_1 = \frac{12m}{35\pi}. \quad (18)$$

By adopting the same considerations presented in [24], the low-frequency ripple components can be estimated as

$$\Delta I_{L1} \approx \frac{D_1 V_C}{6\omega_1 L} = \frac{mV_C}{35\pi^2 fL}. \quad (19)$$

$$\Delta V_{C1} \approx \frac{D_1 I_L}{6\omega_1 C} = \frac{mI_L}{35\pi^2 fC}. \quad (20)$$

The required inductance and capacitance considering both low-frequency and high-frequency ripple are given by

$$L \approx \frac{mV_C}{35\pi^2 f\Delta I_L} + \frac{D_{max}V_{in}}{f_s \Delta I_L}. \quad (21)$$

$$C \approx \frac{mI_L}{35\pi^2 f\Delta V_C} + \frac{(1-D_{min})I_{in}}{f_s \Delta V_C}. \quad (22)$$

From (21) and (22) it is evident that DPWM requires larger passive input elements compared to the MSVM.

C. Proposed Selected Space Vector Modulation (SSVM)

A proper selection of vectors is proposed to reduce significantly the CMV in the SSVM. The switching vectors whose V_{cm} corresponds to zero and $V_C/3$ are excluded, therefore the vectors V_2, V_4, V_6 and V_7 are employed in this modulation strategy. Furthermore, only high-frequency ripple is present on input variables i_L and V_C. Let us suppose a voltage reference to be synthesized by the inverter $u_{Ref} = \begin{bmatrix} u_\alpha & u_\beta \end{bmatrix}$. The dwell times of switching vectors can be defined by the volt-second balance equation, where the time-normalized form can be expressed as

$$\begin{bmatrix} u_\alpha & u_\beta & 1 \end{bmatrix}^T = M \begin{bmatrix} d_2 & d_4 & d_6 \end{bmatrix}^T + M_7 d_7. \quad (23)$$
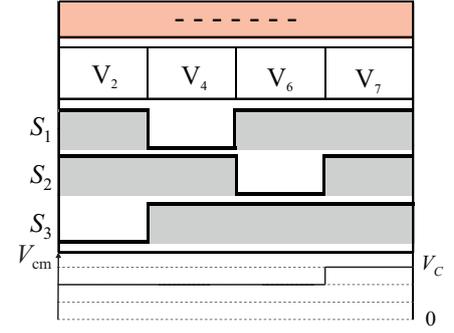
Fig. 6. Switching sequence for the proposed SSVM.

where

$$M = \begin{bmatrix} v_{\alpha2} & v_{\alpha4} & v_{\alpha6} \\ v_{\beta2} & v_{\beta4} & v_{\beta6} \\ 1 & 1 & 1 \end{bmatrix}; \quad M_7 = \begin{bmatrix} v_{\alpha7} \\ v_{\beta7} \\ 1 \end{bmatrix}. \quad (24)$$

By pre-multiplying both sides of (23) by M^{-1}, the dwell times of the vectors V_2, V_4, V_6 can be determined as

$$\begin{bmatrix} d_2 \\ d_4 \\ d_6 \end{bmatrix} = M^{-1} \left(\begin{bmatrix} v_\alpha \\ v_\beta \\ 1 \end{bmatrix} - \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} d_7 \right). \quad (25)$$

where d_7 is constant over a fundamental period and depends on the desired voltage gain. Figure 3b. shows the SV diagram for the proposed SSVM strategy. The dwell times of all the vectors are shown in Table II.

Similarly to the previous strategy, the maximum modulation index is also limited by the operating voltage gain. From (25), it can be derived (26) which results in the maximum modulation index as function of the inductor discharge interval.

$$m \leq \frac{\sqrt{3}}{3}(1 - d_7). \quad (26)$$

Figure 6 shows the proposed switching sequence for the SSVM. Note that the SV diagram has only one sector, therefore this switching sequence is implemented for all inverter operating region. For the proposed SSVM strategy, the CMV is kept within the range between V_C to $2V_C/3$.

D. Proposed Virtual Space Vector Modulation (VSVM)

In order to reduce the CMV and to extend the linear operating region, it is proposed the VSVM where only the vector V_0 is excluded from the SV diagram. The VSVM strategy employs virtual vectors which are a combination of the existing voltage vectors. The virtual vector replaces the vector V_0, resulting in constant voltage gain and reduced CMV, when compared to MSVM strategy. Let us suppose a voltage reference u_{Ref} within the sector A, represented in Figure 7a.. In this sector, the vectors V_1, V_2, V_4 and V_7 are employed. Furthermore, the vectors V_1 and V_4 composes a null virtual vector and the dwell times of the vectors for the sector A are given by

$$\begin{bmatrix} u_\alpha & u_\beta & 1 \end{bmatrix}^T = M_A \begin{bmatrix} d_1 & d_2 & d_v \end{bmatrix}^T + M_7 d_7. \quad (27)$$
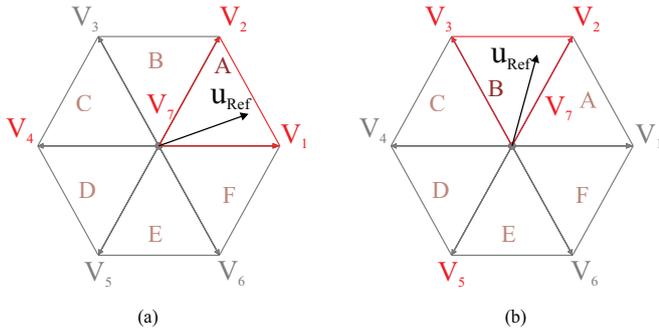
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Fig. 7. SV diagram for the proposed VSVM strategy. (a) Sector A. (b) Sector B.

$$M_A = \begin{bmatrix} v_{\alpha 1} & v_{\alpha 2} & (v_{\alpha 1} + v_{\alpha 4})/2 \\ v_{\beta 1} & v_{\beta 2} & (v_{\beta 1} + v_{\beta 4})/2 \\ 1 & 1 & 1 \end{bmatrix}. \tag{28}$$

where M_A is valid for the sector A and d_v is the dwell time of the virtual vector. By pre-multiplying both sides of (27) by M_A^{-1}, the dwell times can be determined by

$$\begin{bmatrix} d_1 \\ d_2 \\ d_v \end{bmatrix} = M_A^{-1} \left(\begin{bmatrix} v_\alpha \\ v_\beta \\ 1 \end{bmatrix} - \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} d_7 \right). \tag{29}$$

Since the virtual vector is created from two vectors, the dwell time of the virtual vector is equally distributed between the adjacent vectors, as (30).

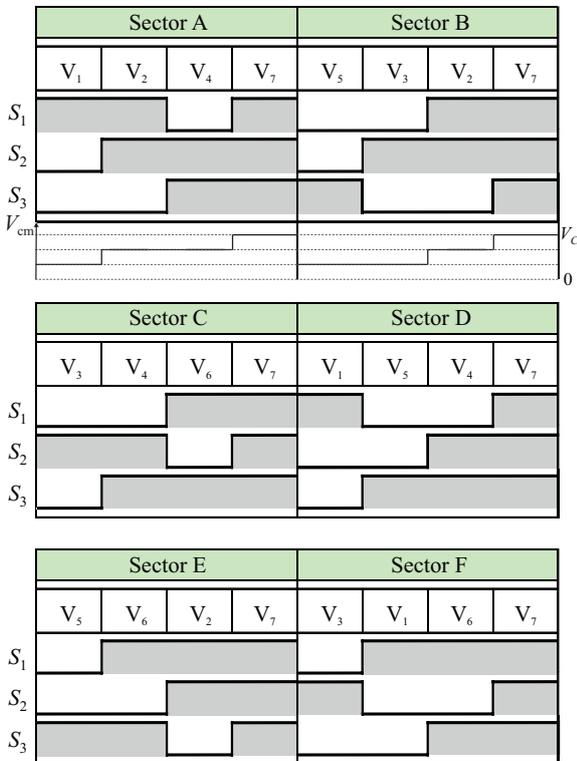$$d_v = 0.5 d_1 + 0.5 d_4. \tag{30}$$

Fig. 8. Switching sequences for the proposed VSVM.

In the sector B, the vectors V_2 and V_5 composes the virtual

redundant vector as shown in Figure 7b.. For the other sectors, the process is very similar. The dwell times of the vectors for all sectors of the SV diagram are shown in Table II. Besides, Figure 8 shows the switching sequences adopted for the proposed VSVM.

Similarly to the previous modulation strategies, the proposed VSVM results in a limited modulation index which depends on the dwell time d_7. The limitation of the modulation index for the VSVM is the same as for the MSVM which is expressed in (12).

IV. COMPARATIVE ANALYSIS

A comparative analysis is performed to verify the merits of the proposed modulation techniques. Figure 9 shows graphically the relationship between the modulation index and the inverter gain for the aforementioned strategies, where the shadowed area below the curve represents the possible inverter operation zone. It is possible to note that the modulation strategies MSVM and VSVM presents greater operation region compared to the SSVM. Furthermore, differently to the other strategies, the operation range of the DPWM strategy corresponds to the points over a line, where its operation is limited to the minimum gain.

Figure 10 illustrates the CMV and the corresponding spectrum for all presented modulation strategies. The MSVM strategy presents a higher CMV component at the switching frequency when compared to SSVM, VSVM and DPWM. On the other hand, the SSVM presents the lowest CMV whereas the VSVM and DPWM present an intermediate value of CMV.

TABLE II
Dwell Times of the Vectors for the Proposed VSVM and SSVM

Strategies	Sectors	Dwell times
VSVM	A	$d_1 = (1 - d_7 + (\sqrt{3}m)\cos(\theta + \pi/3))/2$
		$d_2 = m\cos(\theta - \pi/2)$
		$d_4 = (1 - d_1 - d_2 - d_7)/2$
	B	$d_2 = (1 - d_7 + (\sqrt{3}m)\cos(\theta))/2$
		$d_3 = m\cos(\theta - 5\pi/6)$
		$d_5 = (1 - d_2 - d_3 - d_7)/2$
	C	$d_3 = (1 - d_7 + (\sqrt{3}m)\cos(\theta - \pi/3))/2$
		$d_4 = m\cos(\theta - 7\pi/6)$
		$d_6 = (1 - d_3 - d_4 - d_7)/2$
	D	$d_4 = (1 - d_7 + (\sqrt{3}m)\cos(\theta - 2\pi/3))/2$
		$d_5 = m\cos(\theta - 3\pi/2)$
		$d_1 = (1 - d_4 - d_5 - d_7)/2$
	E	$d_5 = (1 - d_7 + (\sqrt{3}m)\cos(\theta - \pi))/2$
		$d_6 = m\cos(\theta - 11\pi/6)$
		$d_2 = (1 - d_5 - d_6 - d_7)/2$
	F	$d_6 = (1 - d_7 + (\sqrt{3}m)\cos(\theta - 4\pi/3))/2$
		$d_1 = m\cos(\theta - \pi/6)$
		$d_3 = (1 - d_6 - d_1 - d_7)/2$
SSVM	-	$d_2 = (m/\sqrt{3})\cos(\theta - \pi/3) + (1 - d_7)/3$
		$d_4 = (m/\sqrt{3})\cos(\theta + \pi) + (1 - d_7)/3$
		$d_6 = (m/\sqrt{3})\cos(\theta + \pi/3) + (1 - d_7)/3$

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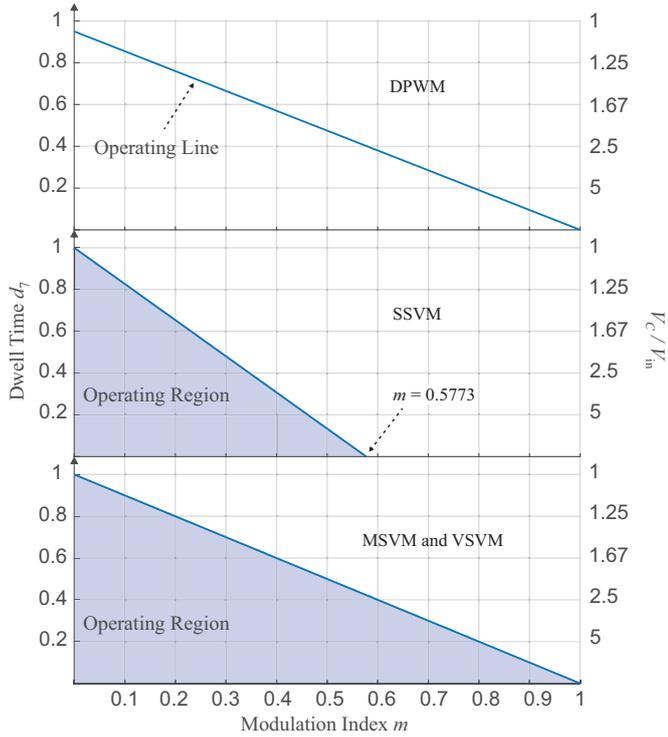Eletrôn. Potên., Fortaleza, v. 25, n. 1, p. 30-40, jan./mar. 2020

Fig. 9. Dwell time d_7 and voltage gain as function of the modulation index.

It can be seen that the strategies MSVM, DPWM and VSVM present third-order components at low frequencies. The amplitude of these components depends on the modulation index; in other words, for low modulation indices, the amplitude of third-order harmonics are low. On the other hand, the CMV components at switching frequency and their multiples do not depend on the modulation index. Figure 11 reports the THD of the line-to-line voltage and the minimum inverter gain (V_C/V_ϕ) as function of the modulation index. Notice that the modulation strategies have different limits for the modulation index, as previously stated. As can be noted in Figure 11, the proposed VSVM and SSVM strategies present higher THD when compared to the MSVM and DPWM strategies. Moreover, the THD of the line-to-line voltage keeps the same behavior for different voltage gains considering a constant dc-link voltage.

The design of the inductive filter L_f is performed to keep the grid current harmonic content at high frequencies under the limits established by grid connection standards [35]. Generally, if the most significant current harmonic component around the switching frequency is under the limits, then its multiple harmonic components will also be within these limits. Figure 11 illustrates the normalized line-to-line voltage magnitude at the switching frequency as function of the modulation index. The grid current at the switching frequency can be approximately defined as

$$I_{\text{fs}} \approx \frac{V_{\text{fs}} \cdot V_C}{2\pi f_s L_f}. \tag{31}$$

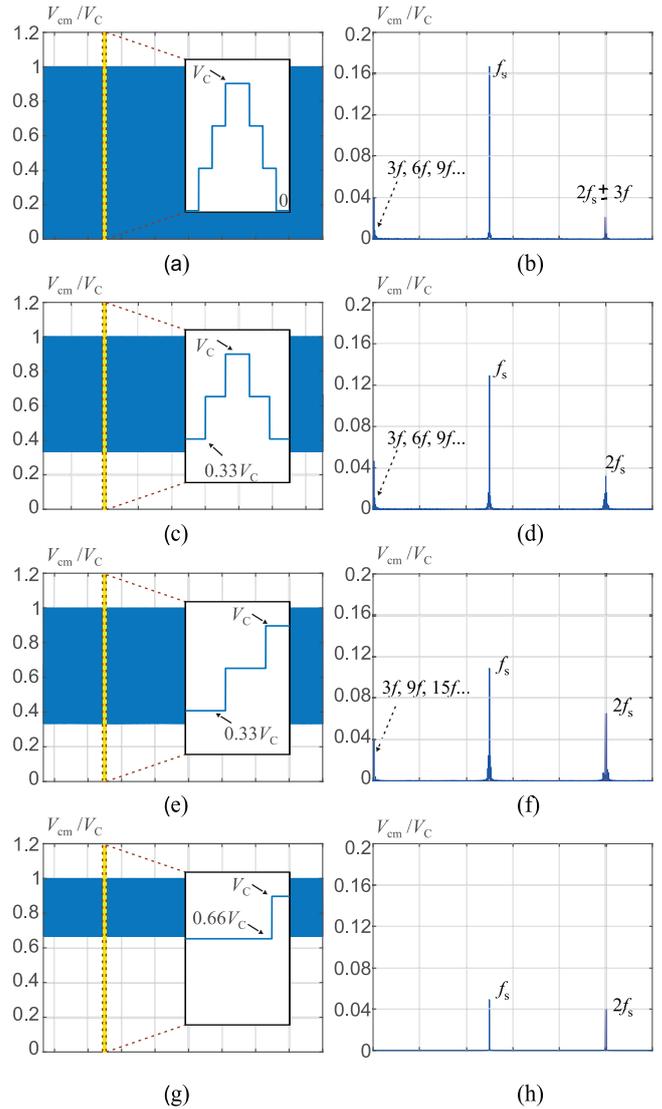$$I_\phi \approx \frac{P}{3V_\phi}. \tag{32}$$

Fig. 10. CMV waveform and corresponding spectrum neglecting the dc component: (a), (b) MSVM. (c), (d) DPWM. (e), (f) VSVM. (g), (h) SSVM.

In order to comply with grid connection standards, the harmonic component of current (I_{fs}) normalized by the fundamental frequency (I_ϕ) must be less than the imposed limits:

$$\frac{I_{\text{fs}}}{I_\phi} = \frac{300V_\phi V_{\text{fs}} V_C}{2\pi f_s L_f P} < H. \tag{33}$$

where H is the percentage value of (I_{fs}/I_ϕ) stipulated by grid connection standards. For instance, according to IEC 61727 [36], the magnitude of harmonic components must be lower than 0.06% (or $H < 0.06$) for harmonic order greater than 23.

$$L_f \geq \frac{300V_\phi V_{\text{fs}} V_C}{2\pi f_s P H}. \tag{34}$$

Remark that most of the harmonic components of leakage current are concentrated around the switching frequency and their multiples, and it was not considered in the filter design. Especially in the MSVM strategy, the highest components are concentrate at twice the switching frequency, instead of the

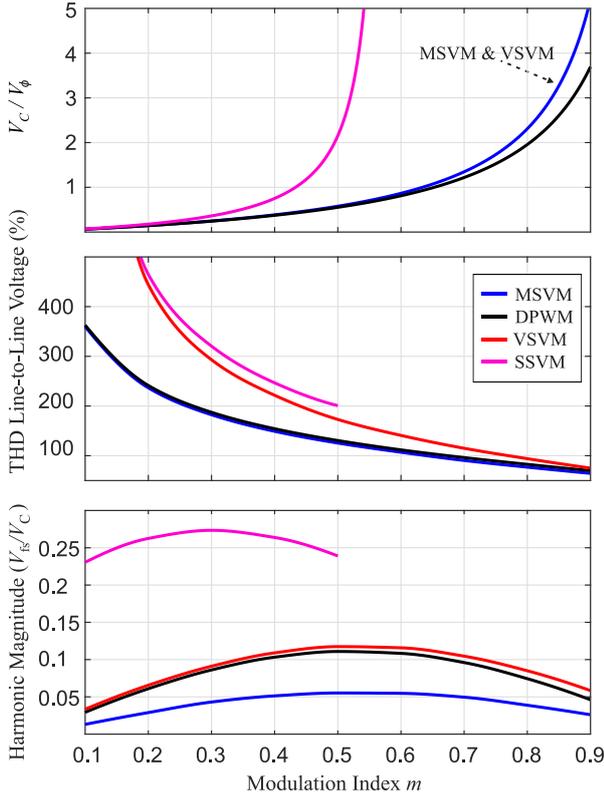Eletrôn. Potên., Fortaleza, v. 25, n. 1, p. 30-40, jan./mar. 2020

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Fig. 11. Minimum voltage gain, THD of the line-to-line V_{ab} voltage and Harmonic amplitude of V_{ab} at switching frequency as function of the modulation index.

first component.

V. HARDWARE-IN-THE-LOOP RESULTS

To demonstrate the effectiveness of the proposed modulation strategies, hardware-in-the-loop results were performed from a Typhoon HIL 402 platform. The DSP TMS320F28379D from Texas Instruments was employed to execute the control and to generate the PWM pulses with a sampling period of $T_s = 40\mu s$. The PWM modulator of the DSP is capable to generate asymmetric pulses for the proposed modulation strategies without any additional logic circuit. The current control strategy in grid-connected mode was performed in synchronous reference frame dq with proportional integral (PI) controllers [37]. Figure 12 shows the diagram block of the implemented system.
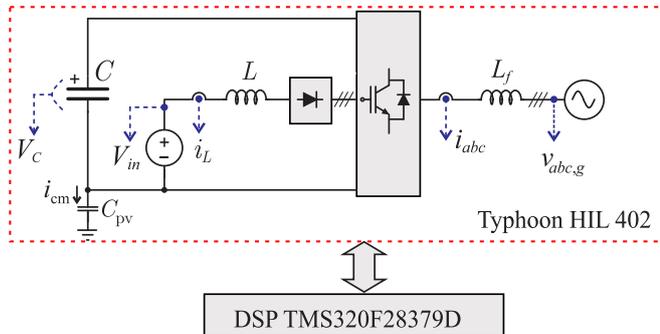

Fig. 12. Block diagram of the implemented system.

TABLE III
Data Parameters

Switching Frequency (f_s)	25 kHz	Line-to-neutral rms voltage	110 V
Filter Inductance (L_f)	5.4 mH	Input Voltage (V_{in})	125 V
DC-Link Capacitance (C)	500 μF	Power (P)	15 kW
Input Inductance (L)	1 mH	DC-link Voltage (V_C)	525−750 V
Parasitic Capacitance (C_{pv})	330 nF		

A capacitor C_{pv} was connected between the negative terminal of the input source and the ground point to emulate the PV parasitic capacitance. This parasitic capacitance depends on the power of the system, the soil where the metal housing is grounded, and especially the PV panel technology [38], [39]. The main parameters of the implemented system are given in Table III. Due to the limited modulation index of the SSVM strategy, the dc-link voltage should be higher than the other strategies. For the MSVM, DPWM and VSVM strategies, the dc-link voltage was $V_C = 525$ V. On the other hand, for the SSVM strategy, the dc-link voltage was $V_C = 750$ V. Therefore, all strategies result in an output line-to-neutral rms voltage of 110 V. The inductive output filter L_f was dimensioned according to (34) for the SSVM strategy, that represents the worst case in terms of high frequency harmonic content.

Figure 13 shows the main waveforms for all modulation strategies when the converter is connected to the grid operating with unity power factor. The results presented are in accordance with the analysis in terms of leakage current. Table IV summarizes the results from Figure 13 and it reports a comparison among the modulation strategies. From the established parameters, only the proposed SSVM resulted in a leakage current inferior to 300 mA which is a limit imposed in [36]. In addition, from the comparison of THD (for L_f=5.4 mH), the SSVM strategy presents the highest value.

The ripple over the variables i_L and v_C is shown in Table IV (for C=500 μF and L=1 mH). As expected, the DPWM strategy presented the highest values of ripple due to the oscillatory gain.

Moreover, PLECS standalone software was employed to estimate the efficiency of the power converter for all modulation strategies. The model of the semiconductors SiC MOSFET BSM180D12P2C101 and input diodes SKN141F were considered for the analysis. It is possible to note that the proposed SSVM has lower efficiency when compared to the other modulation strategies. Finally, Figure 14 illustrates the harmonic components of the output grid currents. The SSVM strategy presented high harmonic components at switching frequency. Despite the low magnitude of V_{fs} for the other strategies (specifically for MSVM and DPWM), there is remarkable harmonic current content at the switching

TABLE IV
Summary of results

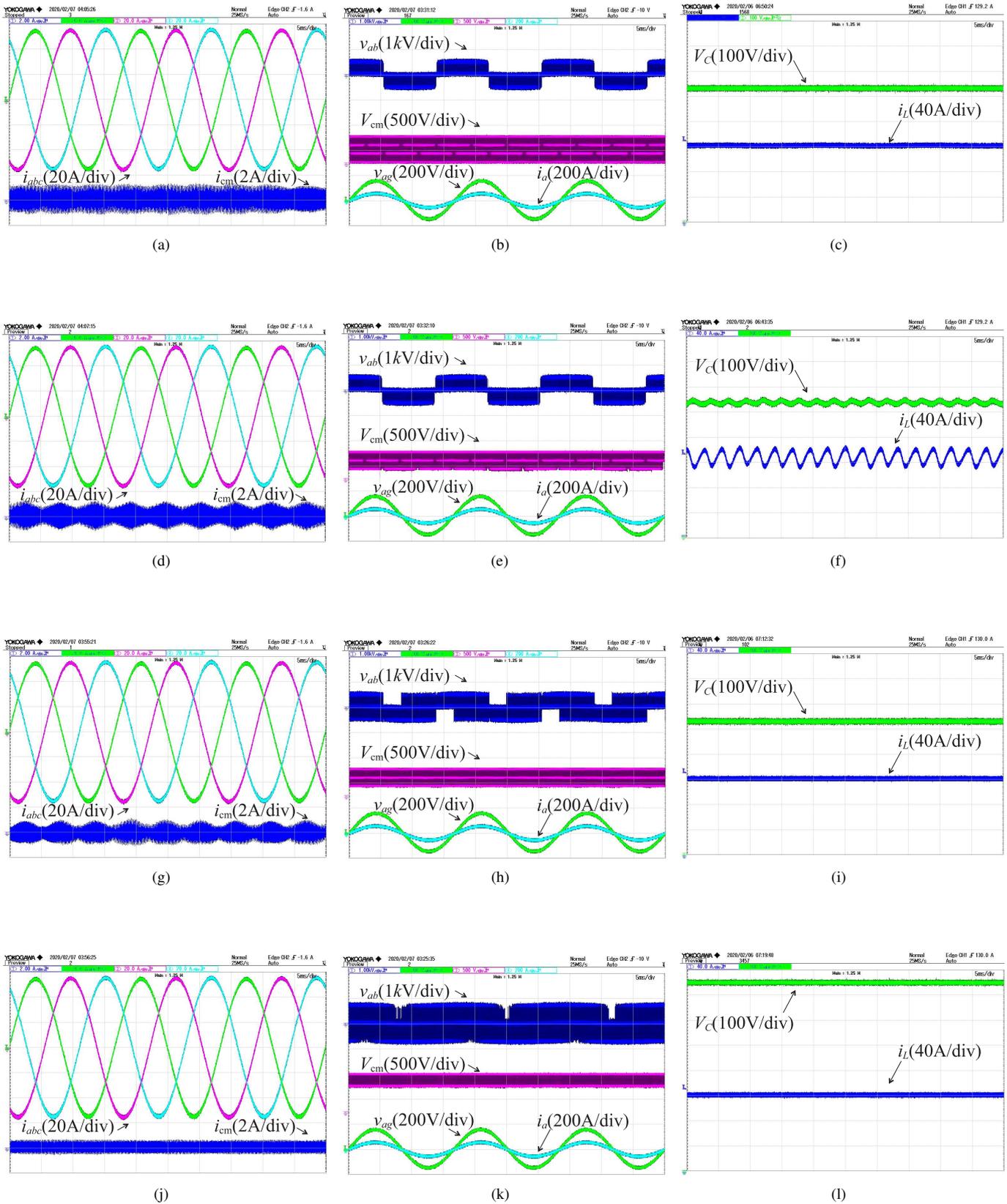| Strategies	MSVM	DPWM	VSVM	SSVM
i_{cm} (rms)	650 mA	497 mA	399 mA	250 mA
THD of i_a	1.37%	1.36%	1.35%	1.55%
ΔI_L	3.17%	17.81%	3.17%	3.47%
ΔV_C	0.43%	1.59%	0.43%	0.30%
Efficiency	97.24%	97.06%	97.05%	96.21%

Fig. 13. Experimental results (time scale 5 ms/div): output grid current i_a, i_b and i_c, leakage current i_{cm}, line-to-line PWM voltage v_{ab}, common-mode voltage V_{cm}, line-to-neutral grid voltage v_{ag}, dc-link voltage V_C and input current i_L. (a), (b) and (c) MSVM. (d), (e) and (f) DPWM. (g), (h) and (i) VSVM. (j), (k) and (l) SSVM.
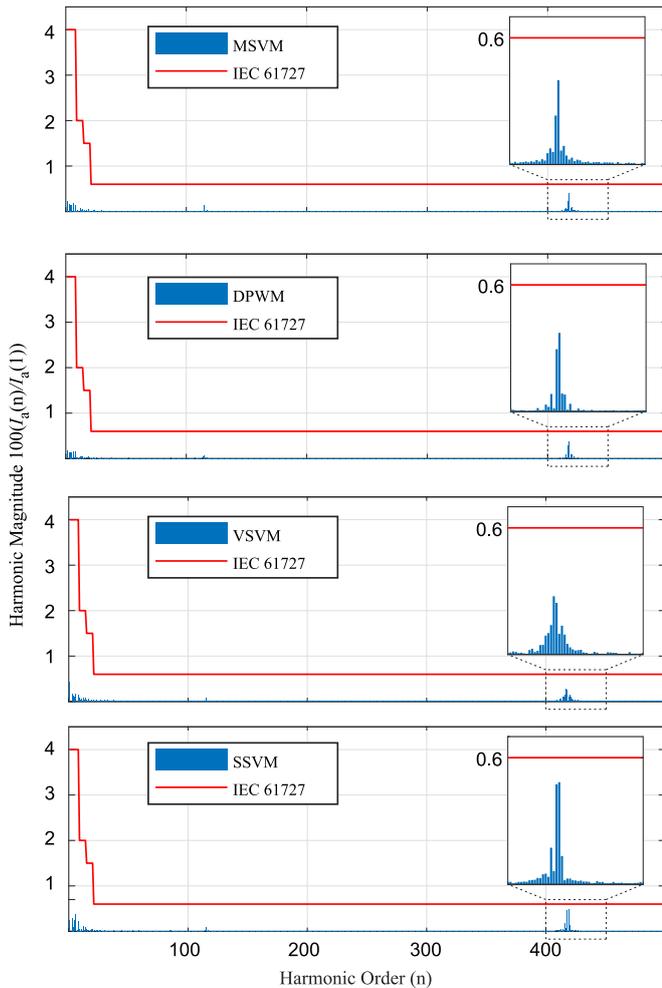
Fig. 14. Harmonic spectra of the grid currents and the limits established in IEC 61727.

frequency due to the leakage current.

VI. CONCLUSION

This paper proposed two modulation strategies with reduced CMV applied to transformerless SSI. The proposed SSVM is based on the selection of specific voltage vectors whereas the proposed VSVM employs virtual vectors that correspond to the combination of existing voltage vectors. The characteristics of the proposed strategies can be summarized as follows:

- both proposed strategies SSVM and VSVM have lower CMV, lower leakage current and higher THD of the line-to-line voltages when compared to those resulted from the MSVM scheme;
- SSVM presents reduced maximum modulation index ($m < 0.577$) whereas the VSVM results in a unitary maximum modulation index;
- SSVM presents higher THD of the line-to-line voltages when compared to the other strategies;
- both proposed SSVM and VSVM strategies present constant voltage gain, resulting in reduced ripple on i_L and V_C;
- VSVM present similar CMV and THD to the DPWM, however the last present oscillatory voltage gain resulting

in high voltage ripple on i_L and v_C;
- all strategies features straightforward implementation since no additional circuits are required for PWM pulse generation.

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BIOGRAPHIES

Diego Brum Chaves was born in Osorio, Brazil, in 1997. He received the B.Sc. degree in electrical engineering from the Federal University of Pampa, Brazil, in 2019. He is currently a master's student at the Federal University of Santa Maria, Brazil. His areas of interest are power electronics and renewable energy conversion systems.

Felipe Bovolini Grigoletto was born in Restinga SÃªca, Brazil, in 1985. He received his B.Sc., M.Sc., and D.Sc. degrees in electrical engineering from Federal University of Santa Maria (UFSM), Santa Maria, Brazil, in 2007, 2009 and 2013 respectively. He is currently a Professor with the Federal University of Pampa (UNIPAMPA), Alegrete, Brazil. His current research interests include renewable energy conversion systems, grid-connected converters and modulation strategies for multilevel converters. Dr. Grigoletto is currently a member of IEEE and SOBRAEP societies.

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