BRIDGELESS BOOST PFC CONVERTER USING THE THREE-STATE SWITCHING CELL

Falcondes José Mendes de Seixas[1], Juan Paulo Robles Balestero[2], Claudiner Mendes de Seixas[3], Fernando Lessa Tofoli[4] and Grover Victor Torrico Bascopé[5]

(1) UNESP – Univ. Estadual Paulista - Ilha Solteira SP, Brazil. E-mail: falcon@dee.feis.unesp.br
(2) IFSC – Federal Institute of Santa Catarina - Chapecó-SC, Brazil. E-mail: juan@ifsc.edu.br
(3) IFSP – Federal Institute of São Paulo - Birigui-SP, Brazil. E-mail: claudiner@ifsp.edu.br
(4) UFSJ – Federal University of São João del-Rei - MG – Brasil. E-mail: fernandolessa@ufsj.edu.br
(5) GTB Power Electronics Research and Technology AB - Kista, Sweden. E-mail: Grover.Torrico@gmail.com

***Abstract* – This paper introduces a bridgeless boost converter based on the three-state switching cell for PFC (power factor correction) applications, whose distinct advantages are reduced conduction losses with the use of magnetic elements with minimized size, weight, and volume. The approach also employs the principle of interleaved converters, as it can be extended to a generic number of legs per winding of the autotransformers and high power levels. The theoretical analysis of the proposed converter is developed, while a comparison with the conventional boost converter is also performed. An experimental prototype rated at 1 kW is implemented to validate the proposal, as relevant issues regarding the novel converter are discussed.**

***Keywords* - AC-DC Converter, Boost, Harmonics, Power Factor Correction, Three-State Switching Cell.**

I. INTRODUCTION

With the advent of telecommunication systems, there has been an increasing demand of more efficient power supplies with some common characteristics e.g. high input power factor, low line current distortion, galvanic isolation between the utility and the load, and regulated dc output voltage.

In low power applications, single-phase power supplies are commonly used and have been already extensively explored in researches. Nevertheless, it is very usual to find a diode rectifier followed by a capacitive filter in many topologies. Such arrangement brings high harmonic distortion to the line current, resulting in low power factor, usually around 0.6.

To satisfy international standards like IEC-61000-3-2 and IEC-61000-3-4, ac-dc conversion stages are required to operate with power factor very close to unity. The arrangement normally used to increase the power factor consists of an input full-bridge diode rectifier followed by a boost converter, as shown in Figure 1 (a). Conduction losses are significant because the current always flows simultaneously through three power semiconductors, i.e., two rectifier diodes and another semiconductor which can either be a diode or one active switch, depending on the operation stage.

The circuit shown in Figure 1 (b), named as bridgeless boost converter in the literature, operates with lower conduction losses [1]-[5] because the current flows simultaneously only through two semiconductors instead of three. It is also noticed that this circuit replaces the pairs of diodes D_1-D_3 and D_2-D_4 with two simple switching cells (named two-state switching cell, or 2SSC), composed by a passive switch (diode) and an active switch. In this circuit, it can be observed that there is a voltage source (capacitive link C_o) between nodes "*a*" and "*b*", while there is a current source connected to node "*c*" (inductive link L_b).

Figure 1(c) shows the proposed single-stage ac-dc converter using the three-state switching cell, defined as "cell B" in [1], [2] and [6]-[10]. When the proposed converter is compared with that shown in Figure 1 (b), the following advantages are addressed:

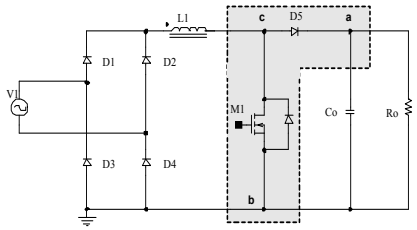
- twice the switching frequency is used for the design of reactive components, implying lower weight and volume;
- the current through each semiconductor is the half of the output current;
- losses are distributed among the semiconductors, leading to a better heat distribution and consequently more efficient use of the heat sink;
- part of the input power is directly transferred to the load (output) through the diodes, mainly when duty cycle is lower than 0.5. As a consequence, conduction and switching losses in the active switches are reduced.

The three-state switching cell allows the parallel connection of switches and therefore inexpensive devices can be used. Furthermore, this topology is suitable when high power is supposed to be processed. The operation of the proposed circuit will be discussed as follows.

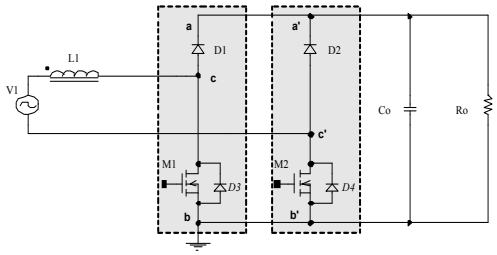
II. OPERATION OF THE PROPOSED CIRCUIT

The proposed boost converter operates in continuous conduction mode (CCM) and can be controlled by using average current mode control technique to achieve PFC. It has two operation modes regarding the value assumed by the duty cycle *D*. In the first mode, when the duty cycle is lower than 50%, there are four operation stages in a switching period of the main switches. The second mode, which occurs when the duty cycle is higher than 50%, has four operation stages in a switching period. When the converter operates in the first half cycle of the line voltage, one cell operates with driven active switches, according to the PWM signals, while the other cell conducts the current flowing through the body diodes of the switches. During the negative half cycle, the opposite occurs.

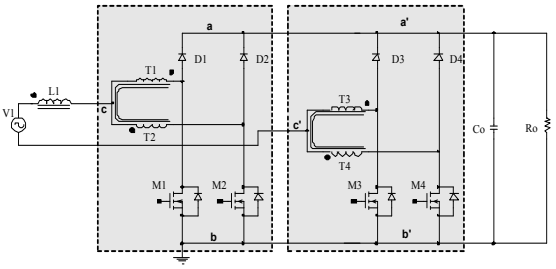
Artigo submetido em 01/12/2011. Primeira revisão em 17/05/2012. Aceito para publicação em 17/05/2012 por recomendação do editor João Onofre P. Pinto.



(a) Ac-dc conventional boost converter



(b) Symmetrical bridgeless boost rectifier



(c) Proposed boost rectifier employing the 3SSC

Fig. 1. High power factor ac-dc converters.

The operation stages are defined by the comparison between the rectified voltage $V_{i(rect.)}$ and the output voltage V_o as a function of the duty cycle D. Thus, when the voltage $V_{i(rect.)}$ is lower than half of the voltage V_o, the converter operates with duty cycle higher than 0.5 (overlapping mode – OM). Otherwise, the converter operates with duty cycle lower than 0.5 (nonoverlapping mode – NOM).

Figure 2 presents the graph of the normalized ripple current through the inductor β as a function of the duty cycle. There are two points of maximum ripple current within the duty cycle range $0<D<1$, namely when D=0.25 and D=0.75. When the duty cycle equals 0.5, the ripple current is zero. At this point, the classic boost has maximum ripple current.

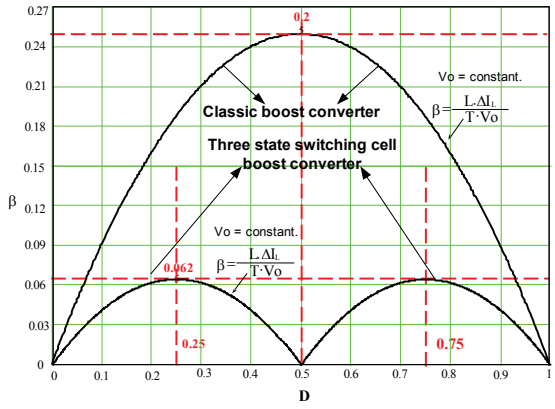


Fig. 2. Normalized ripple current as a function of the duty cycle.

A comparison of the ideal output characteristic between the proposed converter and classical converter is depicted in Figure 3. In this, the voltage gain is shown as a function of the load, considering that the duty cycle is the varying parameter. DCM and CCM refer to discontinuous conduction mode and continuous conduction mode, respectively. Besides, parameter γ is defined as:

$$\gamma = \frac{2 \cdot L_b \cdot I_o}{V_{i(rect.)} \cdot T_s} \quad (1)$$

where I_o is the output current and T_s is the switching period.

Notice in Figure 3 that the DCM region is smaller for the proposed boost converter using two three-state switching cells. The highest load limit (γ) for DCM, in the classic boost, is found at γ=0.25, while the load limit in the boost converter using three-state switching cells is γ=0.0625.

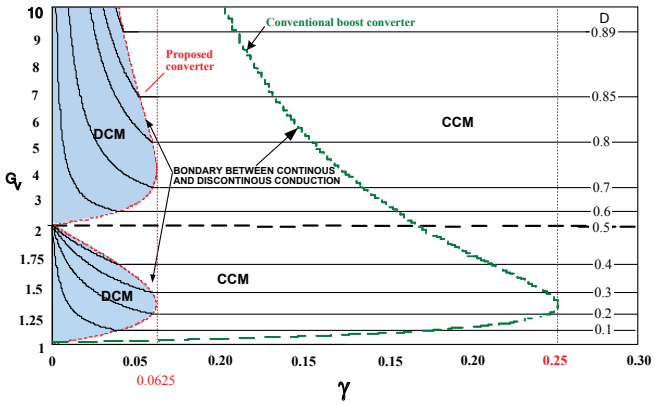


Fig. 3. Static gain curves.

A. Operation in NOM (D<0.5)

The converter operation can be defined according to four operating stages as shown in Figure 4. The respective main theoretical waveforms are presented in Figure 5, where each one of the variables is defined as follows:

$V_{g(S1)}$, $V_{g(S2)}$ – gating signals applied to switches S_1 and S_2, respectively;

I_{Lb} – current through boost inductor L_b, as the maximum and minimum values assumed by this quantity are I_M and I_m, respectively;

I_{S1} – current through switch S_1;

I_{Db1} – current through boost diode D_{b1};

I_{Vo} – current through the output stage, which is the sum of the currents through the output capacitor (I_{Co}) and the load (I_o);

V_{S1} – voltage across switch S_1;

V_{Db1} – voltage across boost diode D_{b1};

V_{Lb} – voltage across boost inductor L_b.

In order to describe the operating stages, the positive half cycle of the line voltage is considered. The behavior of the converter during the negative half cycle is analogous, although switches S_3 and S_4, boost diodes D_{b3} and D_{b4}, and antiparallel diodes D_{s1} and D_{s2} are supposed to replace their respective counterparts i.e. S_1 and S_2, D_{b1} and D_{b2}, D_{s3} and D_{s4}, respectively.

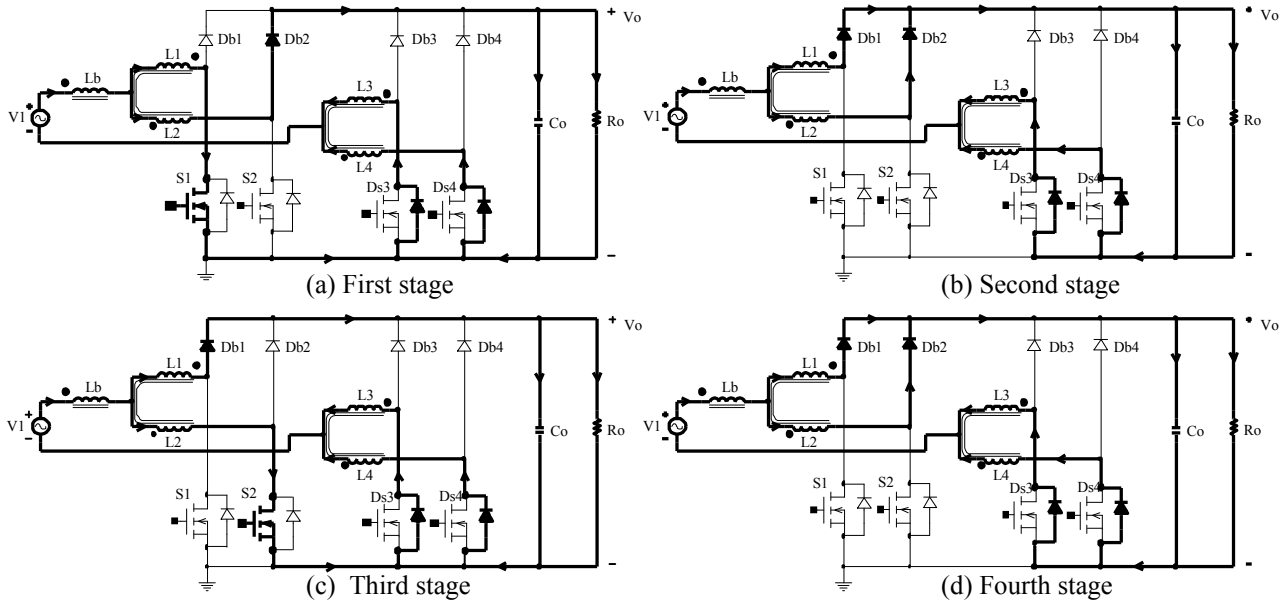


Fig. 4. Operating stages of the proposed boost converter in NOM-CCM considering the positive half cycle of the input voltage.

First stage [t_0, t_1] (Figure 4 (a)): Initially, switch S_1 is turned on, while switch S_2 is turned off. The current through the boost inductor is divided in two parts. The first one flows through L_2 and D_{b2} with energy being delivered to the load. The second one flows through L_1 and S_1. Current sharing is maintained since the turns ratio for L_1 and L_2 is the same. The current through L_b increases linearly. Windings L_1 and L_2 have the same impedance, and the voltages across them are equal to half of the output voltage V_o. The return path of the current to the source occurs through antiparallel diodes D_{s3} and D_{s4}. This stage finishes when S_1 is turned off.

Second stage [t_1, t_2] (Figure 4 (b)): Switch S_1 is turned off while switch S_2 remains off. The voltage across inductor L_b is inverted. Diode D_{b1} is forward biased while D_{b2} remains conducting. The energy stored in L_b during the previous stage is then transferred to the load. The current flow through $L_1||L_2$, according to the given polarity, what causes the magnetic flow in the core to be null. The current returns to the source analogously to the previous stage. This stage finishes when S_2 is turned on.

Third stage [t_2, t_3] (Figure 4 (c)): Due to symmetry of the circuit, this stage is similar to the first one, although switch S_2 is turned on and S_1 remains turned off. Diode D_{b1} keeps conducting and D_{b2} is reverse biased.

Fourth stage [t_3, t_4] (Figure 4 (d)): This stage is similar to the second one, as the same equivalent circuit and operating conditions are valid in this case.

B. Operation in OM (D>0.5)

The converter operation can be defined according to four operating stages as shown in Figure 6, while the respective main theoretical waveforms are presented in Figure 7.

In order to describe the operating stages, the positive half cycle of the line voltage is considered. The behavior of the converter during the negative half cycle is analogous, although switches S_3 and S_4, boost diodes D_{b3} and D_{b4}, and antiparallel diodes D_{s1} and D_{s2} are supposed to replace their respective counterparts i.e. S_1 and S_2, D_{b1} and D_{b2}, D_{s3} and D_{s4}, respectively.

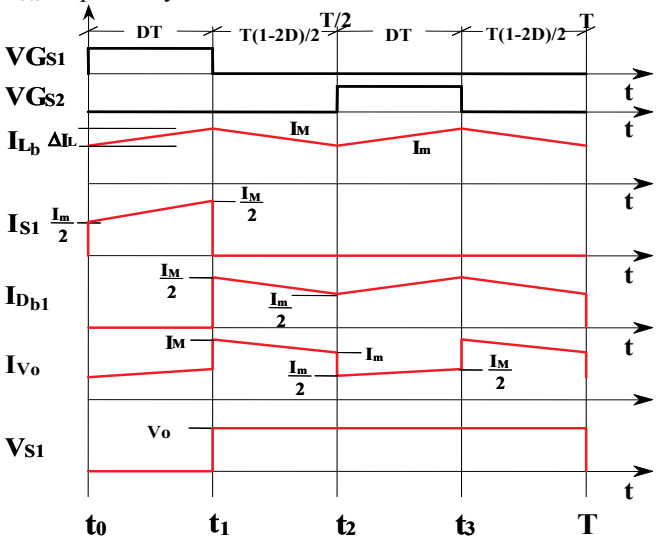


Fig. 5. Main theoretical waveforms for NOM-CCM.

First stage [t_0, t_1] (Figure 6 (a)): Initially, during the positive half cycle of the line voltage, switch S_1 is turned on, while switch S_2 also remains turned on. Boost diodes D_{b1} and D_{b2} are reverse biased. One part of the boost inductor current flows through L_1 and S_1, and the remaining one flows through L_2 and S_2. Considering Kirchhoff's law and the returning path, current flows through L_3-D_{s3} and L_4-D_{s4}. By adopting the same turns ratio for L_1 and L_2, current sharing is maintained. The opposite polarity between the windings causes the voltage across the windings to be null, what represents a short-circuit.

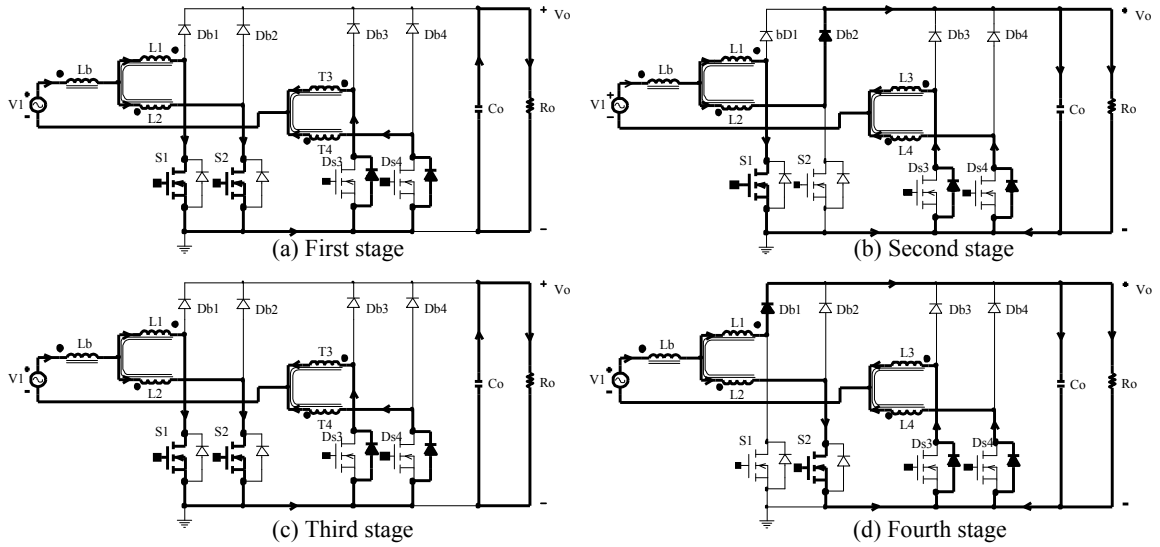


Fig. 6. Operating stages of the proposed boost converter in OM-CCM considering the positive half cycle of the input voltage.

Similarly to the first autotransformer, the voltage across L_3 and L_4 is also null. Moreover, the boost inductor L_b stores energy and the current through it increases linearly. During this stage, only the output capacitor C_o provides power to the load, and it finishes when S_2 is turned off.

Second stage [t_1, t_2] (Figure 6 (b)): Switch S_2 is turned off and S_1 remains turned on. The voltage across the boost inductor is inverted. Diode D_{b2} is forward biased while D_{b1} is reverse biased. The boost inductor current is divided into two parts. Energy transfer then occurs from L_1-S_1 and L_2-D_{b2} to the load. Moreover, the current decreases linearly, transferring the energy previously stored in inductor L_b and also energy from the source to the load. Since L_1 and L_2 have the same turns ratio, current sharing is maintained. Analogously to the first stage, the current returns to the source. This stage finishes when switch S_2 is turned on.

Third stage [t_2, t_3] (Figure 6 (c)): This stage is similar to the first one, although switch S_2 will be turned on while switch S_1 remains also turned on. Boost diodes D_{b1} and D_{b2} are also reverse biased. Similarly to the first stage, only the output capacitor provides energy to the load.

Fourth stage [t_3, t_4] (Figure 6 (d)): This stage is similar to the second one, although switch S_1 is turned off while switch S_2 remains turned on. Diode D_{b1} is forward biased whereas D_{b2} is reverse biased. This way, energy is transferred from the input source and the boost inductor to the load.

III. DESIGN PROCEDURE

The specifications of the converter are listed in Table I and were used in the implementation of an experimental prototype. Some important calculations are performed in order to evidence the loss mechanism of the converter. It is also worth to mention that both conduction and commutation losses are estimated under rated load condition.

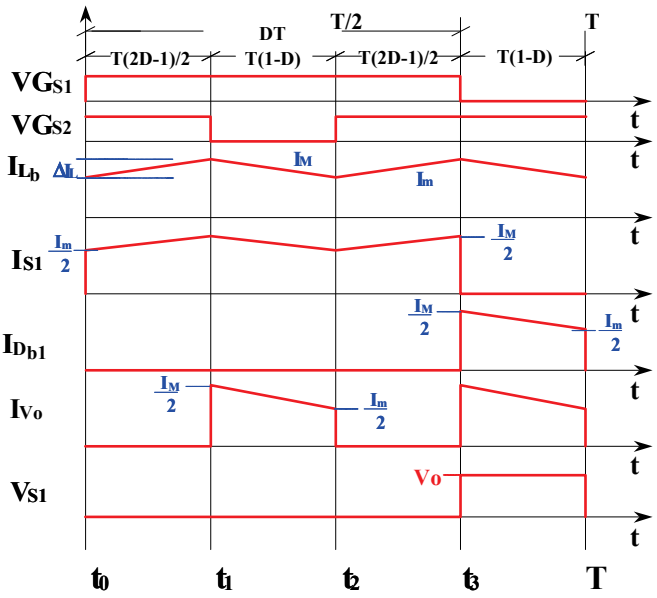


Fig. 7. Main theoretical waveforms for OM-CCM.

A. Preliminary Calculation

Parameter α is the ratio between the output voltage and the peak input voltage and calculated as:

$$\alpha = \frac{400}{\sqrt{2}\cdot 220} = 1.286 \qquad (2)$$

The angle that represents the transition between OM and NOM is:

$$\theta_1 = \sin^{-1}\left(\frac{\alpha}{2}\right) = 0.6982 \text{ rad} \qquad (3)$$

The output current is:

$$I_o = \frac{P_o}{V_o} = \frac{1000}{400} = 2.5 \text{ A} \qquad (4)$$

TABLE I
Design specifications

Parameter	Value
Rms value of the rated input voltage	V_i=220 V
Grid frequency	f=60 Hz
Input current ripple (20% of the input current)	ΔI_{Lb}=1.325 A
Switching frequency	f_{si}=30 kHz
Rated output power	P_o=1 kW
Output voltage	V_o=400 V
Output voltage ripple	ΔV_o=10 V
Expected theoretical efficiency	η=97%

B. Boost Inductor

The boost inductance is given by:

$$L_b = \frac{V_o}{16 \cdot \Delta I_{Lb} \cdot fsi} = \frac{400}{16 \cdot 1.325 \cdot 30 \cdot 10^3} \cong 630\ \mu\text{H} \quad (5)$$

The rms and peak currents through the boost inductor are given by (6) and (7), respectively.

$$I_{Lb(rms)} = \frac{\sqrt{2} \cdot \alpha \cdot I_o}{\eta} = \frac{\sqrt{2} \cdot 1.286 \cdot 2.5}{0.97} = 4.686\ \text{A} \quad (6)$$

$$I_{Lb(pk)} = \frac{2 \cdot \alpha \cdot I_o}{\eta} = \frac{2 \cdot 1.286 \cdot 2.5}{0.97} = 6.627\ \text{A} \quad (7)$$

The core loss in the boost inductor can be obtained from:

$$P_{Lb(core)} = \Delta B^{2.4} \cdot \left(K_H \cdot f_{Lb} + K_E \cdot f_{Lb}^{\ 2} \right) \cdot V_e = 0.036\ \text{W} \quad (8)$$

where ΔB=0.04 is the magnetic flux variation; K_H=4·10^{-5} is the hysteresis loss coefficient; f_{Lb}=2·f_s=60 kHz is the operating frequency of the boost inductor; K_E=4·10^{-5} is the eddy-current loss coefficient; and V_e=42.5 cm^3 is the core volume.

The copper loss in the boost inductor is given by:

$$P_{Lb(copper)} = \frac{\rho \cdot l_t \cdot N_{Lb} \cdot I_{Lb(rms)}^{\ 2}}{n_{Lb} \cdot S_f} = 0.976\ \text{W} \quad (9)$$

where ρ=2.078·10^{-6} Ω·m is the copper resistivity @70° C; l_t=11.6 cm is the average length of one turn; N_{Lb}=30 is the number of turns of the boost inductor; n_{Lb}=5 is the number of wires in parallel; S_f=0.003255 cm is the cross section area of copper wire AWG22.

C. Autotransformers

The maximum voltage across the windings is:

$$V_{T1} = \frac{V_o}{2} = 200\ \text{V} \quad (10)$$

The rms and peak currents through transformer T_1 are given by (11) and (12), respectively.

$$I_{T1(rms)} = \frac{\sqrt{2} \cdot \alpha \cdot I_o}{2 \cdot \eta} = \frac{\sqrt{2} \cdot 1.286 \cdot 2.5}{2 \cdot 0.97} = 2.343\ \text{A} \quad (11)$$

$$I_{T1(pk)} = \frac{\alpha \cdot I_o}{\eta} = \frac{1.286 \cdot 2.5}{0.97} = 3.314\ \text{A} \quad (12)$$

The core loss in each autotransformer can be obtained from:

$$P_{T1(core)} = \Delta B^{2.4} \cdot \left(K_H \cdot f_{T1} + K_E \cdot f_{T1}^{\ 2} \right) \cdot V_e = 1.719\ \text{W} \quad (13)$$

where ΔB=0.15 is the magnetic flux variation; K_H=4·10^{-5} is the hysteresis loss coefficient; f_{T1}=2·f_s=60 kHz is the operating frequency of the transformer; K_E=4·10^{-10} is the eddy-current loss coefficient; and V_e=42.5 cm^3 is the core volume.

The copper loss in the windings of transformer T_1 is given by:

$$P_{T1(copper)} = \frac{2 \cdot \rho \cdot l_t \cdot N_{T1} \cdot I_{T(rms)}^{\ 2}}{n_{T1} \cdot S_f} = 0.976\ \text{W} \quad (14)$$

Where ρ=2.078·10^{-6} Ω·m is the copper resistivity a 70°C; l_t=11.6 cm is the average length of one turn; N_{T1}=24 is the number of turns of the 1:1 transformer; n_{T1}=2 is the number of wires in parallel; S_f=0.003255 cm is the cross section area of copper wire 22AWG.

D. Main Switches

The threshold voltage across one main switch is:

$$V_{S1} = V_o = 400\ \text{V} \quad (15)$$

The average current $I_{S1(avg)}$, the rms current $I_{S1(rms)}$, and the peak current $I_{S1(pk)}$ through the switch are given by (16), (17), and (18) respectively.

$$I_{S1(avg)} = \frac{-\alpha \cdot I_o}{\eta} \cdot \frac{\sin(\alpha)}{(\pi \cdot \alpha)} = -0.787\ \text{A} \quad (16)$$

$$I_{S1(rms)} = \frac{\alpha \cdot I_o}{2 \cdot \eta} \cdot \sqrt{\frac{(2 \cdot \alpha - \sin(\alpha))}{\alpha}} = 1.855\ \text{A} \quad (17)$$

$$I_{S1(pk)} = \frac{\alpha \cdot I_o}{\eta} = 3.314\ \text{A} \quad (18)$$

MOSFET 5015VBR manufactured by APT was then chosen as the main switch, whose characteristics are: drain to source voltage V_{DS}=500 V; diode forward voltage $V_{S(F)}$=1.3 V; drain current I_D=32 A; on resistance $R_{DS(on)}$=0.15 Ω; rise time t_r=14 ns; fall time t_f=11 ns.

The conduction loss regarding each main switch is:

$$P_{S1(cond.)} = V_{S1(F)} \cdot I_{S1(avg)} + R_{DS(on)} \cdot I_{S1(rms)}^{\ 2} = 1.539\ \text{W} \quad (19)$$

The switching loss during turn on and turn off for a single switch is:

$$P_{S1(sw.)} = \frac{f_s}{2} \cdot (t_r + t_f) \cdot I_{S1(avg)} \cdot V_{S1} = 0.118\ \text{W} \quad (20)$$

E. Boost Diodes and Antiparallel Diodes

The reverse voltage across one boost diode is:

$$V_{Db1} = V_o = 400\ \text{V} \quad (21)$$

The average current $I_{Db1(avg)}$, the rms current $I_{Db1(rms)}$, and the peak current $I_{Db1(pk)}$ through the diode are given by (22), (23), and (24), respectively.

$$I_{Db1(avg)} = \frac{\alpha \cdot I_o}{4 \cdot \eta} = 0.828\ \text{A} \quad (22)$$

$$I_{Db1(rms)} = \frac{\sqrt{\alpha} \cdot I_o}{2 \cdot \eta} = 1.461\ \text{A} \quad (23)$$

$$I_{Db1(pk)} = \frac{\alpha \cdot I_o}{\eta} = 3.314\ \text{A} \quad (24)$$

Diode MUR460 was then chosen as the boost diode, whose characteristics are: reverse voltage $V_{D(rev.)}$=500 V; forward voltage $V_{D(F)}$=1.28 V; average forward current I_F=40 A; reverse recovery time t_{rr}=75 ηs.

Estimating the intrinsic resistance of the diode from the curves given in the datasheet as R_D=33 mΩ, conduction loss regarding each boost diode becomes:

$$P_{Db1} = V_{Db1(F)} \cdot I_{Db1(avg)} + R_{Db1} \cdot I_{Db1(rms)}^{\ 2} = 1.13 \text{ W} \quad (25)$$

Switching losses regarding the boost diodes are given as:

$$P_{S1(sw.)} = \frac{1}{2}\left(V_{D(F)P} - V_{D(F)}\right) \cdot I_{Db1(avg)} \cdot t_{rise} \cdot f_s + V_{Db1} \cdot Q_{rr} \cdot f_s = 0.016 \text{ W} \quad (26)$$

Where $V_{D(F)P}$=1.3 V is the maximum value assumed by the forward voltage, t_{rise}=1.5 ns is the rise time of the current through the diode, and Q_{rr}=1.355 ηC is the amount of charge stored in the intrinsic capacitance of the boost diode.

Switching losses regarding the antiparallel diodes of the main switches are not supposed to be neglected and were estimated as 0.248 W for each component by using expression (26).

IV. EXPERIMENTAL RESULTS

To emulate the behavior of a pure resistance, average current mode control is one of the most popular techniques mainly due to the availability of dedicated commercial ICs and will be chosen for this work. The converter was designed according to the parameters listed in Table I, and the components specified in Table II were used. Figure 8 shows the complete designed circuitry.

TABLE II
Power Stage Elements

Parameter	Value
Boost inductor	L_b=630 µH, 30 turns, 5×22 AWG, core E-55/28/21 – IP12
Autotransformers T_1 and T_2	n_1=24: n_2=24, 2×22 AWG, core E-55/28/21 – IP12
Main switches S_1… S_4	MOSFET 5015VBR
Boost diodes D_{b1}… D_{b4}	MUR 460
Output capacitor	C_o=780 µF
Load resistance	R_o=160 Ω

PFC is evidenced in Figure 9, where it is possible to notice the regions in which the duty cycle is less than 0.5 or greater than 0.5.

When the output power is increased from 650 W to 1 kW in Figure 9 (b), the harmonic content of input current I_i is slightly increased. At rated power, the total harmonic distortion of the input current (THD_I) is 12.012% and the power factor is 0.992. This occurs due to the existent asymmetry in the gating signals that drive the main switches. Besides, trade-offs have to be made between reduced harmonic content of the input current and regulated output voltage when designing the control system of the converter.

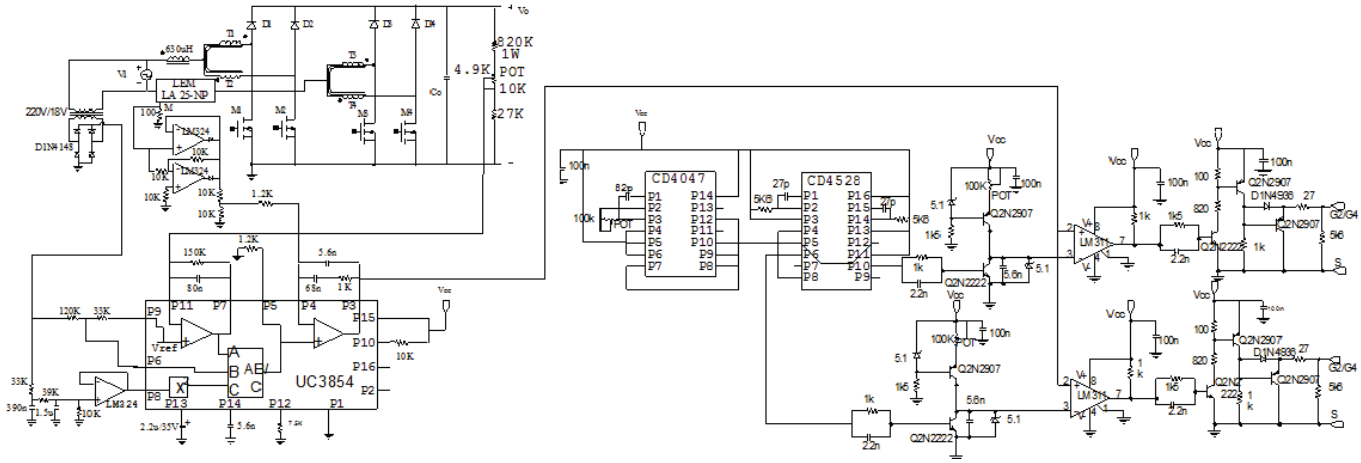
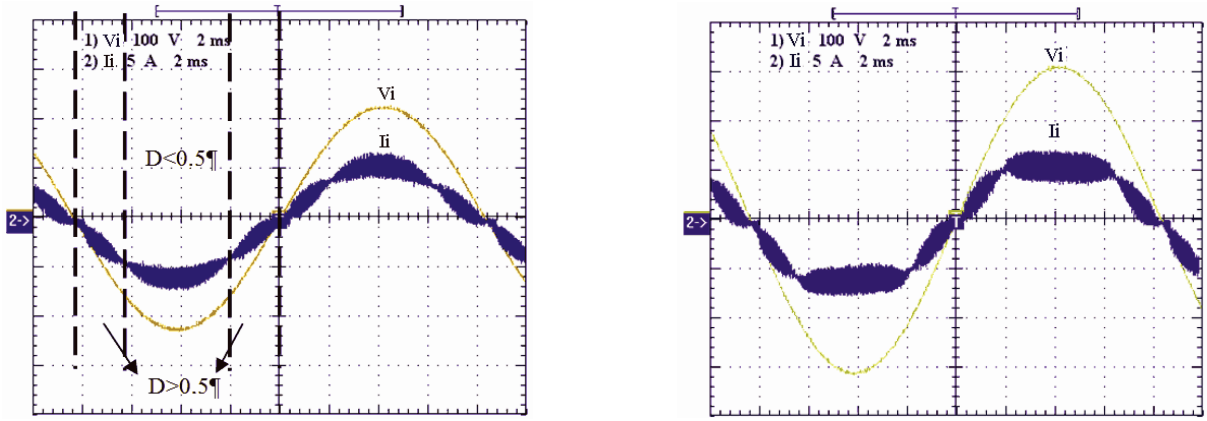


Fig. 8. Complete designed circuitry.



(a) V_i=160 V, P_o=650 W (b) V_i=220 V, P_o=1 kW

Fig. 9. Input voltage and input current.

In order to verify if the proposed converter is in compliance with standard IEC 61000-3-2, the harmonic content of the current in Figure 9 (b) was compared with that established for class A equipment. According to Figure 10, the limits imposed by the aforementioned standard are strictly respected.

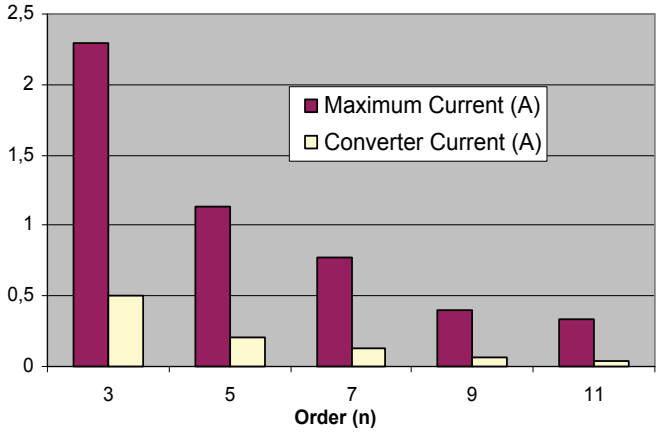


Fig. 10. Limits Imposed by Standard IEC 61000-3-2 for Class A Equipment.

Energy transfer from the source to the load occurs during almost the entire switching period for the 3SSC topology. On the other hand, in the conventional boost converter, it does only occur during part of the switching period, namely when the main switch is off and the output capacitor is charged. It certainly contributes for the reduction of the current peak in the switches causing efficiency to increase. Efficiency is higher than 95% (Figure 11) over the entire output power range, demonstrating the merit of the proposed converter.

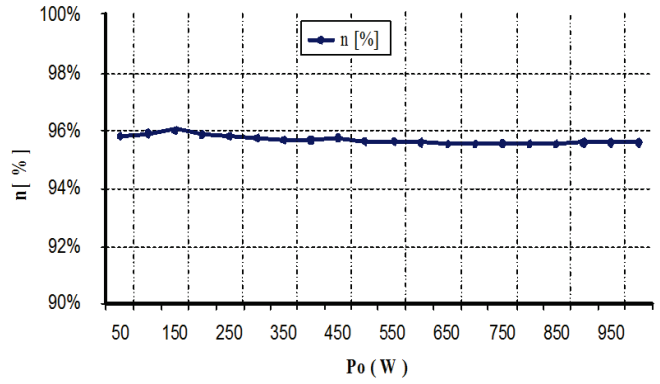


Fig. 11. Efficiency as a function of the output power.

V. CONCLUSION

A bridgeless single phase boost converter based on the 3SSC has been presented. In this approach, the benefits of both bridgeless and three-state cell are incorporated to the converter. In bridgeless topology, conduction losses are minimized because the current always flows through two power semiconductor in series, instead of three as in the conventional boost converter. When the 3SSC is employed, the current is distributed among the semiconductors. Furthermore, only part of the energy from the input source flows through the active switches, while the remaining part is directly transferred to the load without being processed by these switches, i.e. this energy is delivered to the load through passive components, such as the diodes and the transformer windings.

The proposed topology can be seen as the association of the converter shown in and the interleaving technique, since it can be extended to a generic number of legs per winding of the autotransformers. Despite the increase in the number of semiconductors, the voltage and current levels on these devices are reduced, enabling the use of inexpensive switches and simplified command circuits because the isolated drive is not required. In front of these characteristics, its application is recommended for high power levels, analogously to the interleaved boost converter.

In addition, the overall losses are distributed among all semiconductors, reducing the heat sink efforts. The reactive components operate with twice the switching frequency, with significant reduction in weigh and volume of such components.

Considering the operation in NOM (D<0.5) and the same ratings, the following characteristics can be addressed to the 3SSC-based converter if compared with the conventional boost topology:

- increased number of semiconductor elements;
- the operating area in CCM is wider;
- the ripple current through the boost inductor is reduced, as well as the currents through the switches;
- reactive elements are designed for twice the switching frequency, causing the required critical inductance to be smaller, for instance;
- only 50% of the power is delivered to the load through the main switches due to the magnetic coupling between the transformer windings.

The same analysis can be performed for the converter in OM (D>0.5), as the following issues result:

- the input current is continuous, while the current through the output stage, composed by the output capacitor in parallel with the load, is discontinuous;
- the operating area in DCM is narrower;
- the maximum ripple current through the boost inductor is lower;
- the size of reactive elements is reduced because they are designed for twice the switching frequency;
- the current ripple at the point that represents the transition between NOM and OM (D=0.5) is almost null.

REFERENCES

[1] T. N. Santelo, J. P. R. Balestero, F. J. M. Seixas, G. V. T. Gascopé "Novel Single-Stage Boost PFC Using the Three-State Switching Cell", in Proc. *8º Congresso Brasileiro de Eletrônica de Potência*, pp. 292–297, 2005.

[2] T. N. Santelo, J. P. R. Balestero, F. J. M. Seixas, G. V. T. Bascopé, "Three-State Switching Cell for Single-Stage PFC rectifier," in Proc. *Global Congress on Engineering and Technology Education*, pp. 1521–1525, 2005.

[3] R. Tymerski and V. Vorperian, "Generation, Classification and Analysis of Switched-Mode DC-to-DC Converters by the Use of Converter Cells", in Proc. of *IEEE INTELEC*, pp. 181–195, 1986.
[4] R. Martinez and P. N. Enjeti, "A High-Performance Single-Phase Rectifier with Input Power Factor Correction," *IEEE Transactions on Power Electronics*, vol. 11, no. 2, pp. 311–317, Mar. 1996.
[5] F. Souza and I. Barbi "A New ZVS-PWM Unity to Power Factor Rectifier with Reduced Conduction Losses", *IEEE Transactions on Power Electronics*, vol. 10, no. 6, pp. 746–752, Nov. 1995.
[6] G. V. Torrico-Bascopé and I. Barbi, "Generation of a family of non-isolated DC-DC PWM converters using new three-state switching cell," in Proc. *IEEE Power Electronics Specialists Conference*, vol. 2, pp. 858–863, 2000.
[7] G. V. Torrico-Bascopé and I Barbi, "Novo Conversor Elevador CC-CC PWM Não Isolado com Célula de Três Estados de Comutação", in *Proc. of CBA*, pp. 778–783, 2000.
[8] I. Barbi and M. T. Peraça, "The Generation of DC-DC Converters Using New Three-Terminal Multiple-State Cells", in Proc. *IEEE PESC'05*, pp. 2657–2663, 2005.
[9] I. Barbi and M. T. Peraça, "A New Boost DC-DC Converter with A Y-D Commutation Cell", in Proc. *8º Congresso Brasileiro de Eletrônica de Potência*, pp. 625-630, 2005.
[10] I. Barbi and M. T. Peraça, "Three-Level Half-Bridge Inverter Based on the Three-State Switching Cell", in Proc. *VII International Conference on Industrial Applications, INDUSCON'06*, pp. 1-6, 2006.

BIOGRAPHIES

Falcondes José Mendes de Seixas, was born in Jales, SP, Brazil in 1965. He received the B.S. degree in electrical engineering from the Engineering School of Lins, Brazil, in 1988 and the M.S. and Ph.D. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1993 and 2001, respectively.

Currently, he is an Assistant Professor at the Department of Electrical Engineering, UNESP - Univ. Estadual Paulista, Ilha Solteira, Brazil. His research interests include power factor correction, switching mode power supplies, and multipulse transformer applications.

Juan Paulo Robles Balestero, was born on February 20, 1978, in Jales, Brazil. He received the B.Sc. and M.Sc. degrees in electrical engineering from the State University of São Paulo, Ilha Solteira, Brazil, in 2004 and 2006, respectively.

Currently he is a professor with the Federal Institute of Education, Science and Technology of Santa Catarina, Chapecó, Brazil. His research interests include dc-dc converters and converter topologies.

Claudiner Mendes de Seixas, received the B.S. degree in electrical engineering from the Engineering School of Lins, Brazil, in 1991 and the M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1993. After that he worked for approximately 16 years in a company in the infrastructure area for telecommunications.

Currently he is a professor with the Federal Institute of Education, Science and Technology of São Paulo, Birigui, Brazil. His research interests include power quality, power factor correction and green energy applications.

Fernando Lessa Tofoli, was born on March 11, 1976, in São Paulo, Brazil. He received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Federal University of Uberlândia, Uberlândia, Brazil, in 1999, 2002, and 2005, respectively.

Currently, he is a Professor with the Federal University of São João del-Rei, São João del-Rei, Brazil. His research interests include power-quality-related issues, high-power factor rectifiers, and soft switching techniques applied to static power converters.

Grover V. Torrico-Bascopé, received the B.Sc. degree in electrical engineering from San Simón University, Cochabamba, Bolivia, in 1993, and the M.Sc. and Dr. degrees in electrical engineering from the Federal University of Santa Catarina, Florianopolis, Brazil, in 1996 and 2001, respectively.

From 2001 to 2002, he was an Advisor with Emerson Energy System, Brazil, where he developed ac/dc three-phase rectifiers. In 2003, he was a Senior Design Engineer with Emerson Network Power Company, Ltd., Stockholm, Sweden. From 2004 to 2009, he was a Senior Engineer in Power Electronics Designs with the R&D Group, Eltek Valere AB, Sweden, where he developed ac/dc three-phase and single-phase highly efficient rectifiers and dc/dc multioutput supplies to the telecom industry.

Since July 2009, he has been a Senior Design Engineer with GTB Power Electronics Research and Technology AB, Kista, Sweden, where he is a Consultant and is offering new high-efficiency (HE) circuit topologies to the power electronic industry. He has published more than 20 technical papers and is the holder of two patents. His main research areas are in industrial power electronics and creating new platforms with HE topologies for high-power and green energy applications.