SERIES-SHUNT COMPENSATION FOR HARMONIC MITIGATION AND DYNAMIC POWER FACTOR CORRECTION

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Abstract — **This work present the development of an electronically controlled harmonic mitigation device with the property that it can inserts specific series harmonic impedances in the electric system. These harmonic impedances are inserted only at specific frequency (or frequencies). It can be utilized, for example, to active detune power factor capacitor banks, limiting the harmonic current through the capacitors without the need for capacitor voltage rating increase, as it does not significantly changes the fundamental voltage at the capacitors. Also the system can be used for implementation of shunt hybrid harmonic filters or be applied on distributed harmonic mitigation strategies, obtaining a flexible and cost-effective solution even for high power applications. Other advantage of the proposed system is the reduced converter rating necessary for the selective harmonic impedance implementation. The utilization of single turn secondary coaxial transformers, where the secondary side is composed only by the power system cable, for harmonic impedance coupling, gives a significant flexibility to its application, allowing an easy application on existing systems, minimizing the downtime for solution implementation and performance evaluation.**

*Keywords - H*armonics, Active Harmonic Filters, Power Factor, Power Factor Correction, Distributed Compensation.

I. INTRODUCTION

The advance of power electronic applications, stimulated by increasing advances on semiconductor device technologies and continuous stimulus for energy savings and productivity increase in industrial manufacturing processes, has significantly increased the presence of non–linear loads on electric systems, such as frequency inverters, soft-starters, arc furnaces, welding machines, etc. The increase of non-linear loads introduces additional characteristics to the electric power system in such a way that its reliability begins to demand a special care with current and voltage harmonic distortions generated by this type of loads. The harmonic distortion increases the power losses in the electric distribution system, reduces the power factor, shortens the lifetime of equipments and can cause electromagnetic interference.

The solutions normally used for harmonic mitigation are passive solutions, which use only inductors, capacitors and resistors on its construction, active solutions, which utilizes series and/or parallel active filters and hybrid solutions that are a composition of active and passive solutions. The main structure of active filters is composed by a controlled DC/AC converter. The major difficulties of the passive solutions are the reduced flexibility and performance strongly dependent of system impedance and load configuration. The main difficulties of active and hybrid solutions application are the implementation cost, mainly in high current and/or voltage systems, and reliability [1] [2].

Recognizing the fact that it is only necessary to reduce the harmonic content of the electric system to the compatibility levels of the connected equipment, and not completely eliminates the harmonic content, this work proposes a series active harmonic impedance insertion system where impedances are coupled only at specific desired harmonic frequencies. The main feature of the proposed system is the use of a coaxial transformer for harmonic impedance coupling. This coupling transformer eases the application of the proposed system giving a high flexibility to install and evaluate different solution configurations in order to select the best solution according to a desired harmonic mitigation characteristic.
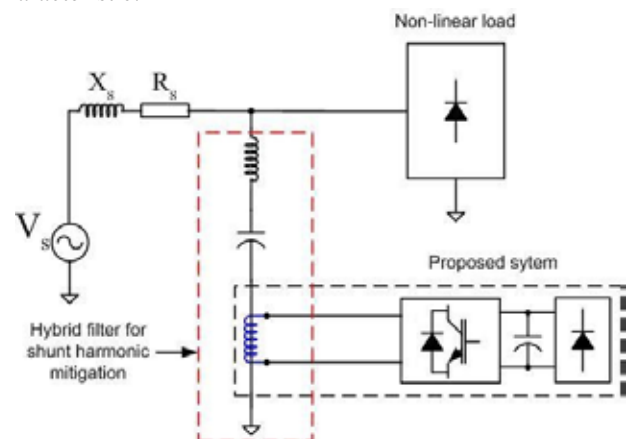

Fig 1. Shunt harmonic mitigation using series hybrid filter.

The harmonic impedances can be used as series or hybrid shunt compensation with the objective to control the harmonic current flow, directing it to paths that do not cause damage to the system components, in distributed compensation implementations, or, as will be discussed in the following sections, to active detuning of power factor

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capacitor banks. The use of the proposed system on hybrid shunt compensation is based on the use of a series hybrid filter [3] as shown in Figure. 1. This application will be discussed on a future work but the application is similar to what was presented in [3] and [4] on the implementation of shunt hybrid filters.

II. DISTRIBUTED HARMONIC COMPENSATION CONCEPT

The concept of distributed harmonic compensation can be understood looking at Figure 2. The concept was previously discussed in [5], considering the use of shunt active filters for harmonic resonance suppression. The objective is to introduce harmonic compensation in different locations in a power distribution system in a way that minimizes the power rating required for mitigation using combined harmonic blocking and sinking characteristics. For example, in Figure. 2, active impedance 1 is used for blocking the harmonic content from the nonlinear sources to flows through the power factor capacitor bank avoiding a resonance condition, for instance. Active impedance 2 is used to introduce a low impedance path to the harmonic flow in order to deviate part of the harmonic current from the nonlinear sources to the source B, sharing the harmonic current with source A, minimizing the harmonic distortion. So, given the flexibility introduced by the proposed coupling mechanism, different approaches can be evaluated directly in the field in order to obtain a cost-effective solution.

This distributed compensation concept is similar as presented in [5] where the use shunt active filters is proposed for distributed harmonic mitigation but the main difference is that in our work we propose the use a device that can be used for both series and hybrid shunt mitigation. In [6], [7] and [8] the concept of distributed impedance is discussed but the focus is on the fundamental frequency power flow control. The focus on this paper is to show the application of the proposed system for harmonic blocking at power factor capacitors.
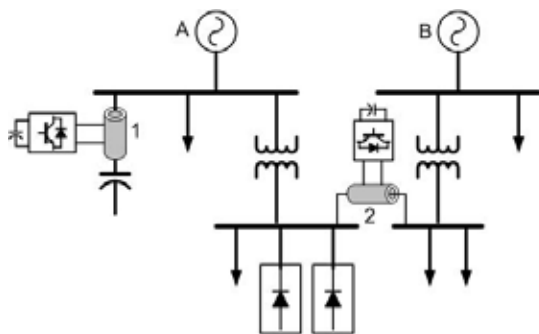

Fig 2. Distributed harmonic mitigation concept.

III. POWER FACTOR CAPACITOR BANKS AND HARMONICS

A. Technologies

Power factor capacitor banks in the industry are not directly associated with the production process and it is common that its necessity is only recognized by industrial managers through penalties applied by the electric energy supplier. Two capacitor technologies are broadly applied in the power factor correction systems: metalized-polypropylene film (dry capacitor) capacitors and oil impregnated polypropylene film capacitors.

Normally, because it cost is about 30% of the oil impregnated capacitor, the metalized polypropylene film capacitor (MPP) is the first choice when the objective is to satisfy power factor requirements imposed by utility companies. The manufacturers of this capacitor technology normally recommends its utilization with maximum harmonic levels in range of 10-15% in current, or 2-5% in voltage, and is very common that the application of power factor capacitor banks results in higher distortion levels when significant nonlinear loads are present, leading to frequent capacitor failures.

B. Cost considerations about power factor correction when harmonics are present

In order to clarify the necessity of cost effective solutions it is interesting to do a cost comparison considering solutions beginning from pure power factor capacitor banks, going to the alternatives where harmonics are treated in a increasingly technology complexity and mitigation performance [2]. Table I shows the cost comparison data which was based on reactive power compensation demand of 200kVAr at 440V rated line voltage and considering that the first case implies on resonance condition. Here will not treat the detailed case study but we will consider a sample scenario commonly found in industry as described in [2]. The costs were obtained from price quotes from manufacturers located in Brazil.

TABLE I
Power factor and harmonic solution cost comparison

	Solution	Capacitor Technology	Cost (%)	Weight (%)
1	Power Factor Capacitor Bank (4 stages)	MPP	100	100
2	Power Factor Capacitor Bank (4 stages)	Oil Imp.	176	178
3	Detuned Filter (4 stages)	MPP	200	376
4	Tuned (only at 5th harmonic)	Oil Imp.	333	475
5	Active Filter + Power Factor capacitor bank	MPP	542	347

The first case presented in table 1 is the base condition where the cheapest power factor capacitor bank is installed but the operation results on an unacceptable harmonic condition for the MPP capacitors. The second solution is an option where the MPP capacitors are replaced by oil impregnated capacitors where it is possible to provide fundamental frequency reactive compensation disregarding the harmonic effects on the system components, "a live with" approach. Oil impregnated capacitors are designed to withstand high harmonic distortion and are the primary choice for use in passive harmonic filters.

The third option is based on the use of MPP capacitors with detuning reactors avoiding the harmonic content to flow through the capacitors. Solution four is the implementation of a tuned LC filter that provides the required reactive energy and also works as a shunt sink for the most harmful harmonic

frequency component. This solution is based on oil impregnated capacitors and series reactors which are carefully designed to handle the additional losses caused by the current harmonic content. The reactor is a critical component on this solution. It increases significantly the volume and solution cost and is highly recommended to monitor its temperature in order to avoid thermal failure. It is important to note that solutions 3 and 4 uses one reactor per capacitor stage, so, for instance, a twelve stages bank will require twelve reactors for solution implementation.

Solution 5 is based on an active shunt filter, responsible for harmonic compensation, in combination with a MPP capacitor bank for power factor correction. The active filter current was specified to be 100A and it is capable to reduce the current harmonic distortion from 50 to 5%, on a 200kVA base.

The scenario shown in Table I is very challenging, from a cost point of view. It demonstrates that a power factor compensation system can have a wide cost range and clearly shows why some industrial managers prefers to include capacitor replacement cost into the maintenance budget, instead to advance in a costly harmonic study and new mitigation equipment that will not directly influence the productivity. Also, as the construction area is a costly resource, it is difficult to get the needed area for installation of any big and heavy equipment, especially in old installations.

As shown in [1] and [2], not necessarily the most costly solution is the best suitable for a specific case, but, even the most simple harmonic "live with" solution has a significant cost increase compared with the basic reactive power factor solution. Our proposal is to introduce an alternative with high application flexibility in order to obtain a cost-effective solution for harmonic mitigation, obtaining the advantages of the detuned and tuned filters but with better cost and volume characteristics. Also the coupling system is designed to allow a fast field evaluation of different configurations in order to choose the more effective solution for each specific case.

IV. ACTIVE HARMONIC IMPEDANCES

A. General Description

The active harmonic impedance proposed here is a controlled source implemented using a static DC/AC converter, implementing a specific relationship between the current and voltage flowing through the secondary of a coupling transformer. This relationship is defined independently from fundamental frequency, for one or more harmonic frequencies in the electrical system.

The major innovative characteristic proposed on this work is the flexibility introduced by the utilization of coaxial harmonic impedance coupling transformer, as can be shown in Figure 3. This coaxial impedance coupling system eases the possibility of implementation of series distributed compensation. In [6] a similar coupling system was discussed for application in distributed fundamental frequency power flow control, proposed in order to obtain flexibility to improve renewable energy market.
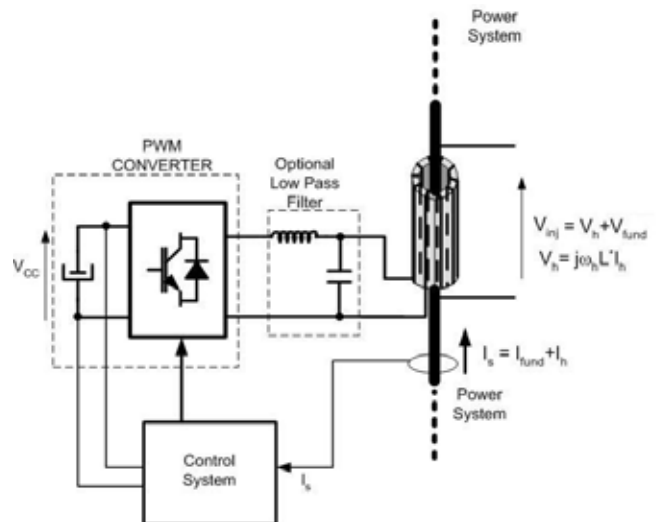

Fig. 3. General diagram of the proposed harmonic impedance.

Also the controllability introduced by the system allows the use of a single system per phase for detuning (or tuning) a capacitor bank composed of several stages, instead of the use of one reactor per stage for detuning or shunt filter banks implementation. As typical industrial electrical loads changes during the day accordingly with the production stages, typical automatic capacitor banks used for reactive compensation and filtering uses up to 12 capacitor stages in order to obtain an efficient compensation at any load demand. Each capacitor stage uses a dedicated reactor in detuned and tuned systems which lead to costly and heavy reactive compensation systems. It is interesting to note that the single phase approach gives the advantage to treat unbalanced harmonic conditions since each phase is considered and compensated independently from the others

The optional LC filter shown in Figure 3 has the objective to reduce high order harmonics that results from the PWM waveform supplied by the converter. As it forms a LCL filter combined with transformer leakage inductance, it must be carefully designed in order to avoid resonance. The design objective is to have a cut-off frequency low enough to attenuate harmonic components near the switching frequency and sufficiently above the synthesized harmonic components to avoid resonance. The design of this LC filter will be treated in a future work. The experimental results presented at section VI use only a small inductor (22µH) at the output of the converter.

Figure 4 shows a block diagram of the proposed system. The transformer secondary current (electrical system power cable) I_s is measured and a PLL algorithm is used to obtain the fundamental frequency current component amplitude and phase. The estimated fundamental current - I_f is subtracted from the measured current and the result – I_h (harmonic component) is directed to another PLL input, tuned to estimate the amplitude and phase of the desired harmonic frequency. The PLL algorithms are discussed in section V.C.
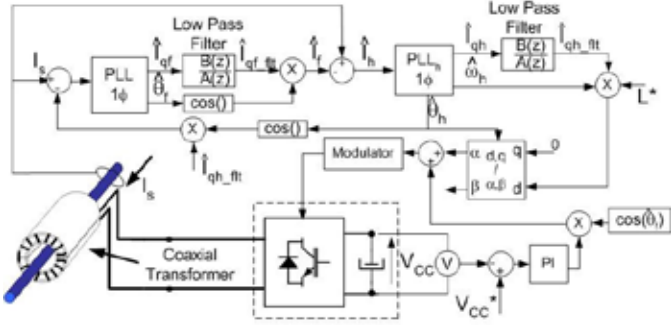
Fig. 4. Block diagram for the implementation of the proposed system.

Fig. 5. Axis references for axis transformations.

In order to apply the proposed system for the compensation of additional harmonic components it is necessary to introduce additional PLL algorithms and inverse Park transforms for each additional harmonic. In practice, the compensation of the 5th, 7th and 11th harmonic is sufficient to obtain satisfactory results on most industrial systems.

In this work the harmonic impedance synthesized is a pure inductive reactance, represented by the inductance L^*, according to the equation:

$$V_h = L^* \frac{dI_h}{dt} \tag{1}$$

Although not explored yet it is possible to implement any kind of impedance (inductive, capacitive and resistive). Future reports will treat about the use of resistance component in order to obtain active harmonic damping. Equation (1) is implemented considering that the current Is, which flows on the coaxial transformer, corresponds to the α component used in Clark transformation, as described on the single phase PLL discussed on section IV-C. The calculation of the voltage to be synthesized is described on the next section.

B. Active harmonic Impedance Implementation

As the PLL algorithms, (1) is implemented considering the emulation of a balanced three-phase system. The calculation of the voltage to be synthesized from equation (1) is carried out in the synchronous reference frame based on the following development, observing the reference axis of Figure 5.

Park's transformation applied to the components α and β is given by:

$$I_q = I_\alpha \cos \theta_h + I_\beta sen \theta_h \tag{2}$$

$$I_d = I_\alpha sen \theta_h - I_\beta \cos \theta_h \tag{3}$$

where:

$$\theta_h = \omega_h t + \phi_h \tag{4}$$

Differentiation of the equations (2) and (3) with respect to time results in:

$$\frac{dI_q}{dt} = \left(\frac{dI_\alpha}{dt} \cos \theta_h + \frac{dI_\beta}{dt} sen \theta_h \right) - \omega_h \left(I_\alpha sen \theta_h - I_\beta \cos \theta_h \right) \tag{5}$$
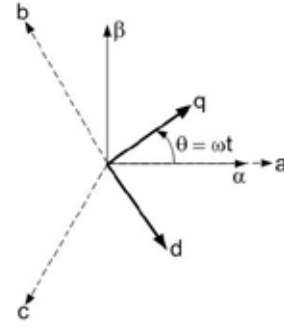
$$\frac{dI_d}{dt} = \left(\frac{dI_\alpha}{dt} sen \theta_h - \frac{dI_\beta}{dt} \cos \theta_h \right) + \omega_h \left(I_\alpha \cos \theta_h + I_\beta sen \theta_h \right) \tag{6}$$

Considering a steady state condition:

$$\frac{dI_q}{dt} = \frac{dI_d}{dt} = 0 \tag{7}$$

$$\left(\frac{dI_\alpha}{dt} \cos \theta_h + \frac{dI_\beta}{dt} sen \theta_h \right) = \omega_h I_d \tag{8}$$

$$\left(\frac{dI_\alpha}{dt} sen \theta_h - \frac{dI_\beta}{dt} \cos \theta_h \right) = -\omega_h I_q \tag{9}$$

Based on the development represented by (2) to (9), and recognizing that in (5) and (6), the terms of the first parentheses after the equal sign represent the Park transformation of the derivatives of the components α and β of the desired currents [9], the components of the voltage to be synthesized are calculated on the synchronous reference frame as follows:

$$V_{qh} = \omega_h L^* I_{dh} \tag{10}$$

$$V_{dh} = -\omega_h L^* I_{qh} \tag{11}$$

Applying the inverse Park transform on the results from (10) and (11) and taking the α-axis component, we obtain (12) which represent the open loop voltage to be synthesized by the PWM modulator, seen at the secondary side of the coupling transformer, responsible for injecting the desired active harmonic impedance.

$$V_h = V_\alpha = -\omega L^* I_{qh} sen \theta_h \tag{12}$$

In Section V simulation results from application of equation (12) to the implementation of the proposed active harmonic impedance are presented. Experimental results are shown in section VI.

C. PLL Algorithms

The PLL algorithms are based on the Park transformations for treatment of desired variables on a synchronous reference frame. The PLL tracking system is based on a PI that

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objectives to cancel the d axis component resulting from the transformation [10], as shown in Figure 6.

The proposed system requires at least two separate PLL algorithms: one for obtaining the amplitude, frequency and phase of the fundamental current component and one PLL in order to obtain the parameters for each harmonic component of interest. It can be found on the literature several alternatives for implementation of the PLL algorithms, but the method of coordinate transformations for the use of synchronous reference has been widely applied. Detailed analysis of PLL algorithms is given in [10], [11], [12], [13] and [14].

The structure used in this work is described in [11] and shown in Figure 6. Basically the PLL emulates a balanced three-phase system using as input the axis α and β components (Clark transformation) of the stationary reference frame. These components are used as input for the transformation used to obtain the quantities on the synchronous reference. The β component is obtained from the q-axis component, obtained from the Park transform output applied to a first order block which the time constant is τ. In order to avoid the PLL tracking on a non-desired harmonic component it is possible to introduce a limiting function on ω or ω_{fbk} in Figure 6.
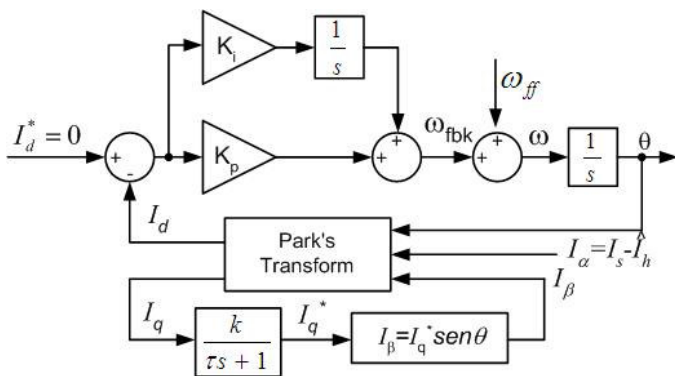

Fig. 6. Block diagram of the single phase PLL algorithm.

The output of the algorithm is the amplitude of the vector representative of the current – the q-axis component, together with its frequency and phase. The tracking is ensured by the PI controller that aims to maintain the calculated d-axis component, obtained by the Park transform, equal zero.

The PLL tuning is based on obtaining the small signal model of the system and to perform the poles allocation in order to obtain appropriate bandwidth and dynamic stiffness with respect to disturbances on the input variable Iα [10]. In order to obtain a better response with respect to estimated amplitude and phase of the fundamental component, the input variable of the PLL algorithm in this project consists of the measured current I_S subtracted from the estimative of the harmonic current, as shown in Figure 4.

The parameter values used in this work are: first order filter time constant τ = 0.001 s and gain k = 1, Kp = 314 rad/A/s, Ki = 3.14 rad/A/s²; ω_{ff} = 377 rad/s, and the poles of the system are: 0.001 and 314 rad/s. The implementation of the system needs the use of low-pass filters for filtering the amplitudes obtained from the PLL algorithms. The filters used in the project are the fourth-order Butterworth type and

were designed using the tool Filter Design & Analysis of MATLAB with the following input parameters: Fpass = 50Hz; Fstop = 360Hz, Apass = 1; Astop = 60dB, fs = 10kHz. The result of applying the low-pass filter for estimation of the magnitude of the fundamental current component is shown in Figure 10.

The structure used for tracking the harmonic component of interest is almost identical to that used for the fundamental component, shown in Figure 5. The input for the harmonic tracking PLL is $I_s - \hat{I}_f$. For synchronization with the harmonic component of interest the following changes in the parameters of the PLL algorithm were introduced: τ = 0.0002 s; ω_{ff} = 1885 rad / s, other parameters have not changed.

The PLL input variable for harmonic frequency component is I_h, which is obtained by subtracting the measured current Is from the instantaneous value of the estimated fundamental current component synchronized by the PLL, as shown in Figure 4. This strategy was adopted in order to reduce fluctuations resulting from the presence of the fundamental component in the calculation of the amplitude of the harmonic component. This strategy allows the filters, to be used in digital output variables of the PLL algorithms, have increased bandwidth and lower order. The results of the estimation of amplitude provided by the PLL algorithms will be used, after digital filtering, for the impedance synthesis associated with the harmonic voltage reference and the active control of the converter DC bus voltage.

D. DC Bus Voltage Control

The control of the DC bus voltage is an item of great importance for appropriate operation of any active filtering scheme based on VSI converter. The performance of the control system of the DC bus voltage must ensure that there is no interaction of this loop with the control of output voltage associated with the harmonic component of interest [15] [16].
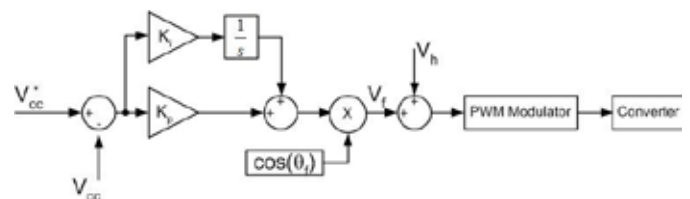

Fig. 7. Converter DC bus control diagram

The control system of the DC bus of the single-phase inverter used in this project is presented in Figure 7. The energy required to maintain DC bus charged is obtained by generating a voltage in phase (or in phase opposition) with the fundamental current flowing in the coaxial transformer secondary. Similar to the strategies presented in [15], [16], [17] and [18] it is used a proportional-integral controller for DC voltage regulation, with the difference that on this work it is generated a voltage in phase with the fundamental current obtained from PLL algorithm and, at the cited references, it is generated a current reference in phase with the voltage obtained from PLL.

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The design of the active harmonic impedance coupling transformer for high currents should consider the use of air gap in order to provide additional flexibility for solution installation, as shown in Figure 9 The use of air gaps allows the use of a transformer that can be assembled directly at the field, avoiding the disconnection of power cables (transformer secondary) allowing a faster solution installation and evaluation. In this condition, care should be taken relative to the transformer magnetizing current magnitude and its effect on the converter current rating. Also, for a cost-effective design, it is important to maintain the inner radio of the toroidal transformer as close as possible from the power cable radio in order to obtain a smaller leakage inductance.

V. SIMULATION RESULTS

A. PLL Algorithms

Figures 10 and 11 show the simulation results obtained from the application of the PLL algorithms to a test signal composed by a fundamental component plus a fifth and seventh harmonic components, with amplitudes of 1 pu, 1 pu and 0.1 pu respectively.

Fig. 10. Amplitude (Iq) and phase angle (θ_f) response obtained from PLL - fundamental component estimation applied to a signal composed by: 1 p.u. (fundamental component) + 1 p.u. (5th harmonic) + 0.1 p.u. (7th harmonic).

If the system stays turned off during long periods, it is interesting to use a small rated pre-charge system, based on a small rated transformer, rectifier and resistor. This allows the charging of the DC bus in order to have the compensation system ready for use. Similar pre-charge strategy is used in basically all commercial frequency converters on the market.

E. Coupling Coaxial Transformer Considerations

The design of the coaxial transformer, shown in Figure 8, should take into consideration the maximum voltage to be injected on the desired frequency and also to ensure the use of the magnetic core at a flux density level below the saturation level of the magnetic material used on its construction, as stated by eq. (13). Maximum flux density choosing is critical, as it is directly related to the iron losses on the transformer core. Another important factor is the primary coil number of turns, which should be defined taking into account the voltage and current of semiconductors with a good cost-benefit relationship available on the market.
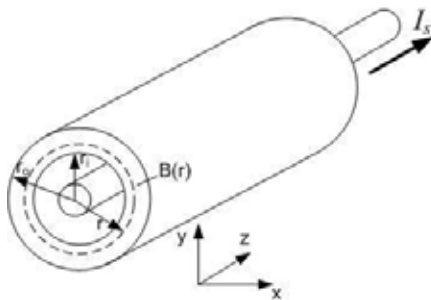

Fig. 8. Coaxial transformer used for active impedance coupling.

$$B(t) = B_1(t) + \sum_h B_h(t) < B_{sat\,max} \qquad (13)$$

The effective harmonic voltage induced in the secondary of the transformer is given by (14). Considering the harmonic induced voltage as a design input, (14) can be used for calculation of the minimum sectional area of the magnetic core necessary to induce the desired harmonic voltage. The magnetic core should be chosen satisfying simultaneously the equations (13) and (14).

$$V_{h2\_rms} = \frac{B_h \omega h A_e}{\sqrt{2}} \qquad (14)$$

Initially we will design the system for injection of a maximum voltage of $6V_{rms}$ at fifth harmonic. Considering that the maximum fifth harmonic flux density is 1T, (14) results in a core section of at least 0.0045 m². Initially, we will consider the use of toroidal magnetic cores, constructed using iron sheets, with the following dimensions: r_o = 5 cm, r_i = 3 cm and width b = 4 cm. Each toroidal core has a sectional area equal to 8x10-4m², which implies the use of six for cores to be able to induce the desired harmonic voltage. It was used 20 turns at the transformer converter side, so the primary synthesized voltage was about 120Vrms.
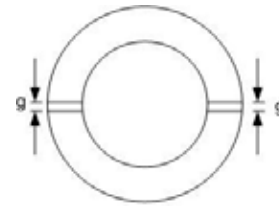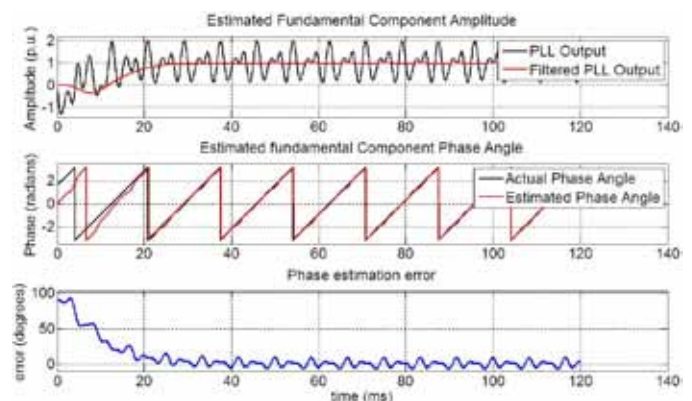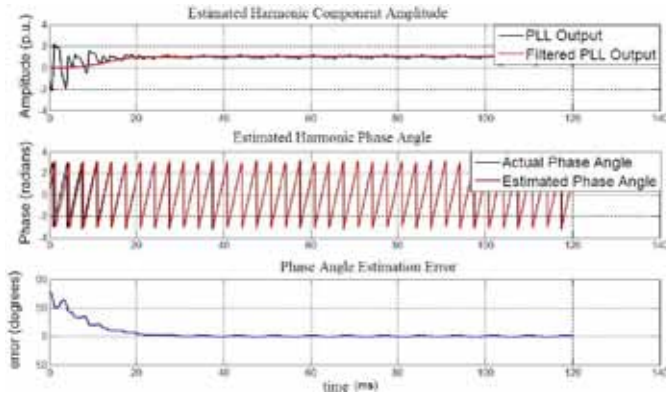
Fig. 11. Amplitude (Iq_{5h}) and phase angle (θ_{5h}) response of the PLL used to estimate the fifth harmonic component.

The PLL simulation results shows the effectiveness of the implemented algorithms, as the fundamental and the fifth harmonic components were correctly tracked even in the presence of an additional harmonic component. The time needed for complete tracking was about 25 ms.

B. Active Harmonic Impedance Application Analysis

The performance of the proposed harmonic impedance will be evaluated on a situation of significant importance in the industrial environment: the detuning of automatic thyristor switched capacitor banks for power factor correction. Thyristor switched banks are used for fast power factor compensation and harmonic filter commutation in systems with fast dynamic changing loads [19] [20]. It is possible to use the proposed system also to implement hybrid shunt active filters (Figure 1), as discussed in [9], [21] and [22], adjusting the control reference in order to obtain a controlled frequency response.

The simulation study of the proposed active harmonic impedance was realized implementing a single-phase system shown in Figure 12. The system consists basically of a source with impedance $R_s + jX_s$, a load with a lagging power factor, a capacitor bank for power factor correction, composed by a fixed stage and three thyristor switched stages, and a harmonic source injecting a 5th harmonic component. The system data are: rated power = 150KVA, X_s = 7%, X/R = 15, load: 100kW, PF = 0.7 inductive, and 5th harmonic I_h = 0.1 pu (100 Amps peak). The total capacitance was calculated for unit power factor and the four stages have equal capacitance.

Figure 13 shows the system response without compensation. In this Figure 1.0 p.u. means the rated capacitor bank current (463 amps rms). We can see in Figure 13 the capacitors stages commutations and that a resonance condition occurs leading to a capacitor harmonic current approximately equal to 3 times the original fifth harmonic current injected.

Figure 14 shows the result when the active impedance compensation is activated at time t = 25ms. Also the maximum harmonic induced voltage at the capacitor side was limited to 10V and the converter switching frequency was 10kHz. The synthesized inductance was selected in order to be obtained a constant harmonic resonance frequency equal 134 Hz for the four capacitor configurations.
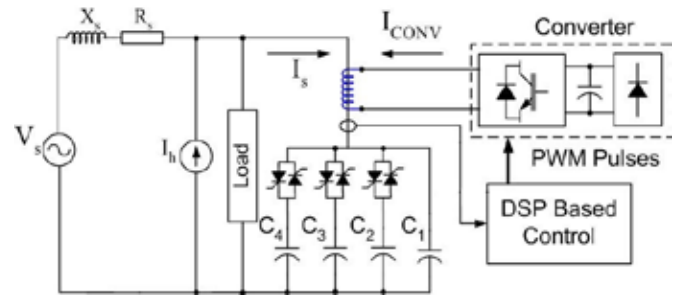

Fig. 12. Basic system for evaluation of active harmonic impedance application.
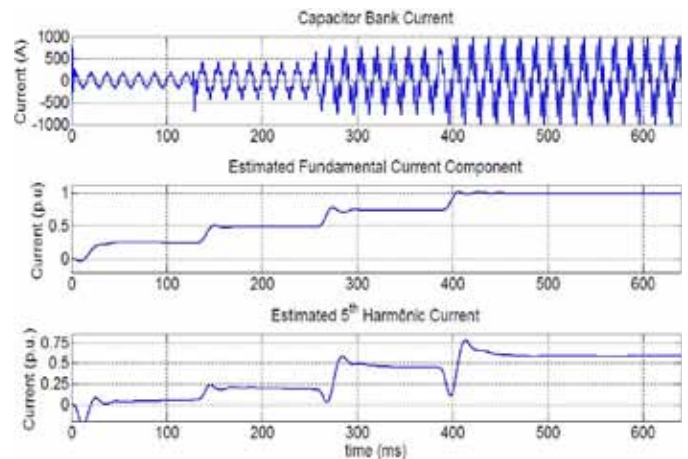

Fig. 13. Current at the capacitor bank without compensation with sequential capacitor switching.

As, on typical industrial power factor controllers, the reactive power of each stage is a data input and, the controller or the switching element (thyristor or contactor), normally has digital outputs used to inform the activation of the each stage, this information is used in order to calculate the necessary reference inductance for the proposed compensation system. This activated stages information can also be used in order to choose PLL gains allowing the best tracking performance even at low currents, when, for instance, only one stage is activated.

As the capacitors fundamental current values are equal for the two situations, with and without compensation, it can be concluded that the fundamental capacitor voltage was unchanged with the compensation active because the fundamental current has no change compared with the result obtained with no compensation. So neglecting converter and transformer losses, the fundamental component synthesized by the converter is virtually zero. Figure 15 shows the source and inverter currents. It can be clearly noted from Figure 15 that the resonance condition was mitigated and that a small 25Arms, 120V, rated converter is suitable for system implementation.

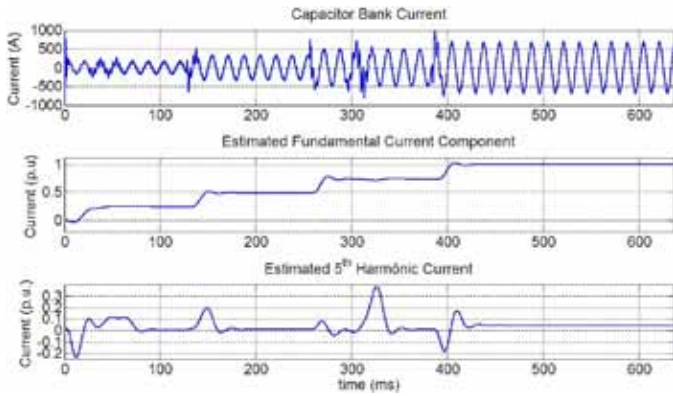Eletrôn. Potên., Campo Grande, v. 17, n. 3, p. 641-650, jun./ago. 2012

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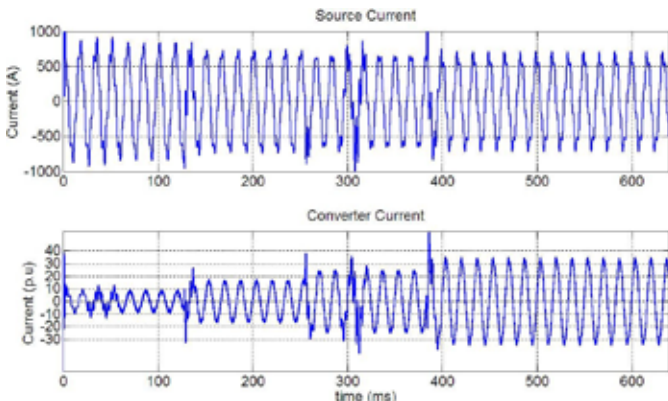Fig. 14. Current at the capacitor bank with compensation activated.

Fig.15. Source and converter currents with compensation active.

The synthesized harmonic inductance L* must be defined accordingly with the control objective, which can be a tuned or a detuned filter, for instance. As the compensation voltage is directly obtained from multiplication of L* and I_{qh}, any deviation will have a direct impact on results in the same way as in passive filters. This is especially critical in tuned filters, where a precise resonance frequency must be obtained in order to have de desired filtering performance. As L* is implemented in a controlled manner, it is simple to adjust the value in the field in order to obtain the desired performance. As an example of deviation on required L*, Figure 16 shows a simulation of the previous system, shown in Figure 10, considering a -20% deviation on L*.
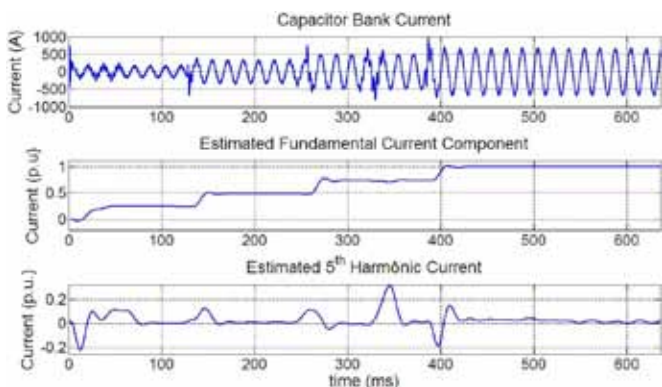

Fig. 16. Simulation results with a -20% of deviation on L*

The system shown in Figure 11 was also simulated changing the fifth harmonic source from a current source to a

voltage source in series with main fundamental voltage. It was introduced a voltage distortion of 10% and the simulation was performed considering all capacitor stages activated. The result of this simulation case is shown in Figure 17, where it is shown the capacitor current and its respective frequency spectrum before and after harmonic mitigation activation. It can be noted from Figure 17 that the proposed system is also able to mitigate voltage distortion.
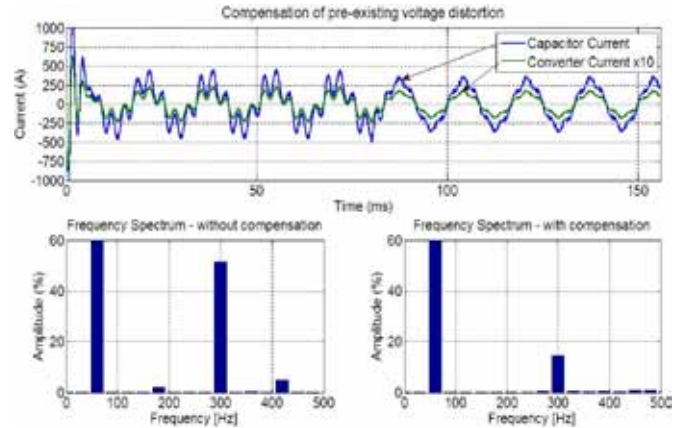

Fig. 17. Simulation of voltage harmonic compensation.

VI. EXPERIMENTAL RESULTS

The basic system shown in Figure 18 was implemented in order to obtain experimental results from the application of the proposed harmonic impedance. The system is composed by a power factor capacitor bank (104μF) that is supplied from the output of an adjustable autotransformer. The control system was implemented using the hardware UPC2812 which is based on the digital signal processor TMS320F2812. The converter switching frequency and sample time was 10kHz, the integration method used was the basic trapezoidal method. The converter was a commercial product, 220VAC, 4A rated, that was adapted to receive PWM commands from UPCC2812.
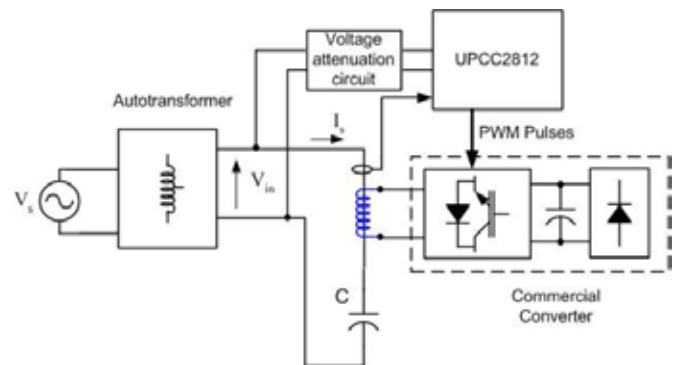

Fig. 18. Experimental setup for active harmonic evaluation

The harmonic source was the pre-existing harmonic voltage distortion from the supply source as can be seen in Figure 18. This experiment can be considered as a small scale evaluation of the results of Figure 17. Figure 19 shows the experimental results for the converter and capacitor currents without and with active impedance compensation.

As it is shown in Figure 19 the fifth harmonic current distortion was reduced from 20% to 3% and illustrates the capability of the proposed system for harmonic mitigation. Although on this paper it was demonstrated a harmonic blocking operation, it is also possible to implement a shunt compensation using the active impedance to tune a shunt filter. Figure 20 shows a picture of the coupling transformer used for the implementation of the proposed system.
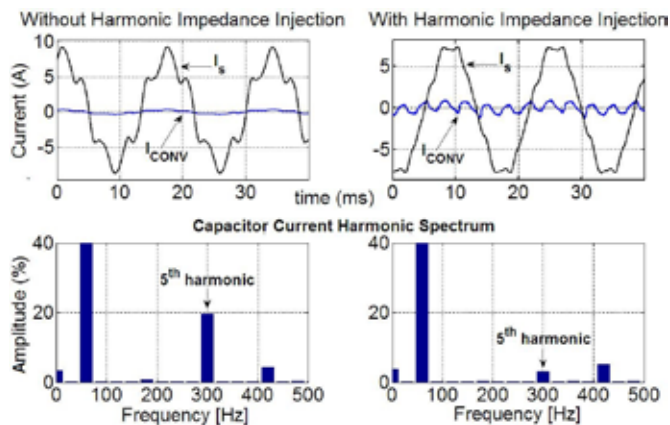

Fig. 19. Capacitor current (I_s), converter current (I_{CONV}) and capacitor current harmonic spectrum: without and with active harmonic impedance injection.

VII. CONCLUSION

This paper described a flexible harmonic compensation system that can be used to implement shunt or series harmonic mitigation devices. The application of the system for capacitor detuning was successfully demonstrated by simulation and experimental analysis. The use of a coaxial coupling transformer gives flexibility to the system allowing a fast field solution evaluation that is especially useful for detecting the better configuration in existing power systems. The use of a small current rated converter for harmonic impedance synthesis and a single transformer for detuning of multiple capacitor stages implies in a cost effective solution.

Fig. 20. Coaxial coupling transformer used for experimental evaluation.

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