A REVIEW OF HYBRID POWER AMPLIFIER TECHNOLOGIES

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***Abstract* – With the aim of synthesizing high-fidelity voltage waveforms without penalizing the system efficiency, several works have proposed hybrid power amplifiers (HPAs), composed of linear and switching amplifiers, combining the benefits of each approach. According to the connection of the linear and the switched amplifiers, the HPAs are classified as envelope, parallel and series configurations. Each configuration holds particular characteristics that can be advantageous in some applications meanwhile to be quite stringent in others. This way, through a review of literature, this work aims to identify the features of each configuration, highlighting its benefits and possible limitations. The topologies proposed hitherto are analyzed from the circuit and control perspective. Therefore, this paper can be useful for one who is starting researching on this field or aims to select a suitable hybrid arrangement for a given application. Finally, an experimental case study is analyzed and future trends in research on HPAs are addressed.**

***Keywords* – AC Power Source, Linear Amplifier, Hybrid Amplifier, Multilevel Inverter, Switching Amplifier.**

I. INTRODUCTION

For decades the power amplification was governed by linear electronics [1]. Nevertheless, with the continuous improvement of power electronic devices, the power switching converters have achieved better performance in terms of dynamic response, efficiency, power density, and reliability [2]–[4]. Unfortunately, switching-mode power amplifiers (SMPAs) present adverse effects such as inherent nonlinearity, time-delays, need for low-pass filters to attenuate switching harmonics (that limit the control bandwidth), nonlinearities of passive components, cross- and inter-modulation (in audio amplifiers) and electromagnetic emissions [5]–[6]. On the other hand, the appeal of high-efficiency, high power density, reduced volume and weight, and low price, achieved, for instance, in single stage conversion amplifiers [6], prompted the researchers to develop alternatives to alleviate the aforementioned limitations.

Regrettably, for high-end audio [7]–[8] or high performance ac power source (ACPS) applications [9], where a wide frequency range and high-fidelity voltage waveform is mandatory, SMPAs presented hitherto still not achieved the performance provided by the linear technology, due to the aforementioned adverse effects.

Therefore, in order to gather both high-fidelity waveforms provided by linear power amplifiers (LPAs) (usually class-A, B or AB amplifiers) and high-efficiency feature of SMPAs, the interest in hybrid power amplifiers (HPAs) has been grown recently [10]. As can be seen in Figure 1, an HPA is an association of an SMPA (operating as the main amplifier and handling most of the total power) and an LPA (operating as the correction amplifier and handling a small amount of the whole power). The main attractive feature of HPAs is that their output waveform quality is defined by the linear stage, presenting high-fidelity with respect to the reference signal, without penalizing the system efficiency.

Although some previous works have presented a sort of topologies of HPAs [11]–[12], there is a lack of literature concerning a concise review of HPAs, identifying the advantages and limitations of most common configurations. Therefore, this work presents a peer review of literature of HPA technologies, concerning the main topologies and control techniques used in industrial applications. With the analyses, it is possible to identify the features of each configuration and its main benefits and drawbacks. This way, this paper can be useful for one who is starting researching on this field or aims to select a suitable hybrid arrangement for a given application.

This paper is organized as follows: Section II presents a classification and main characteristics of HPAs. Sections III, IV and V present the concept, the topologies, the main control techniques and the common applications of the envelope, parallel and series configurations of HPAs, respectively. In section VI is realized a qualitative analysis of each class of HPA topologies. Section VII shows a case study, demonstrating through experimental results the main features of an HPA. Finally, Section VIII summarizes the main characteristics of each approach and discusses the trends in the field.

II. CLASSIFICATION OF POWER AMPLIFIERS

In most applications, the power amplifier is commonly implemented through an LPA or an SMPA alone. The former alternative is preferable when the output voltage waveform fidelity is the main concern, while the latter enables to establish a trade-off between fidelity and efficiency. As

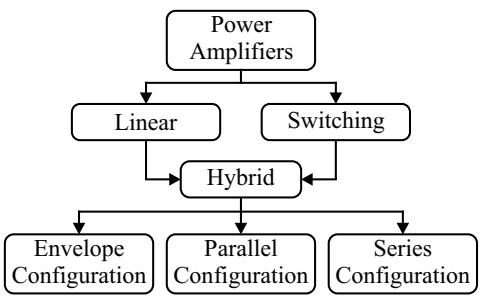

Fig. 1. Classification of power amplifiers.

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aforementioned in Section I, a topology that combines both an LPA and an SMPA in the same circuit is called HPA. Yundt [10] defined two possible arrangements of HPAs: series and parallel configurations, depending on how the LPA and SMPA are connected to each other. More recently, this classification was expanded [11], including the envelope configuration into the set of possible arrangements. This general classification is represented in Figure 1.

Next sections present the most common topologies and control techniques of HPA applications. Although there is a great number of control techniques that can be applied to HPA topologies (for both main and correction amplifiers), only those normally identified in industrial applications are referred in this paper.

Before the analysis of the topologies and control techniques, two important concepts are defined for the HPAs. The first is the "power converter bandwidth," which is related to the maximum reference frequency that can be synthesized by the main amplifier. The latter is the "control system bandwidth," which concerns to the dynamic response of the whole amplifier, being defined by the correction amplifier. The power and control bandwidths are usually different, since the first one is defined by the main amplifier (SMPA) while the latter is defined by the correction amplifier response (LPA).

Throughout the paper, simulations are presented for selected topologies intending to point out details about positive and negative characteristics of the referred HPA configuration. The simulation specifications are oriented to the identification of the circuit and control behavior in specific conditions and do not serve nor intend to comparative means.

III. ENVELOPE CONFIGURATION

Hybrid power amplifiers belonging to the class of the envelope configuration are composed of an output LPA, which is responsible for synthesizing the desired output voltage waveform, and by a tracking power source (TPS) (implemented by means of a high-efficiency switch-mode power supply), which is responsible for regulating the variable dc bus voltage of the LPA. A conceptual diagram can be seen in Figure 2 (a), where $v_+(t)$ and $v_-(t)$ are the voltage waveforms synthesized by the TPS, $v_o(t)$ is the load voltage waveform, and $i_o(t)$ is the load current. With the aim of generalizing the nomenclature throughout the paper, the TPS is called as "main amplifier" and the LPA as "correction amplifier" from hereinafter.

The aim of regulating the dc bus voltage is to provide adequate bias conditions to the correction amplifier with low-losses for the entire LPA output voltage range. In this way, the amplitude of the dc bus voltage should not exceed an optimum limit defined by the LPA designer. Thus, the waveforms are as shown in Figure 2 (b). The voltage across the output linear transistors (bipolar- or MOS-type) of the correction amplifier is significantly reduced, minimizing the conduction losses due to the dc bias. As the main amplifier is a switching converter, which presents low-losses, a high-efficiency and high-fidelity power amplifier can be achieved with the envelope configuration.

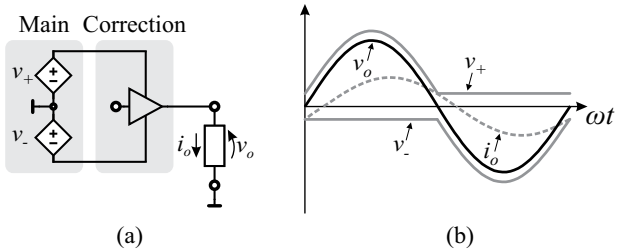

Fig. 2. Envelope configuration [11]. (a) Diagram of the general scheme. (b) Main waveforms.

The envelope configuration has been effectively employed in portable battery-operated systems (e.g., cellular phones, laptops, etc.), where high-efficiency is mandatory to extend the battery life [13] as well as to provide a portable device with low volume and weight. These applications demand a high-fidelity main amplifier with high-bandwidth, which can be achieved only by employing very high switching frequencies (e.g., megahertz) and/or passive high-order low-pass filters [14]. This way, most applications are restricted to low-power (few watts), although it is also possible to employ the envelope configuration to applications where dozens of watts are handled.

A. Common Envelope Topologies

Several topologies have been proposed to implement the main amplifier of the envelope configuration, as presented in Figure 3. They are characterized to present a very low output voltage (e.g., in grid supplied applications) or a very low input voltage (e.g., in battery supplied applications). The simplest way to implement the main amplifier is employing a dc-dc step-down converter [15], as can be seen in Figure 3 (a). Although most applications are in low-power, a three-level dc-dc step-up converter was employed in [16] to implement a middle point, as shown in Figure 3 (b), enabling a high-power ACPS to synthesize ac voltage waveforms. With the aim of extending the operation range of the main amplifier to low input voltages (supplied by batteries in portable devices), a cascaded step-up and step-down converter was proposed in [17], as shown in Figure 3 (c).

Since the relative cost of inductive filtering increases as the power goes down, alternative solutions have been studied to minimize the output voltage ripple produced by the main amplifier, without significantly increasing the switching frequency and/or the filter requirements. With this purpose, there is the interleaved dc-dc step-down converter [18] and the three-level (flying capacitor) dc-dc step-down converter [19], depicted in Figure 3 (d) and (e), respectively.

The main amplifiers presented in Figure 3 vary their output voltage continuously, which generally demands a fast dynamic response. It is important to note that class-H audio amplifiers make use of a similar approach, although there is no an explicit main amplifier to regulate the dc bus voltage level [5], [20]. As an alternative, there is the possibility of varying the output voltage of the main amplifier in discrete steps [21], [22], whose concept is similar to that employed by class-G audio amplifiers [5]. Figure 4 (a) presents a topology where the output voltage of the main amplifier can be selected among different levels [21], [22]. Yang, Haddad and East [22] have demonstrated that the efficiency gain achieved by this

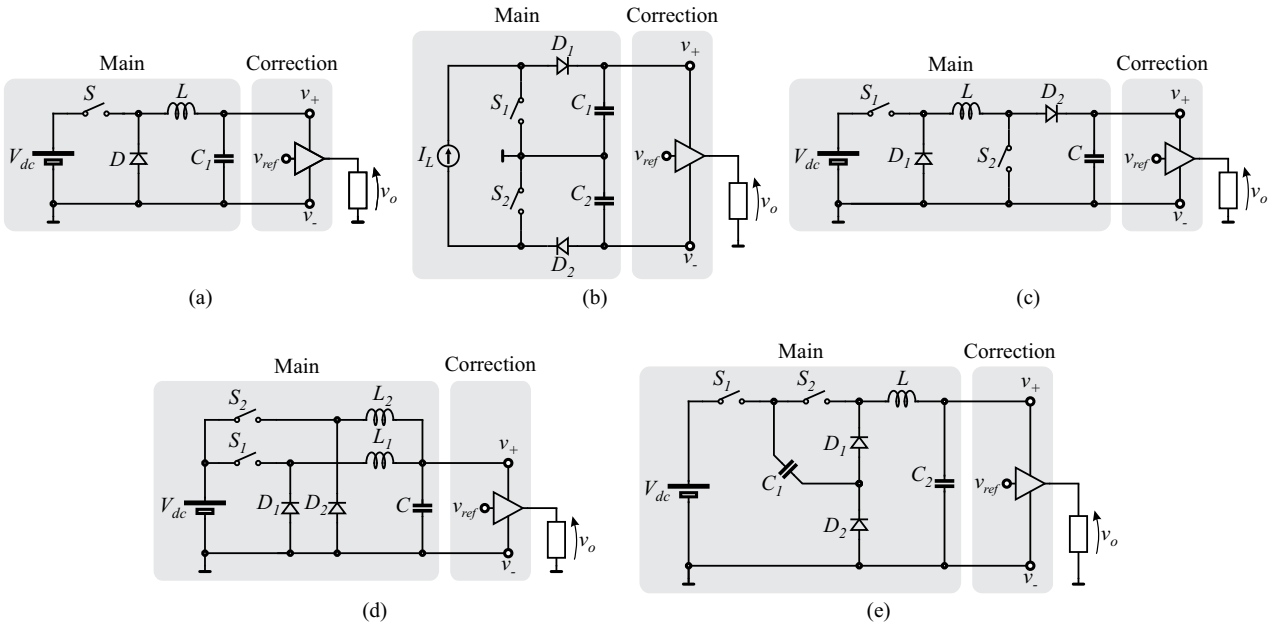

Fig. 3. Envelope configuration topologies. (a) Dc-dc step-down converter [15]. (b) Three-level dc-dc step-up converter [16]. (c) Cascaded dc-dc step-up and step-down converters [17]. (d) Interleaved dc-dc step-down converters [18]. (e) Three-level dc-dc step-down converter [19].

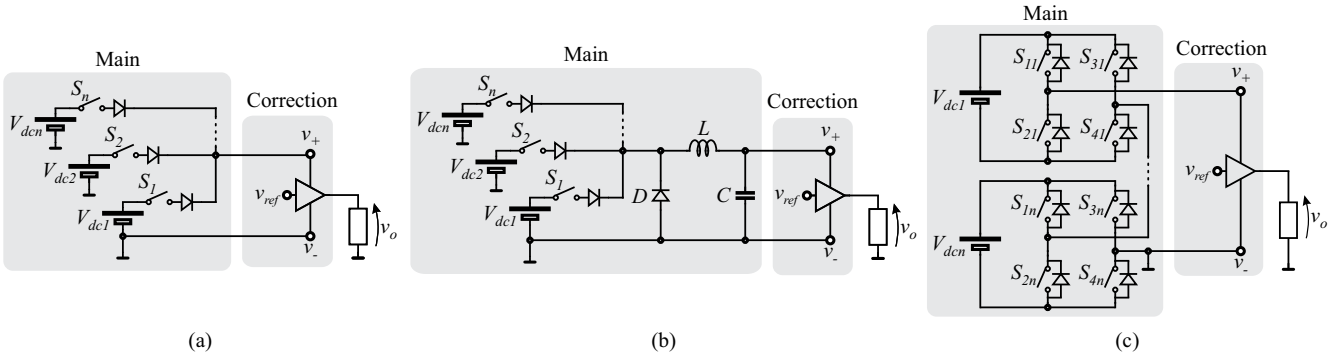

Fig. 4. Envelope configuration topologies with discrete voltage sources. (a) Multilevel converter with independent voltage sources [21]–[22]. (b) Multilevel converter with independent voltage sources and output low-pass filter [23]. (c) Multilevel converter with cascaded full-bridge cells [24].

topology is lower than that obtained by varying continuously the voltage waveform supplied to the correction amplifier and goes toward this when the number of levels is increased. It corroborates with the idea that a continuous varying dc voltage ensures an optimized value for the dc transistor bias.

Similarly, a topology with discrete input voltage levels but with an additional output low-pass filter is proposed in [23], as shown in Figure 4 (b). As a matter of fact, this topology does not present discrete steps at the main amplifier output voltage waveform, since an output low-pass filter is used, but it is presented here due to its similarity with the topology of Figure 4 (a). A multilevel inverter with cascaded full-bridge cells can be used as main amplifier [24], as presented in Figure 4 (c). In this case, it is suggested to select the values of V_{dc1} to V_{dcn} in order to maximize the system efficiency for a given output voltage profile (well-known in RF applications).

B. Common Control Techniques for Envelope Topologies

This section discusses the main techniques presented in the literature to control only the main amplifier. Basically, two approaches are adopted:

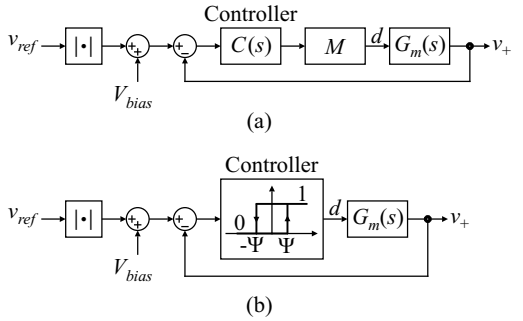

Fig. 5. Common controllers employed for the main amplifier. (a) Phase lead and/or phase lag compensation [25]. (b) Hysteretic controllers [14], [16], [25].

(i) Phase lead and/or phase lag compensation, which makes use of proportional-integral (PI) and proportional-integral-derivative (PID) controllers [25]. This approach (for controlling, for example, $v_+(t)$) is represented in Figure 5 (a), where V_{bias} is the quiescent voltage, $C(s)$ is the controller, M is the modulator, and $G_m(s)$ is the plant model;

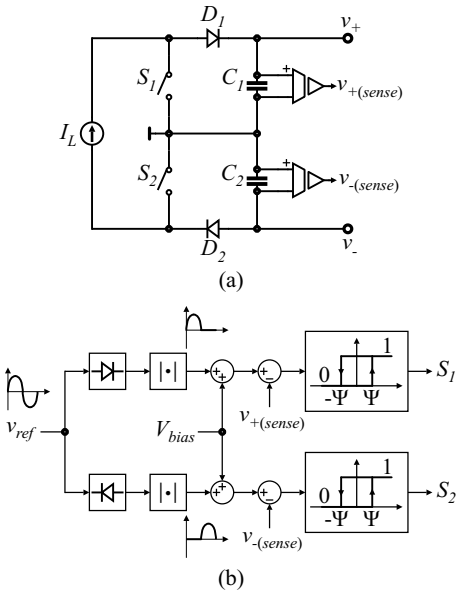

Fig. 6. Simulation of a three-level dc-dc step-up converter [16]. (a) Topology. (b) Control approach.

(ii) Hysteretic controllers [14], [16], [25]. This approach is represented in Figure 5 (b), where –Ψ and +Ψ define, respectively, the lower and upper limits of the hysteretic controller.

Due to its simplicity, the hysteretic controller is the most used controller in the main amplifiers of the envelope configuration. Comparative results carried out in [25], between the performance of a main amplifier employing a PID and a hysteretic controller, has demonstrated that the latter provides a better dynamic response than the former, since it guarantees a control bandwidth equivalent to the converter switching frequency. On the other hand, the hysteretic controller usually implies in a variable switching frequency, making difficult to design a filter to attenuate the harmonics from modulation. A hysteretic controller with fixed switching frequency (for a range of output voltages) is proposed in [14], which is achieved by varying the limits of the hysteretic window, but it affects the voltage ripple.

C. Example and Simulation Analysis

This analysis intends to illustrate some aforementioned features of the envelope configuration by means of a numerical simulation that is carried out using the PSIM® software. For sake of simplicity, the nonlinearities of the semiconductors and other devices have been neglected. In this section the three-level dc-dc step-up converter of Figure 3 (b) used in an ACPS application described in [16] is employed as example.

In this example, the control of I_L is not taken into account (I_L is considered constant). The design considerations are well discussed and presented in [16]. The main specifications are: I_L = 10 A (input current); $C_{1,2}$ = 470 nF (output filter capacitors); and $v_{ref,rms}$ = 115 V @ 400 Hz (reference voltage).

The simulated power and control circuits are presented in Figure 6 (a) and (b), respectively. Two independent control loops, based on hysteretic controllers, are used for controlling $v_+(t)$ and $v_-(t)$. The limits of hysteretic controller are defined as

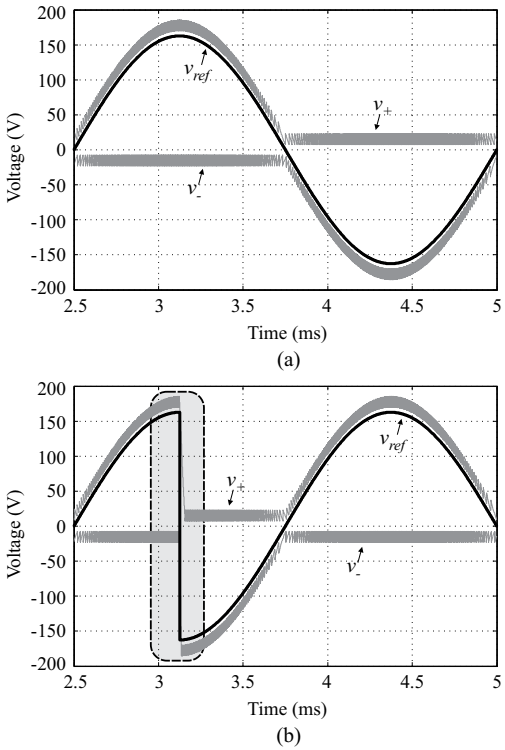

Fig. 7. Simulation results of a three-level dc-dc step-up converter. (a) Steady-state operation. (b) Phase inversion in reference voltage.

2Ψ = 15 V, and the quiescent voltage (mandatory for biasing the output linear transistors of the correction amplifier) is defined as V_{bias} = 30 V.

The simulation results are shown in Figure 7. The voltage waveforms for steady-state operation are shown in Figure 7 (a). As one can see, the voltage waveforms $v_+(t)$ and $v_-(t)$ present a variable frequency ripple (characteristic of hysteretic controllers) and are offset of $\pm V_{bias}$ in relation to $v_{ref}(t)$, as expected. Furthermore, the simulation results for an abrupt changing (phase inversion) in reference voltage $v_{ref}(t)$ are shown in Figure 7 (b) (see the shaded area). The dynamic response of the controllers in this case was not enough to guarantee that $\pm V_{bias}$ is presented, making impossible the operation of the correction amplifier. One possible solution is to select a higher value for V_{bias} paying the price of offsetting the converter efficiency [14].

It must be emphasized that the output linear transistors of the correction amplifier must sustain entirely the load voltage. Therefore, the LPA is designed to support a peak of 162 V and conducts entirely the load current, which can make the selection of the output linear transistors difficult.

IV. PARALLEL CONFIGURATION

In the parallel configuration, the outputs of both main and correction amplifiers are connected in parallel, as presented in the diagram of Figure 8 (a). While the main amplifier supplies the bulk of the load current, the correction amplifier is responsible for setting the required load voltage. Thus, only a small current is circulating through the correction amplifier, enabling to minimize the losses through its output linear transistors. Additionally, the correction amplifier defines the output impedance of the HPA [10].

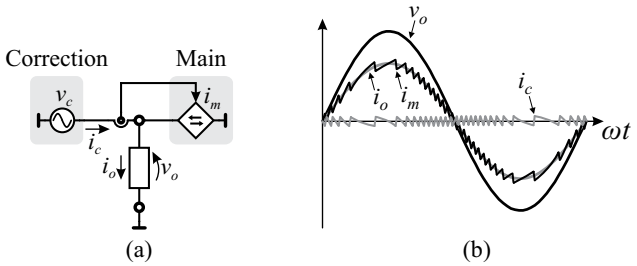

Fig. 8. Parallel configuration [10]. (a) Diagram of the general scheme. (b) Main waveforms.

The operation of the parallel configuration is illustrated in Figure 8 (b), where $v_o(t)$ is the load voltage waveform and $i_o(t)$ is the load current waveform, which is composed of the currents supplied by the main $i_m(t)$ and correction $i_c(t)$ amplifiers. The control strategy is designed in such way that the main amplifier supplies most of the load current, while the correction amplifier compensates for the ripple observed in $i_m(t)$ and defines the load voltage. In other words, the main amplifier current $i_m(t)$ is made as close as possible to the load current $i_o(t)$. It is interesting to note that the correction amplifier in the parallel configuration operates analogously to a shunt active power filter, i.e., injecting harmonic content to smooth the load current. Nevertheless, it is important to highlight that the correction amplifier can be designed to supply the entire load current during a severe transient event, when the main amplifier is not able to act sufficiently fast due to its relatively low control bandwidth (in comparison to the linear correction amplifier) [10]. If these events occur occasionally, the additional power dissipated by the correction amplifier may not offset the designed system efficiency. On the other hand, an oversized correction amplifier may contribute to increase the system costs.

A. Common Parallel Topologies

Due to the aforementioned characteristics, the parallel configuration is commonly adopted in high-end audio applications [26]. Some works even propose its use in RF applications [27], low-voltage power supplies (e.g., for microprocessors [28]) and, hardly, ACPS applications [12].

The main topologies of HPAs in the parallel configuration are summarized in Figure 9. The symbol of the bipolar junction transistor (BJT) is generally used in Figure 9 to represent the output linear transistors of the correction amplifier, independently of the semiconductor technology adopted to implement them.

The simplest topology is represented in Figure 9 (a), which

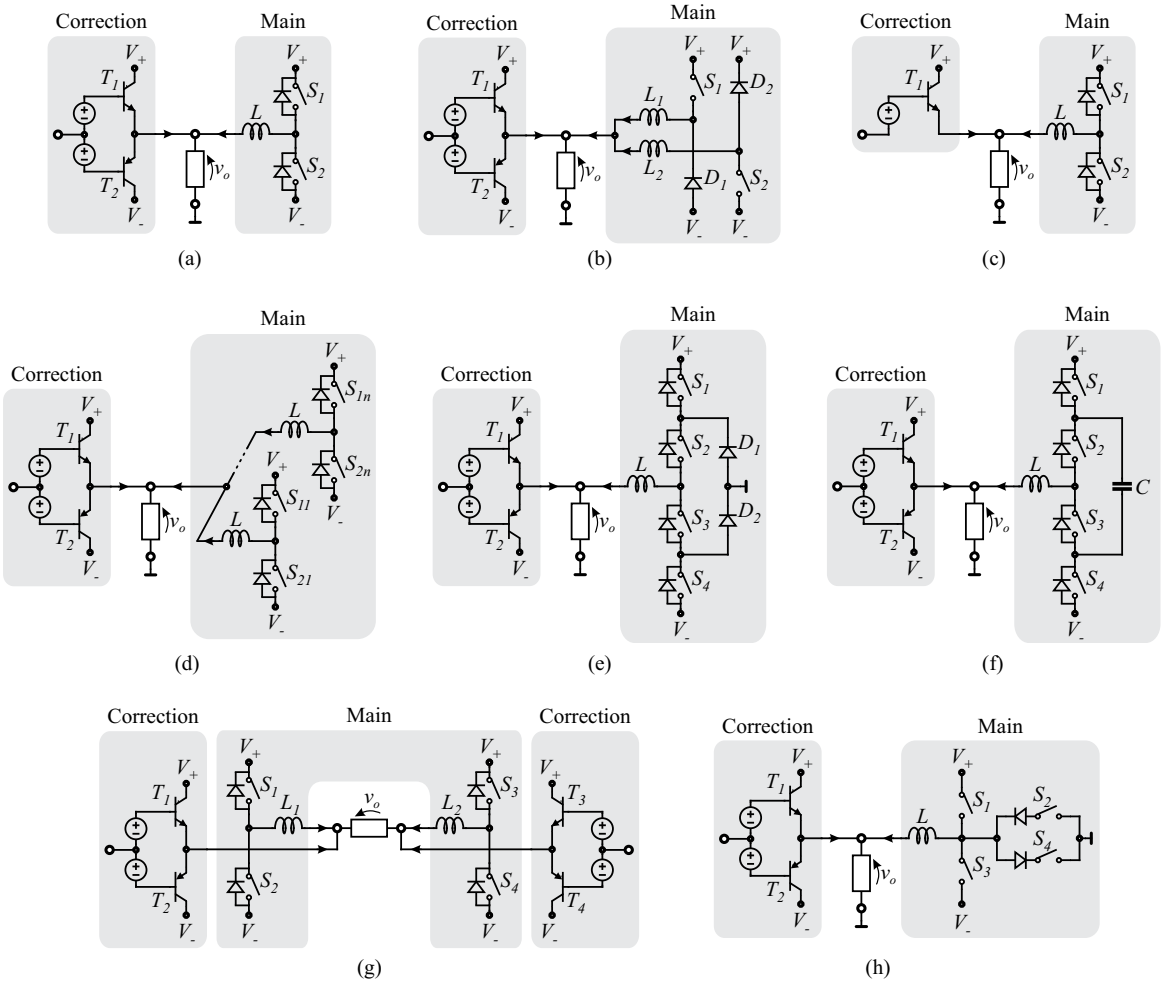

Fig. 9. Topologies employed in the parallel configuration. (a) Half-bridge inverter [12], [26], [29]. (b) Parallel-connected unidirectional dc-dc converters [12], [26]. (c) Half-bridge inverter and unidirectional linear power amplifier [12]. (d) Interleaved half-bridge inverters [12]. (e) Half-bridge inverter with neutral-point-clamped [12]. (f) Half-bridge inverter with flying capacitors. (g) Full-bridge inverter [30]. (h) Modified full-bridge inverter [30].

is composed of a half-bridge inverter that connects the inductor L to the constant dc bus voltage levels V_+ or V_- [12], [26] and [29]. Additionally, the division of the half-bridge inverter into two unidirectional dc-dc step-down converters was proposed in [12] and [26], as shown in Figure 9 (b), eliminating the possibility of shoot-through and, especially, enabling to employ ultrafast diodes, minimizing the reverse-recovery losses that plague the MOS transistors.

As MOSFET-type semiconductor switches are more efficient for low-voltage ratings (up to 500 V) and their current ratings is limited by their breakdown voltage (especially *p*-channel devices), Ertl, Kolar and Zach [12] proposed to control the main amplifier in a way that the correction amplifier can supply only unidirectional currents, enabling to eliminate the *p*-channel transistor, as shown in Figure 9 (c). Unfortunately, this solution results in a non-uniform pulse response of the whole amplifier, i.e., for the rising-edge the response is defined by the correction amplifier (which presents high-bandwidth and high slew rate) and for the falling-edge it is defined by the main amplifier (which presents slower dynamic response and lower slew rate) [12].

In order to increase the current capability of the whole system and also to reduce the ripple of the current supplied by the main amplifier, an interleaved half-bridge inverter with phase-shift (PS) pulse-width modulation (PWM) [12] can be employed, as depicted in Figure 9 (d). Another solution for ripple reduction is possible by using multilevel structures, such as the neutral-point-clamped (NPC) inverter [12], Figure 9 (e), and the flying capacitor inverter, Figure 9 (f). The advantages of the multilevel inverters of Figure 9 (e) and (f) over the interleaved inverter of Figure 9 (d) are the possibilities of using low-voltage rating semiconductor switches, which is an interesting feature in high-voltage applications (e.g., in ACPS, where the mains voltage waveforms must be emulated).

With the purpose of eliminating the dc bus middle-point required by half-bridge inverters and its unbalance issues, a full-bridge inverter can be employed as main amplifier [30], as depicted in Figure 9 (g). On the other hand, the topology of Figure 9 (g) demands the use of two correction amplifiers. This way, in [30] it is also proposed a modified full-bridge structure, resulting on the topology presented in Figure 9 (h), where the pair of switches $\{S_1, S_2\}$ is used to supply positive currents to load, while the pair $\{S_3, S_4\}$ is used to supply only negative currents.

B. Common Control Techniques for Parallel Topologies

In the parallel configuration, both main and correction amplifiers are controlled in closed loop. The former is controlled to supply the load current and the latter to supply the load voltage. This section is focused on the control techniques commonly applied to the main amplifier stage. Due to their implementation simplicity, robustness and fast dynamic response, the use of hysteretic controllers in the current control loop of the main amplifier appears to be an agreement in literature [26], as can be seen in Figure 10 (a). The basic goal is to make the main amplifier supplies almost the load current $i_o(t)$. In order to achieve this, the reference current of the main amplifier $i_{m,ref}(t)$ is defined by a factor K ($K > 1$) multiplying the correction amplifier current $i_c(t)$. Since $i_o(t)$ is only defined by the load and $i_o(t) = i_c(t) + i_m(t)$,

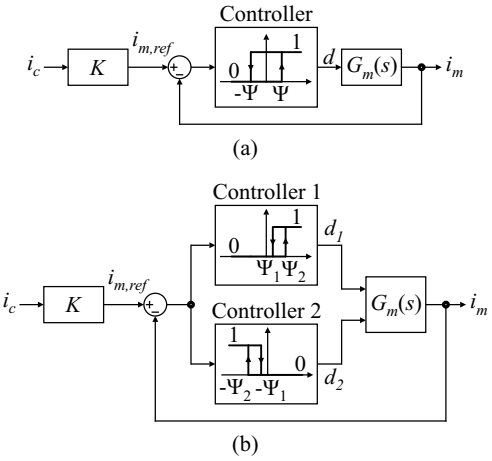

Fig. 10. Common controllers employed for the parallel configuration [26]. (a) Hysteretic controller. (b) Hysteretic controller with dead-band.

then $i_c(t) = i_o(t)/(1+K)$. Therefore, the factor K defines the current sharing between the main and correction amplifiers.

Individual hysteretic controllers with a dead-band near zero current (between $-\Psi_1$ and Ψ_1) to each dc-dc step-down converter of topology of Figure 9 (b) is proposed in [26] and represented in Figure 10 (b), so that neither converter contributes to the load current. This way, only the correction amplifier contributes to the load current at low-power or low-current levels, reducing the distortions caused by the limit cycle ($i_m(t)$ oscillates around zero for $i_o(t)$ equal to zero), although this approach reduces the whole amplifier efficiency.

Regrettably, a balanced current sharing among cells in interleaved converters (e.g., interleaved half-bridge inverter of Figure 9 (d)) is impaired by the use of hysteretic controllers, offsetting the expected reduction of current ripple since the phase-shift pulse-width modulation is no longer presented [12].

An interesting feature of both parallel and series configurations is related to the global system stability, which is determined by the correction amplifier (see Appendix). Generalizing, this feature implies that, even if the main amplifier were unstable, the system could be theoretically stable, since the correction amplifier presents sufficient energy (i.e., current capability in parallel configuration and dc bus voltage in series configuration) to compensate for the oscillations caused by the former [28]. Of course, in actual circuits, both main and correction amplifiers are designed to be stable, although ideally it is not necessary [28].

C. Example and Simulation Analysis

With the aim of illustrating some aforementioned characteristics of the parallel configuration, a simulation analysis is carried out in this section for the half-bridge inverter of Figure 9 (a) used in a high-end audio application [26]. The design considerations are presented in [26] and the main specifications are: $V_+ = 40$ V and $V_- = -40$ V (dc bus voltage); $L = 220$ µF (filter inductor); $v_{ref,rms} = 15$ V @ 1 kHz. (reference voltage); and $Z_o = 4\ \Omega$ (resistive load).

The simulation circuit is presented in Figure 11 (a) and two different control circuits are simulated, as presented in Figure 11 (b) and (c). For the control circuit of Figure 11 (b), which employs one hysteretic controller, the gain factor K is defined as 50 (that means the main amplifier supplies a current 50 times

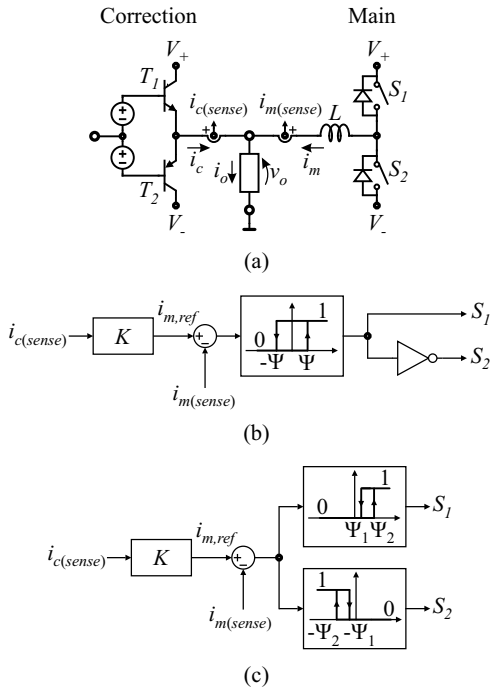

Fig. 11. Simulation of an HPA using a half-bridge inverter as main amplifier. (a) Topology [12]. (b) Control approach employing one hysteretic controller [26]. (c) Control approach employing two hysteretic controllers and a dead-band [26].

higher than the correction amplifier). The window of the hysteretic controller, defined as 2Ψ, is selected in order to guarantee that the maximum current ripple of $i_m(t)$ (and of $i_c(t)$, as consequence) is about 350 mA. Similar design conditions were selected for the control circuit of Figure 11 (c), which employs two hysteretic controllers in order to implement a dead-band, independently controlling the switches S_1 and S_2. The basic difference in this case is that into the interval $[-\Psi_1, \Psi_1]$ neither switch is activated and the load current $i_o(t)$ is entirely supplied by the correction amplifier.

The current waveforms for steady-state operation and the simulation results for an abrupt load step (from 50% to 100% of load) are shown in Figure 12 (a) and (b), respectively. As can be seen in Figure 12 (b), the dynamic response of the main amplifier was not enough to supply the load current during the transient event. Therefore, the correction amplifier supplied the entire load current during this short period. It is clear that the correction amplifier must be designed for this operation condition. If these events occur occasionally, the designed system efficiency will not be offset.

Figure 12 (c) presents the current waveforms for the system operating with the controller of Figure 11 (c). As shown in Figure 12 (c) (see the shaded area), for low-currents, the main amplifier is turned off and the correction one is responsible for supplying entirely the load current. It must be emphasized that $i_m(t)$ does not reach $i_o(t)$ due to the offset of upper and lower limits of hysteretic controllers in relation to zero, as can be seen in Figure 11 (c). This approach is well-suited for applications where the amplifier does not supply power for long periods, since $i_m(t)$ does not oscillate around zero, and, as a consequence, the correction amplifier can be deactivated too.

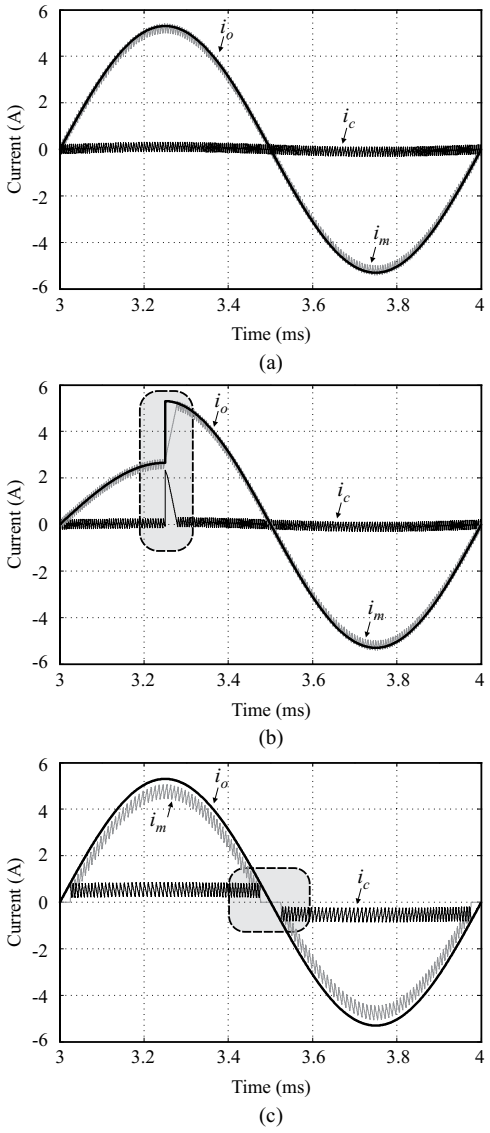

Fig. 12. Simulation results of a half-bridge inverter. (a) Steady-state operation. (b) Abrupt load step (50% to 100%). (c) Hysteretic control with dead-band.

It is important to emphasize that the output linear transistors of the correction amplifier must sustain entirely the load voltage, like the envelope configuration, but the required current can be greatly reduced in comparison to the previous one. In this example, the LPA must be designed to support a peak of 40 V, which limits most of the applications for low-voltages.

V. SERIES CONFIGURATION

In the series configuration of HPAs, the outputs of both main and correction amplifiers are connected in series, as can be seen in the conceptual diagram of Figure 13 (a), where $v_o(t)$ is the load voltage waveform, and $v_m(t)$ and $v_c(t)$ are the voltage waveforms synthesized by the main and correction amplifiers, respectively. While the main amplifier synthesizes a voltage waveform with amplitude close to the reference signal, the correction amplifier operates to compensate for any distortion observed in the voltage waveform synthesized by the former, operating as a series active power filter. Hence, if

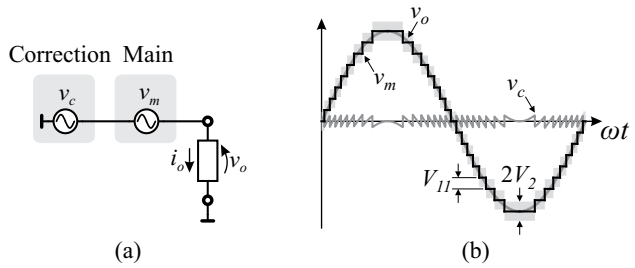

Fig. 13. Series configuration [10]–[11]. (a) Diagram of the general scheme. (b) Main waveforms.

the main amplifier was able to provide high-fidelity voltage waveforms by itself, a low-voltage correction amplifier can be employed and a low-power and low-losses correction amplifier can be used. Therefore, the series configuration is suitable for high-voltages, as ACPS applications, where voltage levels of up to 400 V are required when the mains voltage is emulated [11], for instance.

Figure 13 (b) presents an example of the key voltage waveforms of a series configuration amplifier. In this case, the main amplifier synthesizes a stepped voltage waveform v_m(t) (for example, using a multilevel inverter) very close to the sinusoidal reference and the correction one synthesizes only the remaining difference $v_c(t)$. It is important to emphasize that the voltage steps (defined as V_{11}) must be within the compensation capability of the correction amplifier, limited by its constant dc bus voltage level (defined as V_2). This capability is represented in Figure 13 (b) by the shaded area.

The main disadvantage of the series configuration is the limitation imposed by the dc bus voltage level of the correction amplifier V_2, which must be as low as possible to minimize the conduction losses of its output linear transistors [10]. In this way, depending on how the main amplifier is implemented as well as its output filter specifications (if required to attenuate switching harmonics), severe load and/or reference voltage variations may cause distortions on $v_m(t)$ that exceeds the compensation capability of the correction amplifier.

A. Common Series Topologies

The simplest topology of a series configuration amplifier is represented in Figure 14 (a), which is composed of a half-bridge inverter, operating as main amplifier, and an LPA, operating as correction amplifier [31]. The main disadvantage of this topology is the use of a second-order output low-pass filter (composed of L_1, L_2 and C) to attenuate high-frequency harmonics generated by the PWM. This filter severely limits the dynamic response of the main amplifier, and also introduces a phase displacement between $v_m(t)$ and the reference voltage waveform, which must be compensated by the correction amplifier. Alternatively, Beltrame et al [32] proposed a topology composed of a symmetrical multilevel inverter with n cascaded full-bridge cells and modulated in phase-shift PWM, as shown in Figure 14 (b), enabling to minimize the output low-pass filter requirements. This way, an improved dynamic response can be achieved with the reduction of the output low-pass filter.

Additionally, some researchers have proposed alternatives to eliminate the output filter. For instance, a voltage-source symmetrical multilevel inverter with n cascaded full-bridge cells (similar to that of Figure 14 (b), but without the output low-pass filter), employing a low-frequency modulation based on the nearest level control [33] was proposed in [11] for an ACPS application. The great advantage of the topology of Figure 14 (b) employing the nearest level control modulation is its fast dynamic response to load and/or reference variations. The main benefit of this topology is the modularity, since semiconductor devices with the same voltage/current ratings can be employed in every cell [11], which is very desirable in large scale production. On the other hand, a symmetrical multilevel inverter demands more cells than an asymmetrical topology to generate the same number of voltage levels [34]. Comparatively, nine full-bridge cells were employed by the topology presented in [11] in order to enable the use a commercial low-voltage linear power amplifier as correction amplifier in a high-voltage ACPS application. Meanwhile, if an asymmetrical multilevel inverter with cascaded full-bridge cells were used, it could be

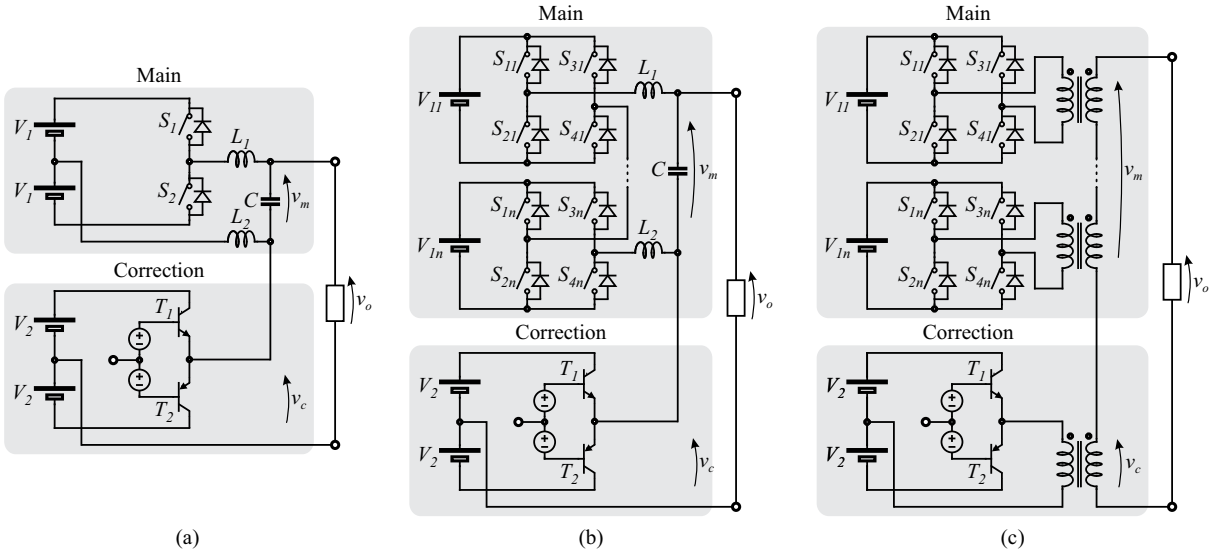

Fig. 14. Topologies employed as main amplifier of the series configuration. (a) Half-bridge inverter [31]. (b) Multilevel inverter with symmetric [11] and [32], and asymmetric [35] cascaded full-bridge cells. (c) Multilevel inverter with output transformer [36].

demonstrated that only three cells would be required to synthesize the same number of voltage levels.

In this way, Mueller and Park [35] have proposed the use of an asymmetrical multilevel inverter with n cascaded full-bridge cells to implement the main amplifier in a magnetic resonance imaging (MRI) system, where voltage waveforms of up to 1.2 kV are synthesized to generate gradient coil currents with fast ramp time. Again, the modulation based on the nearest level control [33] was used for the main amplifier, and the steps on the main amplifier voltage waveform are sufficiently small to be compensated by a low-voltage and low-power correction amplifier.

It must be pointed out that all dc voltage sources of both main and correction amplifiers of Figure 14 (a) and (b) must present galvanic isolation. To overwhelm this restriction, Hammond [36] has proposed the topology of Figure 14 (c), which implements the connection between the multilevel cells and the LPA by means of an output low-frequency transformer. On the other hand, this topology is not able to synthesize ac voltage waveforms with a superimposed dc component due to the presence of an output transformer, which may be also bulky due to the low-frequency operation.

B. Common Control Techniques for Series Topologies

Differently from the previous arrangements, the main amplifier of the series configurations is open-loop controlled whereas the correction amplifier can be controlled in open-loop or closed-loop. This way, this section focuses on the correction amplifier control. The control approaches normally used in the series configuration of HPAs are restricted to

(i) Feed-forward compensation [31] (open-loop); and/or
(ii) Phase lead and lag compensation (closed-loop) [32].

Generally speaking, an amplifier can be employed as an arbitrary waveform generator (e.g., as a general purpose laboratory voltage source) or as an actuator in a control process (e.g., as an adjustable-speed drive). In the first case, when the amplifier is intended to be used as an arbitrary waveform generator, the main concern is to guarantee a high-fidelity output voltage $v_o(t)$. In this case, a simple approach can be used: a feed-forward compensation (only to compensate for the well-known attenuation of the filter) [31], as presented in Figure 15 (a). In this figure, $G_{ff1}(s)$ and $G_{ff2}(s)$ are the filters employed, respectively, to control the main, $G_m(s)$, and correction amplifier plants, $G_c(s)$.

In the second case, it is mandatory to make $v_o(t)$ as close as possible to the reference signal in terms of amplitude and, mainly, of phase in order to not depreciate the phase margin of the process in which the amplifier is being used. Therefore, if an output low-pass filter were used in the main amplifier, as the topologies of Figure 14 (a) and (b), the correction amplifier must compensate for both phase displacement and amplitude attenuation of $v_m(t)$ caused by the low-pass filter. In this case, a closed-loop approach is usually adopted, as presented in Figure 15 (b). As can be seen in Figure 15 (b), the voltage waveform synthesized by the main amplifier v_m(t) is treated as a disturbance for the correction amplifier control loop [32]. In addition, a feed-forward compensation can be even introduced for

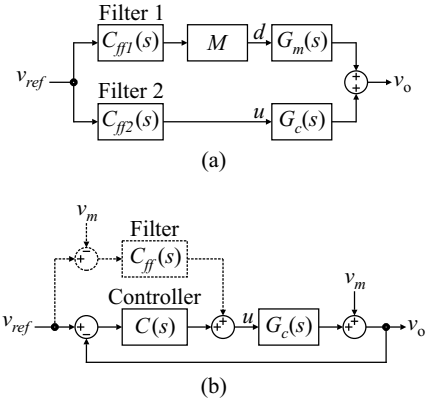

Fig. 15. Common controllers employed for the series configuration. (a) Feed-forward compensation [31]. (b) Phase lead and/or phase lag compensation with [11] or without feed-forward compensation [32].

improving the dynamic response [11], where the difference between $v_{ref}(t)$ and $v_m(t)$ is employed to minimize the impact of the disturbance caused by the main amplifier voltage waveform.

It must be emphasized that the main amplifier of Figure 14 (b), without an output low-pass filter, does not suffer with phase lag at output voltage waveform and can be operated in open-loop, as aforementioned. Meanwhile, the LPA is controlled in closed-loop with an interesting feature: a simple proportional controller can be adopted [11], since the LPA transfer function exhibits an integral behavior, as demonstrated in [32]. Hence, the transfer function of the LPA is used in association with the proportional controller to compose a PI controller (i.e., $C(s)$ and $G_c(s)$ in Figure 15 (b) are integrated into the same block).

C. Example and Simulation Analysis

Some characteristics of the series configuration of HPAs are illustrated in the simulation analysis carried out in this section. As an example, a multilevel inverter with symmetric cascaded full-bridge cells, Figure 14 (b), used in an ACPS application [11] is considered. In this example, the correction amplifier is closed-loop controlled and the main amplifier is open-loop controlled.

The simulation circuit and the control circuit are presented in Figure 16 (a) and (b), respectively. The design considerations for the circuit are presented in [11], while a detailed control design is described in [32]. The main specifications are: P_o = 1 kW (output power); V_{11} =…= V_{19} = 40 V (dc bus voltage of the main amplifier); V_2 = 50 V (dc bus voltage of the correction amplifier); L = 10 µH (output filter inductor); C = 220 nF (output filter capacitor); L_d = 68 µH (damping inductor); R_d = 5 Ω (damping resistor); and $v_{ref,rms}$ = 270 V @ 400 Hz (reference voltage). Although the topology of Figure 16 (a) is modulated in low-frequency (nearest level control), there is the necessity of an output low-pass filter (composed of L, C, L_d and R_d) to limit the slew-rate in the voltage steps of $v_m(t)$. This constraint is mandatory due to the limited bandwidth of the correction amplifier. The controller of the correction amplifier is a simple PI controller that makes use of the integral characteristic of the LPA transfer function [32]. In this example, the power bandwidth is 5 kHz and the control bandwidth is 600 kHz.

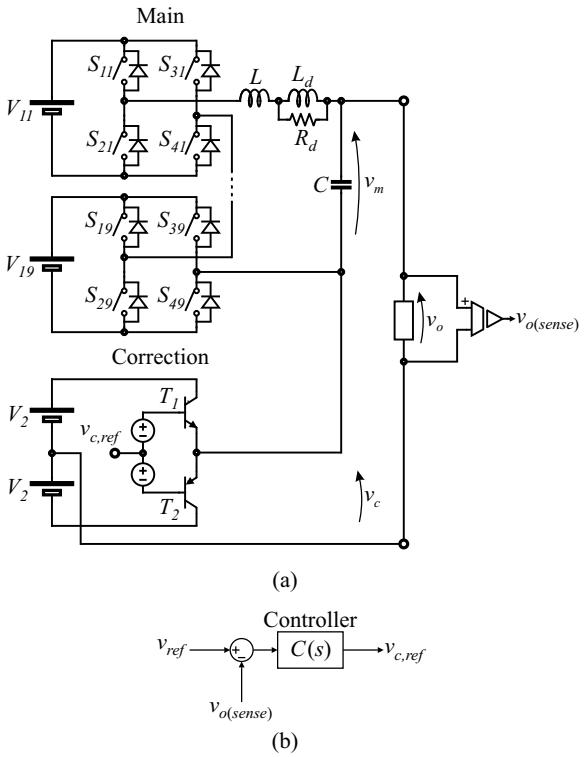

Fig. 16. Simulation of a multilevel inverter with nine symmetric cascaded full-bridge cells [11]. (a) Topology. (b) Control approach [11], [32].

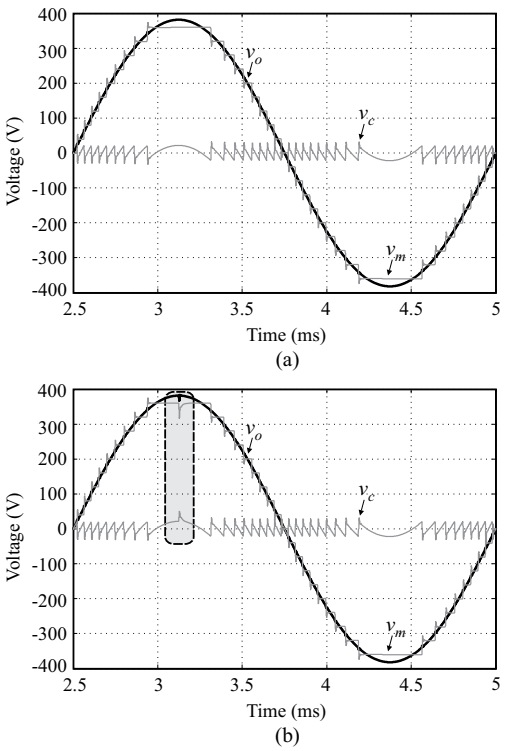

Fig. 17. Simulation results of a multilevel inverter with symmetric cascaded full-bridge cells. (a) Steady-state operation. (b) Abrupt load step (0 to 100%).

The voltage waveforms for steady-state operation are shown in Figure 17 (a). As one can see, the correction amplifier is synthesizing a steady-state voltage waveform to compensate for the difference between $v_{ref}(t)$ and $v_m(t)$ (i.e., the voltage steps and oscillations introduced by the output low-pass filter).

Furthermore, the simulation results for an abrupt load step (from no-load to full-load) are shown in Figure 17 (b) (see the shaded area). The undershoot observed in $v_m(t)$ could not be completely compensated by the correction amplifier, since it clamped at V_2 (saturation) and a distortion can be observed in $v_o(t)$. It is important to note that the correction amplifier conducts entirely the load current.

VI. QUALITATIVE ANALYSIS

From the characteristics of envelope, parallel and series configuration of HPA topologies presented hitherto, it is possible to identify the operation boundaries of each arrangement, as sketched in Figure 18.

For this analysis, it is assumed that

(i) The LPA (correction amplifier) is designed *a priori* with the desired control bandwidth and rated power (defined by the maximum voltage, $v_{c,max}$, and current, $i_{c,max}$, of its linear output transistors); and

(ii) An HPA technology is intended to be used to maximize the efficiency of the whole amplifier.

Therefore, regarding Figure18, three regions can be defined:

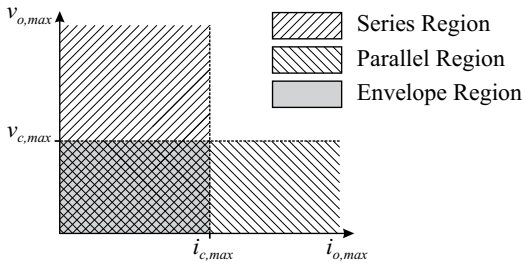

Fig. 18. Operation boundaries of envelope, parallel and series configuration of HPAs.

(i) *Series region*: this region is limited by the condition ($i_{o,max} < i_{c,max}$). It means that the maximum output voltage, $v_{o,max}$, can assume any value while the maximum output current, $i_{o,max}$, must be lesser than the correction amplifier capability, since it conducts entirely the load current in the series configuration.

(ii) *Parallel region*: this region is bounded by the condition ($v_{o,max} < v_{c,max}$). It indicates that the maximum output current, $i_{o,max}$, can assume any value while the maximum output voltage, $v_{o,max}$, must be lesser than the correction amplifier capability, since it sustains entirely the load voltage in the parallel configuration.

(iii) *Envelope region*: this region is limited by the conditions ($v_{o,max} < v_{c,max}$) and ($i_{o,max} < i_{c,max}$), i.e., both maximum output voltage, $v_{o,max}$, and current, $v_{o,max}$, must be lesser than the correction amplifier capability. The main goal in this case is not related to extend the power range of the whole amplifier (limited by the LPA), but to improve the converter efficiency by reducing the voltage through the output transistors of the LPA.

Figure 19 shows a design oriented flowchart based on the operation boundaries given in Figure 18. As can be seen in Figure 19, the suitable configuration of HPA can be identified and selected in a straightforward way for a given LPA (correction amplifier) specification.

VII. CASE STUDY

In order to illustrate the features of HPAs, an experimental case study is carried out in this section. The application example is an amplifier used as an ACPS to create the test conditions for electronic equipments employed in aircraft applications, which operate at 115 V @ 400 Hz [37]–[38].

Initially, it is necessary to define the well-suited configuration for this application. Thus, the basic specifications of the amplifier are presented in Table I. Due to the high bandwidth (500 kHz), high slew-rate (130 V/μs) and relative low cost, the off the shelf LPA Apex® MP111A was selected for this application. It can be noted from Table I that the correction amplifier cannot supply entirely the output voltage, i.e., $v_{o,max} > v_{c,max}$. On the other hand, it can supply entirely the output current, since $i_{o,max} < i_{c,max}$. This way, by making use of the flowchart of Figure 19, it is possible to conclude that the series configuration of HPA (detailed in Section V) is the unique possible arrangement for this application.

Therefore, in this case study, the topology of Figure 14 (b) is selected and analyzed experimentally, which employs an output low-pass filter and the phase-shift PWM strategy. The design considerations are given in [32]. The main and correction amplifier specifications are summarized in Table II.

Figure 20 (a) presents the voltage and current waveforms of both main and correction amplifiers supplying a linear load at full power for a reference voltage of $v_{ref,rms}$ = 115 V @ 400 Hz. As can be seen, the correction amplifier is synthesizing a steady-state voltage waveform to compensate for the difference between $v_{ref}(t)$ and $v_m(t)$ (i.e., voltage ripple, and phase and attenuation introduced by the output low-pass filter). Furthermore, Figure 20 (b) shows the same variables under a non-linear load (single-phase uncontrolled rectifier). Although v_m(t) presents a considerable distortion, the quality of the output voltage $v_o(t)$ is guaranteed by the correction amplifier.

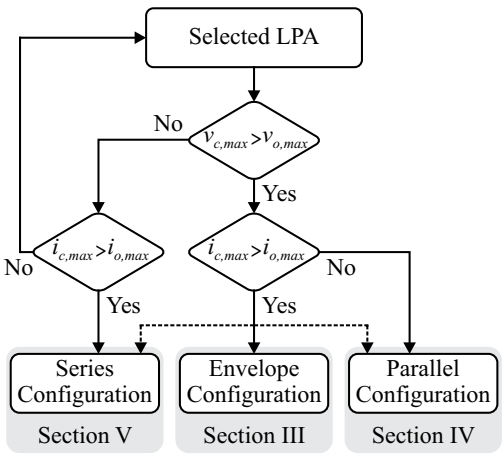

Fig. 19. Flowchart for selection of the appropriate HPA arrangement.

TABLE I
Power amplifier specifications

Converter	Parameter	Value
Power amplifier (ACPS)	Output power	P_o = 500 W
	Output voltage	$v_{o,rms}$ = [0, 115] V
	Output frequency	f = [50, 1200] Hz
	Max. output voltage	$v_{o,max}$ = 165 V
	Max. output current	$i_{o,max}$ = 6.5 A
Correction amplifier (Apex® MP111A)	Max. output voltage	$v_{c,max}$ = 42 V
	Max. output current	$i_{c,max}$ = 15 A

TABLE II
Main and correction amplifier specifications

Converter	Parameter	Value
Main amplifier	Number of cells	n = 3
	Dc bus voltage levels	V_{11} = 66.70 V V_{12} = 66.70 V V_{13} = 66.70 V
	Output low-pass filter	C = 2 μF $L_1 = L_2$ = 44 μH
Correction amplifier (Apex® MP111A)	Dc bus voltage level	V_2 = 22.20 V

In Figure 20 (c) the waveforms for a load step from no-load to 60% of the rated power are presented. The voltage synthesized by the main amplifier $v_m(t)$ presents an undershoot right after the load step event, which is completely compensated by the correction amplifier $v_c(t)$, resulting in an output voltage waveform $v_o(t)$ without any distortion. The capability of the ACPS in synthesizing arbitrary voltage waveforms is demonstrated in Figure 20 (d), where a triangular voltage waveform with amplitude of 155.56 V and frequency of 400 Hz is produced.

In order to evaluate the voltage waveforms, the total harmonic distortion (THD) was measured for no-load to full-load for linear and non-linear loads by using the digital power meter Yokogawa® WT1600. The measured THD was below 0.27% for linear loads and 0.63% for nonlinear loads. Finally, the converter efficiency was experimentally evaluated for both linear and nonlinear loads, and the obtained results are plotted in Figure 21. As we can see, the efficiency of the ACPS supplying a nonlinear load is higher than that for a linear load. This feature can be explained by comparing Figure 20 (a) and (b). It is possible to observe that the correction amplifier is more required to compensate the distortions caused by nonlinear loads. Therefore, it supplies more power to load and, as a consequence of any LPA, presents a higher efficiency.

As can be concluded from the aforementioned results, even employing an output low-pass filter, the series configuration of HPAs can be useful to synthesize high-quality voltage waveforms when supplying linear and non-linear loads, as well as arbitrary voltage waveforms.

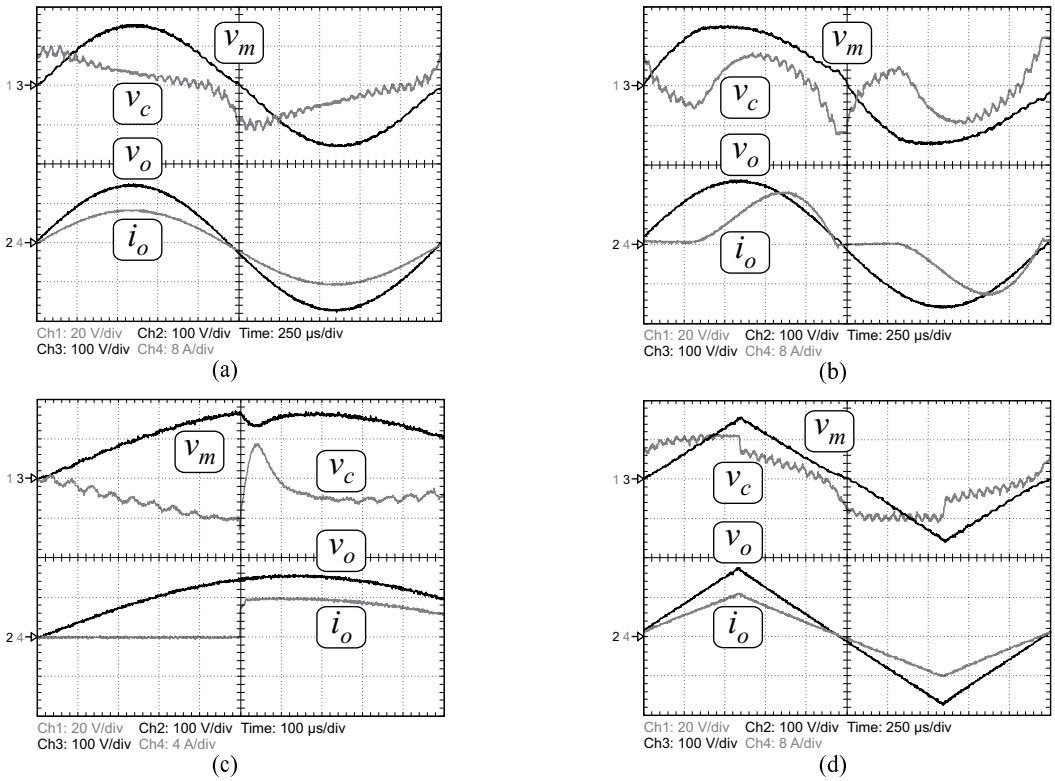

Fig. 20. Experimental results for series configuration. (a) Linear load. (b) Nonlinear load. (c) Load step (0 to 60%). (d) Triangular voltage waveform.

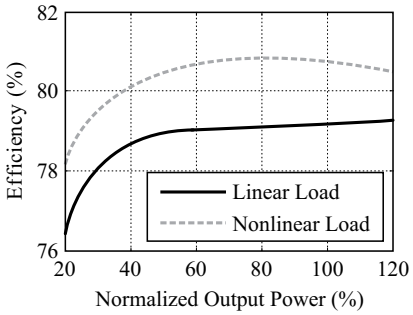

Fig. 21. Efficiency versus normalized output power for two load characteristics ($v_{o,rms}$ = 115 V @ 400 Hz).

VIII. SUMMARY

Aiming to contribute with the advances in the field of power amplification, this work provided a review of the main topologies and control techniques of the three possible arrangements of hybrid power amplifiers, known as envelope, parallel and series configurations.

Since the LPA in envelope configuration must be designed to sustain entirely the load voltage, as discussed in Section III, its use is common in low-voltage applications, as in portable battery-operated systems. These applications demand a high-fidelity main amplifier with high-bandwidth, which is usually achieved by employing very high switching frequencies (e.g., megahertz).

The parallel configuration, discussed in Section IV, is also preferable for low-voltage applications (e.g., audio, RF amplifiers, low-voltage power supplies, etc.), since the LPA must be designed to sustain entirely the load voltage. While the main amplifier supplies the bulk of the load current, the correction amplifier is responsible for setting the required load voltage. Thus, only a small current is circulating through the correction amplifier, enabling to minimize the losses through its output linear transistors. It must be pointed out that the LPA can be designed to provide full power during small periods, guaranteeing the output voltage waveform fidelity even during a severe transient event.

The least explored possibility until now, the series arrangement of hybrid power amplifiers, was discussed in Section V. This configuration is useful for high-voltage applications, such as ACPS applications. The main disadvantages of the series configuration are the demand for limiting the slew rate of main amplifier (through the gate-driver circuit or by inserting an output low-pass filter) in order to enable the correction amplifier to compensate for the voltage steps when the nearest level control is employed, and the saturation of correction amplifier during severe transient events due to its limited dc bus voltage. The series configuration of hybrid power amplifiers has not been deeply explored in literature, remaining a great of its potential still unrevealed. For instance, different multilevel inverters can be explored to implement the main amplifier of Figure 14 (b) aiming to reduce the component count.

Hence, this paper can be viewed as a useful tool to aid the designer engineer in the identification of a suitable Hybrid Power Amplifier for a given application.

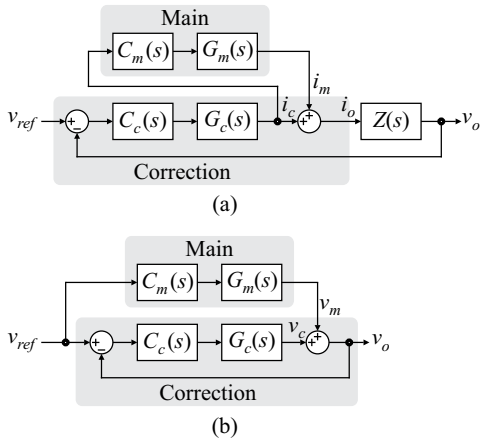

Fig. 22. General control loops of hybrid power amplifiers. (a) Parallel configuration. (b) Series configuration.

APPENDIX

CLOSED-LOOP CONTROL ANALYSIS OF PARALLEL AND SERIES CONFIGURATIONS OF HPAs

In this section an analysis is carried out to demonstrate that the global dynamic of parallel and series configuration of HPAs is determined by the correction amplifier. Figure 22 presents the general control diagrams of both parallel and series configurations, where $C(s)$ denotes the transfer function of controllers, $G(s)$ denotes the transfer function of converters and $Z(s)$ denotes the transfer function of load (the subscripts "m" and "c" refer to main and correction amplifiers, respectively).

Differently from Section IV and V, in this case, both the main and correction amplifier control loops are taken into account. Additionally, it is assumed for this small-signal analysis that, after proper design of the controllers, the control bandwidth of correction amplifier is much greater than that of the main amplifier. This condition implies that the open-loop crossover frequency of the correction amplifier, f_c, is much greater than that of the main amplifier, f_m.

A. Parallel Configuration Transfer Functions

As discussed in Section IV for the parallel configuration, the correction amplifier is responsible for defining the load voltage, while the main amplifier supplies almost entirely the load current. The complete control diagram of the parallel configuration is shown in Figure 22 (a). From Figure 22 (a), it is possible to demonstrate that the closed-loop input-to-output transfer function is given by

$$\frac{v_o(s)}{v_{ref}(s)} = G_{LPA}(s) + G_{Sw}(s), \tag{1}$$

where

$$G_{LPA}(s) \triangleq \frac{C_c(s)G_c(s)Z(s)}{1+C_c(s)G_c(s)Z(s)\left[1+C_m(s)G_m(s)\right]} \tag{2}$$

and

$$G_{Sw}(s) \triangleq \frac{C_c(s)G_c(s)C_m(s)G_m(s)Z(s)}{1+C_c(s)G_c(s)Z(s)\left[1+C_m(s)G_m(s)\right]}. \tag{3}$$

If the controller $C_c(s)$ is designed to guarantee stability for the correction amplifier, and provided that $C_c(s)G_c(s)Z(s) \gg 1$ and $C_m(s)G_m(s) \ll 1$ in the desired frequency range (e.g., $f_m < f < f_c$), we can see from (2) that $G_{LPA}(s) \to 1$, and from (3) that $G_{Sw}(s) \to 0$. It means that, with the proper design of $C_c(s)$, the correction amplifier defines the output voltage. Additional details for other frequency ranges are provided in [28].

B. Series Configuration Transfer Functions

As presented in Section V for the series configuration, the main amplifier synthesizes a voltage waveform with amplitude close to the reference signal and the correction amplifier operates to compensate for any distortion on it. Thus, only the correction amplifier operates in closed-loop control, as shown in Figure 22 (b), although a feed-forward compensation (represented by $C_m(s)$ in this case) can be used for the main amplifier. More importantly, the main amplifier can be treated as a disturbance at the output of the correction amplifier, as shown in Figure 22 (b). Therefore, it is possible to derive the closed-loop input-to-output transfer function as

$$\frac{v_o(s)}{v_{ref}(s)} = G_{LPA}(s) + G_{Sw}(s), \tag{4}$$

where

$$G_{LPA}(s) \triangleq \frac{C_c(s)G_c(s)}{1+C_c(s)G_c(s)} \tag{5}$$

and

$$G_{Sw}(s) \triangleq \frac{C_m(s)G_m(s)}{1+C_c(s)G_c(s)}. \tag{6}$$

If the controller $C_c(s)$ is designed to guarantee stability for the correction amplifier, and provided that $C_c(s)G_c(s) \gg 1$ and $C_c(s)G_c(s) \gg C_m(s)G_m(s)$ in the desired frequency range (e.g., $f_m < f < f_c$), we can see from (5) that $G_{LPA}(s) \to 1$, and from (6) that $G_{Sw}(s) \to 0$. This way, with the proper design of $C_c(s)$, the correction amplifier not only defines the output voltage, but also rejects the perturbation on $v_o(t)$ caused by the main amplifier.

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