A NEGATIVE-SEQUENCE CURRENT INJECTION METHOD TO MITIGATE VOLTAGE IMBALANCES IN MICROGRIDS

Gustavo M.S. Azevedo[1], Joan Rocabert[2], Marcelo C. Cavalcanti[1], Francisco A.S. Neves[1], Pedro Rodriguez[2]
[1]Federal University of Pernambuco (UFPE - DEE), Recife - Brazil
[2]Technical University of Catalonia (UPC), Barcelona - Spain
gustavomsa@aim.com, marcelo.cavalcanti@ufpe.br, fneves@ufpe.br

***Abstract* - This paper proposes a control strategy to reduce the voltage imbalances by injection of a proper negative-sequence current into the microgrid. This task can be done by each inverter connected to the microgrid in a shared way. The current compensation reference is obtained through a negative-sequence voltage control loop, avoiding the load current measurement. The detection of the negative-sequence voltage, at the converter connection point, is performed by a double second order generalized integrator, properly tuned for this purpose. Besides, a current limiter is used to limit the current compensation and avoid the converter overload. This strategy neither requires any hardware modification of the converter nor additional sensors. This new control strategy is simulated in Matlab/Simulink and experimental results are presented to prove its effectiveness.**

***Keywords* – Microgrids, Distributed Generation Systems, Unbalanced Load.**

I. INTRODUCTION

Microgrid (MG) has been proposed for effective integration of distributed energy resources (DERs) to the utility grid to provide high quality and high reliability electric power for the end-users [1]-[3]. The MG is connected to the main grid at the point of common coupling (PCC), but it should be able to operate with or without this connection. The DERs are connected to local electric grid through power conditioning units. Thus, inverters or ac-ac converters are connected to the local loads via a common ac bus. The schematic diagram of a possible MG is shown in figure 1.

Power quality is a key issue in MG and a common problem is the voltage imbalance. Several works have been published on this topic. Some of them focused on mitigating the voltage imbalance due to the main electrical grid [4], [5] and others due to the unbalanced loads [6]-[8]. In a low voltage distribution network there is the increased tendency of significant load imbalance between phases [6]. Three-phase low-voltage MG feed a large variety of loads and some of these loads are single-phase, making the currents delivered by the DERs units unbalanced. Therefore the voltages across the line impedances and consequently the load voltages become unbalanced. A large voltage imbalance can cause abnormal operation, particularly for sensitive loads, increase losses and affect proper operation of rotating generators or motors in the MG [7]. Each DER unit in the MG is able to impose balanced voltage near itself. The inverter control strategy defines if its output voltage will be balanced or unbalanced. The inverters with droop control [9]-[13] can achieve balanced voltages because this strategy controls the inverter output voltage and frequency. However some DERs, like photovoltaic and wind power, can not use droop control because their goal is to deliver all available power. These DER units are current or power controlled, i.e., there is not output voltage control.

This paper proposes a control strategy to mitigate the negative-sequence voltage component in the output of inverters controlled in current mode or power mode. Consequently, it enhances the voltage quality around these inverters. The negative-sequence voltage compensation can be achieved both in grid-connected or islanding mode, but the voltage imbalance level is higher under islanding mode due to the reduction on short-circuit power caused by the absence of the main source. The proposed strategy is based on the injection of negative-sequence current to locally supply the demand of this current component. Although it is a well-known approach, the contribution of this work is the method to generate the compensation voltage reference. The classical method consists of measuring the load current, detect its negative-sequence component and inject it through an inverter, like in [7]. However, in this paper a negative-sequence control loop, based only on the MG voltage measurement, is used to determine the negative-sequence compensation current reference. Thus, the load current measurement is not necessary, and consequently, additional current sensors are not necessary.

II. NEGATIVE-SEQUENCE VOLTAGE COMPENSATION

The system in figure 1 can be represented by a simple Thevenin equivalent circuit as shown in figure 2. All elements on the left side of the point A (figure 1) were represented by a voltage source, v_s, and an equivalent line impedance, Z_s. The loads on the right side of A are represented by an impedance, Z_L, and the converter by a controlled current source.

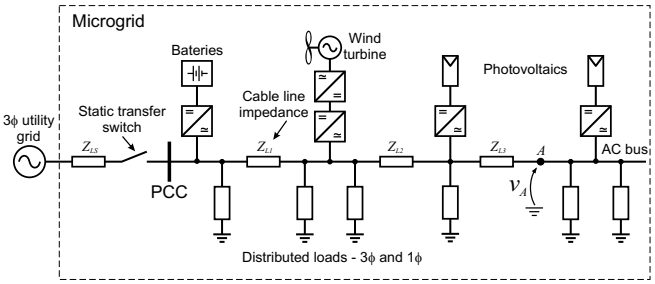

Fig. 1. Example of a possible MG configuration.

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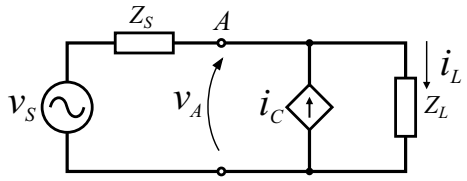

Fig. 2. Equivalent circuit in the MG of figure 1 at the point A.

A. Equivalent circuit of the MG

Assuming initially that the converter currents are balanced, if Z_L is balanced the load currents have only positive-sequence components and the voltages across the line impedance have only positive-sequence too. On the other hand, if the load is unbalanced the load currents have both positive- and negative-sequence components. The latter component results on unbalanced voltages across the line impedance, and consequently across the load. The load voltages unbalance can be eliminated by compensating the negative-sequence currents demanded by the loads. Fortunately, the inverter connected near to the loads can be used to do it. Thus a proper detection of the load current components to perform the compensation is necessary. However, current sensors are not a suitable choice because there might be more than one load, possibly far from the converter. Besides, they increase the cost of the overall system.

Assuming that the voltage source of the system in figure 2 is balanced, the negative-sequence circuit (considering the phasor equivalent circuit) that represent this system is shown in figure 3, where the load was replaced by a current source that demands the same negative-sequence current of the load. When there is no compensation $I_C = 0$ the negative-sequence voltage at the point *A* is given by:

$$\mathbf{V}_A^- = -\mathbf{Z}_s^- \mathbf{I}_L^-, \tag{1}$$

where the superscript "$-$" denotes negative-sequence. Equation (1) can be rewritten as

$$\mathbf{I}_L^- = -\frac{\mathbf{V}_A^-}{\mathbf{Z}_s^-}. \tag{2}$$

Thus the compensation current injected by the converter should be

$$\mathbf{I}_C^- = \mathbf{I}_L^- = -\frac{\mathbf{V}_A^-}{\mathbf{Z}_s^-} \tag{3}$$

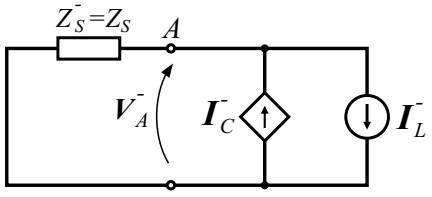

Fig. 3. Phasor equivalent circuit for the negative-sequence component.

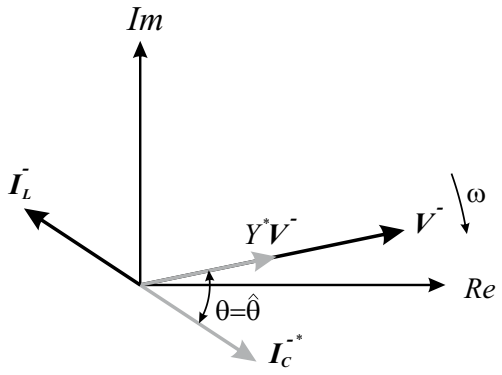

Fig. 4. Phasor diagram of the negative-sequence components.

or

$$\mathbf{I}_C^- = -Y\angle -\theta\, \mathbf{V}_A^- \tag{4}$$

$$\mathbf{I}_C^- = \left(-Y\, \mathbf{V}_A^-\right) e^{-j\theta}, \tag{5}$$

where Y is the absolute value of the line admittance (the inverse of $\mathbf{Z}_s^-$) and θ is the line impedance phase angle. From (4) note that the compensation current is proportional to the negative-sequence voltage and its phase angle is shifted $\pi - \theta$, as shown in figure 4.

B. Proposed control

The proposed compensation control is based on estimation of the current compensation using only the negative-sequence voltage measured on the ac bus. The control algorithm calculates the absolute value of $\mathbf{V}_A^-$ and forces it to zero through a proportional-integral (PI) compensator. The control diagram is shown in figure 5. The first block is a sequence calculator based on a dual second order generalized integrator (DSOGI) [14], [15], which is discussed in next subsection. This block obtains the instantaneous negative-sequence component of the converter output voltage vector on stationary reference frame. The magnitude of $\mathbf{V}^-$ passes through a low-pass filter (LPF) to smooth the load transients and the voltage disturbances due to the injection of currents by the inverter. Besides, this filter is used to impose the dynamics of the compensation system and make it stable.

The compensation current amplitude depends on the voltage imbalance, which is usually due to the unbalanced loads.

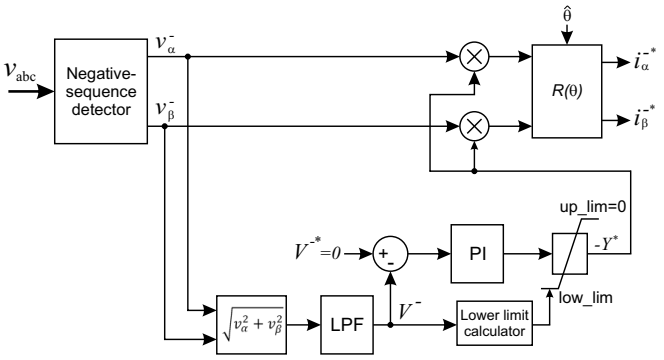

Fig. 5. Control diagram of the negative-sequence compensator.

However, sometimes the electrical grid voltage could be imbalanced, for instance, during a fault. The latter case could result in high compensation currents that can overpass the converters rated limits. Therefore, a current limiter must be implemented to avoid the converter overcurrent trip. The compensation current amplitude can be limited indirectly by means of a saturation in the admittance reference, $-\mathbf{Y}^*$, as shown in figure 5. The upper limit defines the minimum current amplitude, hence it must be zero. On the other hand, the lower limit defines the maximum current amplitude and it changes with the $\mathbf{V}^-$ amplitude. From (4) it can be deduced that

$$-Y_{low\_lim} = -\frac{I^-_{MAX}}{V^-}, \tag{6}$$

where I^-_{MAX} is the maximum admissible amplitude of the current compensation.

The latest block in figure 5 is a phase-shift transformation to make the current compensation phasor in phase with the negative-sequence load current as shown in figure 4. This is obtained by the rotating transformation:

$$R(\hat{\theta}) = \begin{bmatrix} \cos(\hat{\theta}) & -\sin(\hat{\theta}) \\ \sin(\hat{\theta}) & \cos(\hat{\theta}) \end{bmatrix}, \tag{7}$$

where the symbol " ˆ " denotes an estimated parameter. It should be noted that this transformation is applied to a negative-sequence component, thus positive angles give phase lag, while negative angles give phase lead. The angle $\hat{\theta}$ is obtained by knowing the X/R ratio at the connection point of the inverter. However, it can be difficult to get this information. Fortunately this angle can be estimated by injecting a known negative-sequence current in the system and observing the deviation in the negative-sequence voltage angle. Nevertheless, in this work it is assumed that the X/R ratio is known, since the X/R estimator is not the focus.

C. Power balancing

The main goal of the DERs is deliver its available power to the electrical grid. Usually, it is made only by means of positive-sequence currents. In normal conditions, i.e., when the grid voltages and injected currents are balanced, the power components delivered by the converter are

$$p = \vec{v}\cdot\vec{i} = VI\cos\phi \tag{8}$$

$$q = |\vec{v}\times\vec{i}| = \vec{v}_\perp\cdot\vec{i} = VI\sin\phi \tag{9}$$

where $\vec{v}$ is the three-phase voltage vector, $\vec{i}$ is the converter output current vector, ϕ is the phase between $\vec{v}$ and $\vec{i}$ and the symbol "$\perp$" denotes ortogonal component. Note that these power components are constant in this case. Otherwise, under unbalanced voltages and considering that the converter is injecting the negative-sequence current for compensation, the power components become

$$p = \vec{v}\cdot\vec{i} = (\vec{v}^+ + \vec{v}^-)\cdot(\vec{i}^+ + \vec{i}^-) = \underbrace{\vec{v}^+\cdot\vec{i}^+ + \vec{v}^-\cdot\vec{i}^-}_{P} + \underbrace{\vec{v}^+\cdot\vec{i}^- + \vec{v}^-\cdot\vec{i}^+}_{\tilde{p}} \tag{10}$$

and

$$q = \vec{v}_\perp\cdot\vec{i} = (\vec{v}^+_\perp + \vec{v}^-_\perp)\cdot(\vec{i}^+ + \vec{i}^-) = \underbrace{\vec{v}^+_\perp\cdot\vec{i}^+ + \vec{v}^-_\perp\cdot\vec{i}^-}_{Q} + \underbrace{\vec{v}^+_\perp\cdot\vec{i}^- + \vec{v}^-_\perp\cdot\vec{i}^+}_{\tilde{q}} \tag{11}$$

Note that the interaction between the voltages and currents with different sequences gives rise to power oscillating components at twice grid frequency, which are represented by $\tilde{p}$ and $\tilde{q}$. The constant components are represented by P and Q. If the power components only due to the compensation are separated, it results in

$$p_c = \underbrace{\vec{v}^-\cdot\vec{i}^-}_{P_c} + \underbrace{\vec{v}^+\cdot\vec{i}^-}_{\tilde{p}_c} \tag{12}$$

$$q_c = \underbrace{\vec{v}^-_\perp\cdot\vec{i}^-}_{Q_c} + \underbrace{\vec{v}^+_\perp\cdot\vec{i}^-}_{\tilde{q}_c}. \tag{13}$$

Equation (12) shows that it is necessary to have active power available at the convert dc side to compensate the negative-sequence. Thus, DERs based on photovoltaic, wind power or any unpredictable source could not perform the compensation when its power is not available. Theses equations also reveal that the compensation increases the power oscillation, therefore the dc bus capacitor should be designed to take it into account.

D. Negative-sequence detection

The correct detection of the negative-sequence component of the grid voltages is a key issue to obtain the compensation current reference. There are many ways to extract the negative-sequence component, such as the decoupled double synchronous reference frame PLL [16] and the methods based on mathematical transformations [17]- [19] or adaptive filters [15] [20]. Regarding the latter one, in [14], [15] is presented a detection system called DSOGI frequency-locked loop (DSOGI-FLL), which has good performance, even under imbalance and harmonic conditions. Besides, this method is easy to implement in any digital signal processor and it does not require neither larger memory nor high computational power. The basis of the DSOGI-FLL is the concept of symmetrical components proposed by *Fortescue* in 1918 [21] and that was extended to the time-domain by *Lyon* [22]. According to *Lyon*, the positive- and negative-sequence of a generic three-phase voltage vetor, $\vec{v} = [v_a\ v_b\ v_c]^T$, is given by

$$\vec{v}^+ = \left[T^+\right]\vec{v} = \frac{1}{3}\begin{bmatrix} 1 & \alpha & \alpha^2 \\ \alpha^2 & 1 & \alpha \\ \alpha & \alpha^2 & 1 \end{bmatrix}\vec{v} \tag{14}$$

$$\vec{v}^- = \left[T^-\right]\vec{v} = \frac{1}{3}\begin{bmatrix} 1 & \alpha^2 & \alpha \\ \alpha & 1 & \alpha^2 \\ \alpha^2 & \alpha & 1 \end{bmatrix}\vec{v} \tag{15}$$

where $\alpha = e^{j2\pi/3}$. In an orthogonal stationary reference frame, $\alpha\beta$, these equations result in

$$\vec{v}^+_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} 1 & -\delta \\ \delta & 1 \end{bmatrix}\vec{v}_{\alpha\beta} \tag{16}$$

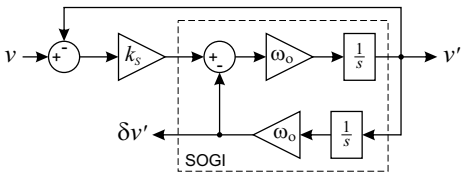

Fig. 6. Scheme of the SOGI-QSG.

$$\vec{v}^{-}_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} 1 & \delta \\ -\delta & 1 \end{bmatrix}\vec{v}_{\alpha\beta} \tag{17}$$

where $\delta = e^{j\pi/2}$ is a phase-shift time-domain operator to obtain in-quadrature version (90^0-lagging) of an original waveform. It is worth to note that the homopolar component does not have effect either on the instantaneous positive- or negative-sequence voltage components in the stationary reference frame.

Several methods for quadrature-signals generator (QSG) have been reported in the literature. A simple and effective way is the use of a second order generalized integrator (SOGI) for quadrature-signals generation. The SOGI-QSG scheme is shown in figure 6 and its characteristic transfer functions are given by:

$$D(s) = \frac{v'(s)}{v(s)} = \frac{k_s\omega_o s}{s^2 + k_s\omega_o s + \omega_o^2} \tag{18}$$

$$\Delta(s) = \frac{\delta v'(s)}{v(s)} = \frac{k_s\omega_o^2}{s^2 + k_s\omega_o s + \omega_o^2}, \tag{19}$$

where ω_o and k_s set resonance frequency and damping factor, respectively. The Bode diagram for the SOGI-QSG outputs, with $\omega_o = 2\pi 60$ and $k_s = 1$, is shown in figure 7. $D(s)$ has characteristic of a band pass filter with bandwidth determined only by k_s (independent of the input signal frequency). On the other hand, $\Delta(s)$ has characteristic of a low pass filter. The phase difference between $D(s)$ and $\Delta(s)$ is always 90^o, independent of the input signal frequency. When the input signal frequency is equal to ω_o the output signals amplitudes are equal to the input amplitude. These characteristics make the SOGI ideal for the quadrature signals generation.

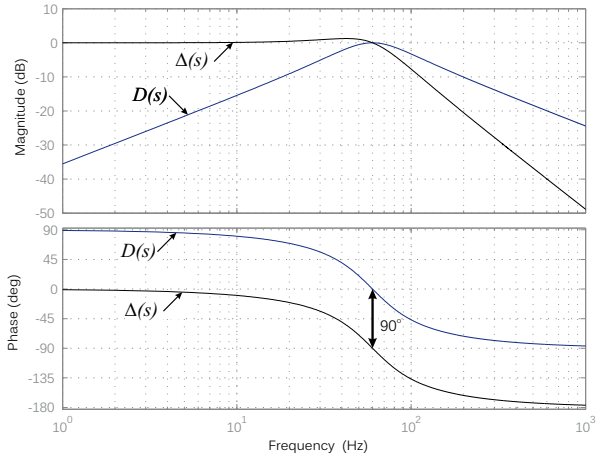

Fig. 7. Bode diagram of $D(s)$ and $\Delta(s)$.

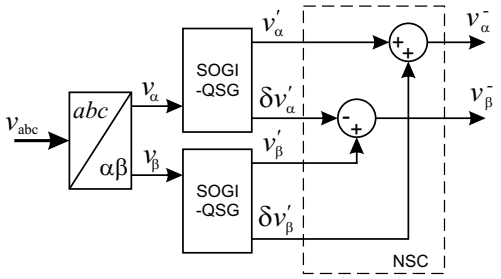

Fig. 8. Schemes of the DSOGI-QSG and the negative-sequence calculation.

Transfer functions (18) and (19) reveal that if v is a sinusoidal signal, v' and $\delta v'$ will be sinusoidal as well. Moreover, $\delta v'$ will be always 90^0-lagging v', independently of both the frequency of v and the values of ω_o and k_s. These equations also reveal that the damping factor set the SOGI dynamics. A lower value of k_s gives rise to a more selective filtering response and a longer stabilization time. However, in this application a slow dynamics is desired to assure the stability of the whole system.

A DSOGI-QSG is necessary to perform the negative-sequence voltage estimation, as evidenced by (17). These SOGIs provide the input signals to the negative-sequence calculator (NSC) as shown in figure 8.

The estimated voltage component magnitude will be correct when ω_o match up the grid frequency. Therefore it is necessary a frequency adaptation system to tune the SOGIs with the grid frequency. The frequency-locked loop (FLL) presented in [15], [23] and [24] is used for this purpose.

III. SIMULATION RESULTS

The performance of the proposed control has been tested in simulations carried out in Matlab/Simulink. The MG shown in figure 1 can be simplified from the perspective of point A as an simple voltage source and its impedance [25]. Thus the MG was modeled by one three-phase voltage source, the line equivalent impedance and some loads (one three-phase and two single-phase). The single-phase loads are connected to phase b through switches. The power converter is composed by a voltage source inverter and a LCL output filter. In order to simplify the simulation the primary source is considered as a constant voltage source. This assumption can be done, since the dc link voltage control dynamics is slow and the dc link capacitance is big enough. In fact, dc voltage oscillation has influence under the current controller and it does not affect the

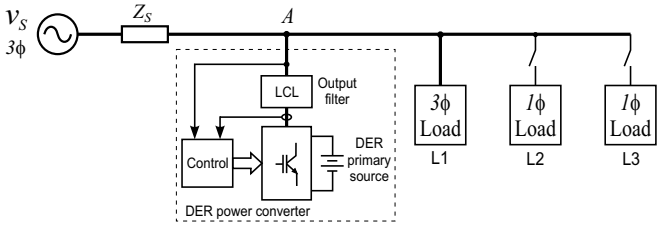

Fig. 9. Simulation set-up.

TABLE I
System parameters used in simulation

Parameter	Value
Load voltage (phase-to-phase)	$380V$
Grid frequency, f_S	$60Hz$
Equivalent line impedance, Z_s	$0.8 + j4\Omega$
Three-phase load power, L_1	$2000 + j300VA$
Single-phase load power, L_2	$1500 + j50VA$
Single-phase load power, L_3	$50 + j1500VA$

proposed control. Therefore, it is desired to keep the dc link voltage constant to evaluate only the behavior of the proposed compensation control. The whole system is shown in figure 9. The most relevant system parameters are shown in Table I.

In order to analyze the behavior of the proposed strategy for different load conditions, the simulation has three stages. In the first one (0 to $100ms$), only the balanced load, L1, is connected to the MG. After that, L2 is connected too. At $400ms$ the load L2 is disconnected and L3 is connected. Load L2 is essentially resistive, whereas L3 is inductive. The MG voltage components are shown in figure 10. In this case the compensation control was disabled. Note that the negative-sequence stays around $10V$ when the unbalanced loads are connected. Besides, the load characteristic (more resistive or inductive) has low effect on the voltage imbalance. The voltage unbalance factor (VUF) in the first stage (only $L1$ connected) is zero, whereas it is 0.051 and 0.043 for the second and third stages, respectively.

The previous simulation is repeated with the compensation control enabled and the converter is adjusted to not deliver active power to the MG. Note that, although the active power reference is set to zero, a low amount of active power is delivered to the MG due to the interaction of the negative-sequence current with the MG voltage. The results for this case are shown in figures 11 and 12. The MG negative-sequence voltage is reduced to less than $2.5V$, as shown in figure 11. The VUF is reduced to 0.011 in both stages (L1 + L2 and L1 + L3). The positive-sequence voltage does not present remarkable changes. The current components consumed by

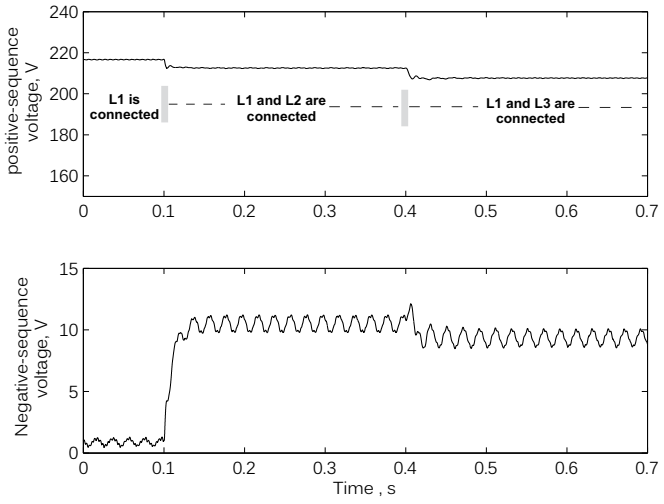

Fig. 10. Positive- and negative-sequence voltage components at the point of connection of the converter (point A in figure 9) without compensation.

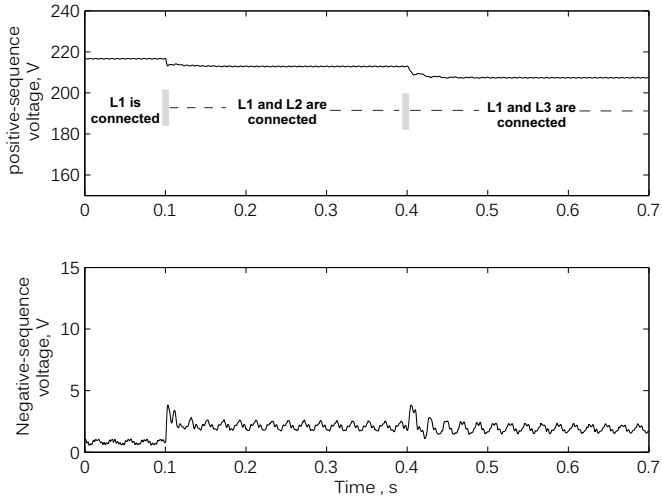

Fig. 11. Voltages when the DER is adjusted to deliver $0\,kW$.

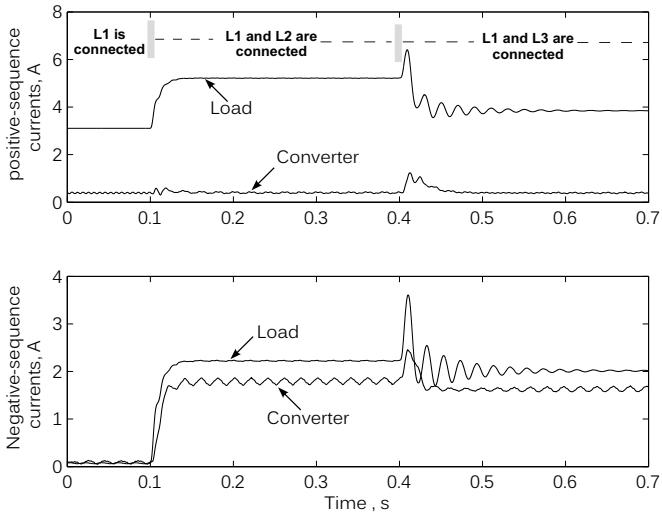

Fig. 12. Load and converter currents when the DER is adjusted to deliver $0\,kW$.

the loads and delivered by the converter are shown in figure 12. The converter positive-sequence current is zero because the active power reference is set to zero. However, it was considered that there is low primary power available to deliver to the MG, since the compensation needs some active power, as was shown by (12). The converter negative-sequence current cannot reach the load current, but it is kept near to it. This steady state error is mainly due to the inaccuracy of the negative-sequence detection for very low voltage imbalances. In addition, the compensation current reference is a portion of the detected negative-sequence voltage, hence, this reference would be lost if the compensation was completed.

When the primary power is available, it is delivered to the MG by positive-sequence current. Figures 13 and 14 show the simulation results when the inverter is adjusted to deliver $1.5kW$ and the loads are the same that were used before. Note that the negative-sequence compensation is not affected by the converter delivering positive-sequence current.

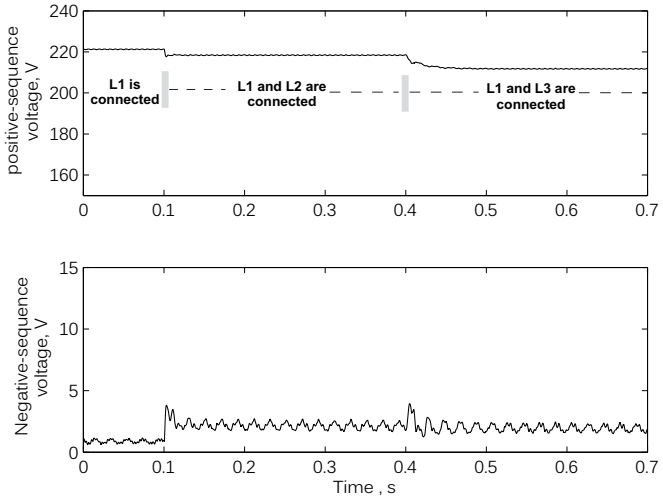

Fig. 13. Voltages when the DER is adjusted to deliver $1.5\,kW$.

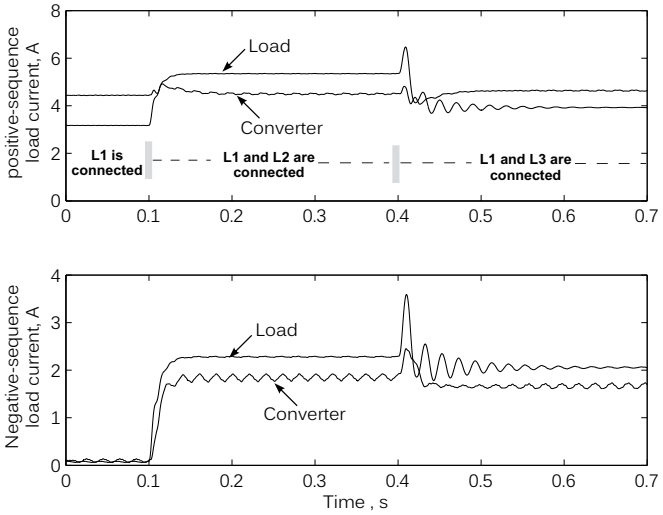

Fig. 14. Load and converter currents when the DER is adjusted to deliver $1.5\,kW$.

IV. EXPERIMENTAL RESULTS

The proposed voltage imbalance compensation was evaluated in an experimental set-up in which part of the MG was emulated by mean of the utility grid (emulating the MG equivalent voltage source) and a set of transformers (emulating the MG line impedance). This set-up is shown in figure 15. The system voltage at point A is $88.4V$ (rms phase-to-neutral) and the equivalent resistance and reactance at this same point, due to the transformers, is 1.7Ω and 6.4Ω, respectively. The load bank has a balanced three-phase resistive load connected

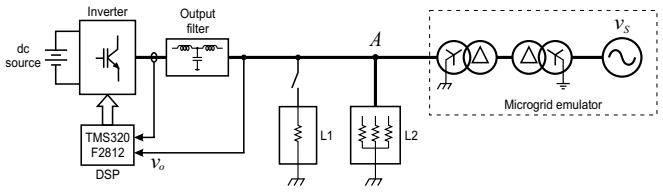

Fig. 15. Experimental set-up.

TABLE II
System parameters used in the experiment

Parameter	Value
Single-phase resistive load, L_1	30.6Ω
Three-phase resistive load, L_2	35.5Ω
Line impedance angle, $\hat{\theta}$	75^o
dc link voltage, V_{dc}	$350V$
Sampling frequency, f	$20kHz$
Switching frequency, f_{sw}	$20kHz$
LPF cut-off frequency, f_c	$5Hz$
Voltage grid angular frequency, ω_S	$376.99\,rad/s$
SOGI resonance frequency, ω_o	$376.99\,rad/s$
SOGI damping factor, k_s	0.1

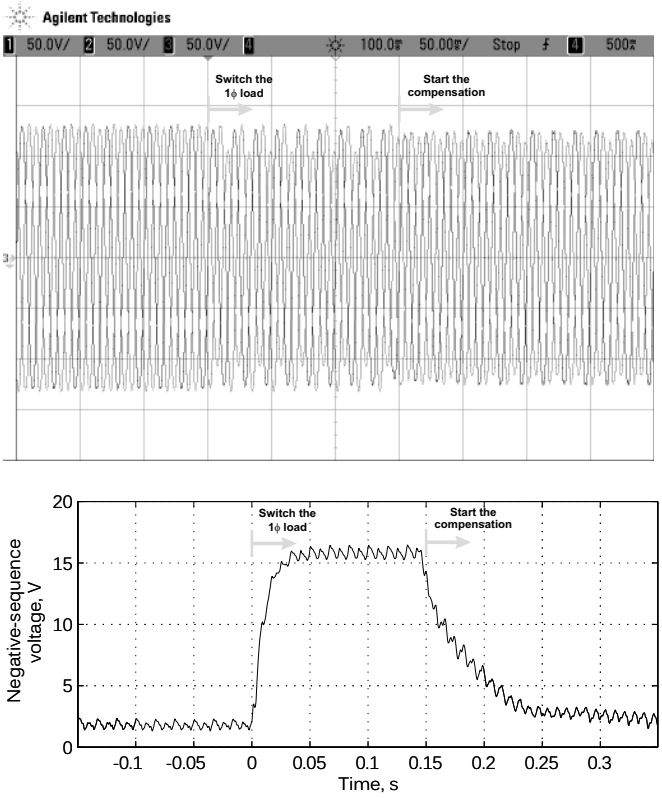

Fig. 16. Results of the voltage imbalance compensation: three-phase voltages at MG ac bus and negative-sequence component

directly to the MG ac bus and a single-phase resistive load, which can be switched to the phase b. The inverter dc side is fed by a dc power source and its output is connected to the MG ac bus through a LCL filter. In this workbench, the control algorithm was implemented in a TMS320F2812, which is a fixed-point DSP that works at $150MHz$. Other system parameters are given in Table II.

The control algorithm was implemented using fixed-point arithmetic. The execution time of the DSOGI-QSG and the NSC together is $754\,ns$. The execution time of the negative-sequence current compensator algorithm, knowing v_α^-, v_β^- and $\hat{\theta}$, is $3,18\,\mu s$. Thus, the total execution time of the proposed compensation algorithm is $3.934\,\mu s$.

In a first experiment, the capability of the negative-sequence voltage compensation was tested. The compensation algorithm begins deactivated and after some time the single-phase load is switched on, resulting unbalanced voltages at ac bus (point A in figure 15). The compensation algorithm

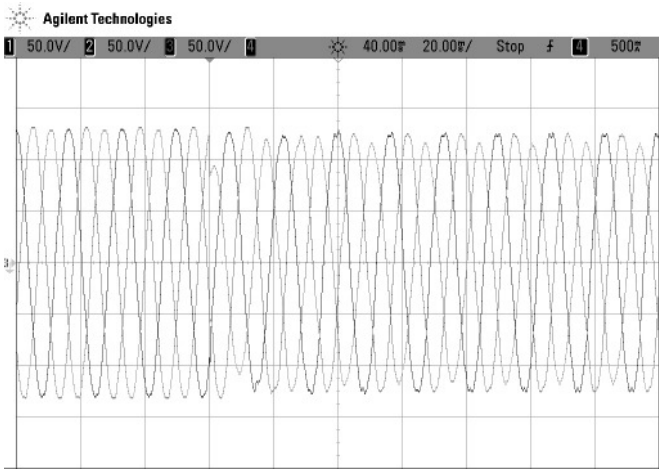

Fig. 17. Dynamics behavior of the compensator.

is enabled $150ms$ later and the voltage imbalance is reduced as shown in figure 16. As it can be noticed, the voltage imbalance rises to over than $15V$ when the loads become unbalanced and it returns to approximately $2.5V$ when the compensator is enabled. The VUF without compensation is 0.170 and it becomes 0.028 when the compensation algorithm is enable. Moreover, it was also observed in this experiment that the utility voltage is unbalanced before switching on the single-phase load. There is a threshold of $1.5V$ in the negative-sequence component to the algorithm start the compensation. This is necessary because for low levels of unbalance the sequence detector accuracy is not good enough and consequently the negative-sequence compensation current references could be wrong.

In second experiment, the compensation dynamics is evaluated. The compensator is always enabled and after some time the single-phase load is switched on. The MG ac bus voltages are shown in figure 17. In can be observed that the algorithm quickly starts to compensate the voltage and it stabilizes in about two cycles of the fundamental frequency.

V. CONCLUSION

This paper proposes a control strategy to mitigate the unbalanced voltages in low-voltage three-phase microgrids. This control technique can be implemented in the DER converters without any modification on the hardware structure. It is not necessary any additional measurement sensor. The negative-sequence voltage compensation is not complete, but the simulation and experimental results show that the negative-sequence component stays below $2.5V$. In the experimental results, the attenuation was around 85%. Therefore it is a very good solution since it does not present any additional cost to the regular system. Although the solution proposed in this work has been developed taking into account the application for microgrids, it can be also effectively used in weak power systems.

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BIOGRAPHIES

Gustavo M. S. Azevedo was born in Belo Jardim, Brazil, in 1981. He received the B.S., M.S. and Ph.D. degrees in electrical engineering from the Federal University of Pernambuco in 2005, 2007 and 2011, respectively. He worked as a visiting scholar at the Polytechnical University of Catalunya, Barcelona, Spain, from 2008 to 2009. His research interests are renewable energy systems and microgrids.

Joan Rocabert was born in Barcelona, Spain. He received the M.Sc. and the Ph.D. degrees in electrical engineering from the Technical University of Catalonia, Barcelona, Spain, in 2003 and 2010, respectively. From 2004 to 2008, he was a Research Assistant in the Department of Electronic Engineering, Technical University of Catalonia, where since 2008 he has been a Researcher and an Assistant Professor with the Department of Electrical Engineering. His research interests are power electronics applied to PV and wind energy systems and microgrids.

Marcelo C. Cavalcanti was born in Recife, Brazil, in 1972. He received the B.S. degree in electrical engineering in 1997 from the Federal University of Pernambuco, Recife, Brazil, and the M.S. and Ph.D. degrees in electrical engineering from the Federal University of Campina Grande, Campina Grande, Brazil, in 1999 and 2003, respectively. He worked as a visiting scholar at Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg - USA, from Oct/2001 to Aug/2002. Since 2003, he has been at the Department of Electrical Engineering, Federal University of Pernambuco, where he is currently a Professor of Electrical Engineering. His research interests are renewable systems and power quality.

Francisco A. S. Neves was born in Campina Grande, Brazil, in 1963. He received the B.S. and M.Sc. degrees in electrical engineering from the Federal University of Pernambuco, Recife, Brazil, in 1984 and 1992, respectively, and the Ph.D. degree in electrical engineering from the Federal University of Minas Gerais, Belo Horizonte, Brazil, in 1999. He worked as a visiting scholar at Georgia Institute of Technology - USA, during 1999, and at Alcala University - Spain, from Feb/2008 to Jan/2009. Since 1993, he has been with the Department of Electrical Engineering, Federal University of Pernambuco, where he is currently a Professor of Electrical Engineering. His research interests include power electronics, renewable energy systems, power quality and grid synchronization methods.

Pedro Rodriguez received the B.S. degree in electrical engineering from the University of Granada, Granada, Spain, in 1989, and the M.S. and Ph.D. degrees in electrical engineering from the Technical University of Catalonia (UPC), Barcelona, Spain, in 1994 and 2004, respectively. He was an Assistant Professor in 1990 and an Associate Professor in 1993 with UPC. He was a Researcher with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, and the Institute of Energy Technology, Aalborg University, Aalborg, Denmark, in 2005 and 2006, respectively. He is currently the Head of the Research Group on renewable electrical energy systems with the Department of Electrical Engineering, UPC. He has coauthored about 100 papers in technical journals and conferences. He is the holder of five patents. His research interests include integration of distributed energy systems, power conditioning, and control of power converters.