

# DESIGN OF MINIMUM VOLUME EMC INPUT FILTERS FOR AN ULTRA COMPACT THREE-PHASE PWM RECTIFIER

Marcelo L. Heldwein\* and Johann W. Kolar\*\*

\* Federal University of Santa Catarina - EEL/INEP - www.inep.ufsc.br - Phone:+55-48-3721-9204

\*\* Swiss Federal Institute of Technology (ETH) Zurich - PES - www.pes.ee.ethz.ch

e-mail: heldwein@inep.ufsc.br, kolar@lem.ee.ethz.ch

**Abstract** - A design procedure is proposed for the electromagnetic compatibility (EMC) filters to be included in a three-phase/-level PWM rectifier unit in order to fulfill EMC requirements related to conducted emissions. An analytical volumetric optimization is performed considering constraints given by electrical safety, power factor and damping of resonances. The procedure avoids the necessity of applying numerical optimization allowing the analytical calculation of the total filter volume as function of rated power and switching frequency. The experimental verification of the proposed procedure is presented through conducted emissions (CE) measurements in the designed system.

**Keywords** - Three-phase filters, line filters, three-phase rectifier, conducted emissions.

## I. INTRODUCTION

The demands for higher system compactness have moved Power Electronics research toward the limits of available circuit topologies, materials, components, modulation schemes and control strategies [1, 2]. Increasing switching frequencies, newly developed materials and high performance cooling systems have allowed the miniaturization of the power converters, which consequently present electromagnetic field spectra of higher frequencies confined to smaller spaces [2–4], where one component notably influences the other if attention is not put on their physical disposition. As electromagnetic compatibility (EMC) must obviously be guaranteed inside the system and within its environment [5], electromagnetic emissions control strategies should be employed. For the reduction of conducted emissions (CE), filters have been designed and applied as an interface between the electrical power grid and the power electronics converters. For high performance three-phase rectifier systems, these input filters are typically designed based on passive components, inductors and capacitors along with resistors providing passive damping [6, 7]. These passive filters are responsible for a significant part of the power system's volume and many efforts have been made in order to improve the performance of filter components and to develop

filter topologies allowing for volume, size and costs reduction. There, multi-stage LC filters lead to more compact filters and sometimes cheaper than single-stage ones [8].

To contribute on this subject a design procedure is proposed, which allows for efficient designing compact EMC input filters for a three-phase/-level PWM rectifier, which is employed as a power factor correction (PFC) front-end converter in telecommunication power supplies. The converter power circuits are shown in Figure 1 [9, 10], where the thyristors have the function to provide the pre-charge of the dc-link capacitors. This rectifier has an output power of 10 kW, power density of 8 kW/dm<sup>3</sup>, switching frequency  $f_p = 400$  kHz, output voltage  $U_o = 760$  V, input voltage  $U_{N1} = 230$  V and is forced air-cooled. The EMC filter is designed to fulfill EMC requirements, where an attenuation specification, based on the estimated CE levels of the rectifier, is calculated. Furthermore, the filters are designed taking into account the limits for CE specified for Class B information technology (IT) equipments as in CISPR 22. The aim is that the designed filters are of minimum volume, present the required attenuation characteristics for the frequency range of interest and include passive damping networks, leading to reasonable efforts for the control design.

The proposed procedure has its emphasis on the minimization of the total filter volume through analytical considerations, avoiding the necessity of numerical optimization calculations [11, 12]. The design of the filters is then split into two tasks, common mode (CM) and dif-

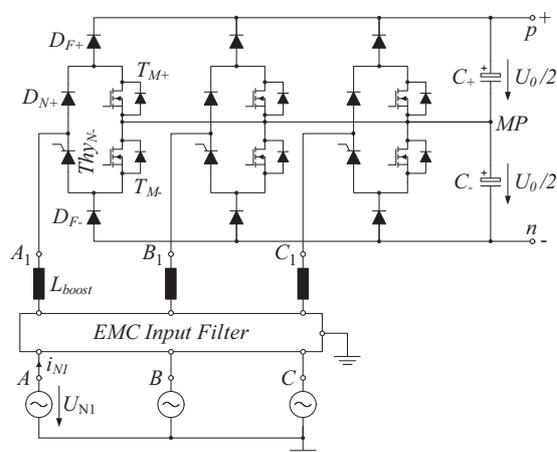


Fig. 1. Circuit schematic of a three-phase, six-switch, three-level rectifier topology used to implement a 10 kW PWM rectifier.

Manuscript received on 15/12/2008. Revised on 26/04/2009.

Accepted by recommendation of the Editor Fernando L. M. Antunes..

ferential mode (DM) filter designs. These tasks are performed before a prototype is built, based on simplified frequency spectra and numerical simulation results of the rectifier and different equivalent circuits for each of the noise modes.

Being the proposed procedure based on analytical equations, a study about the influence of the switching frequency and the parasitic capacitances on the total filter volume is possible. Such study is performed for the rectifier under consideration. The results show the impact of the EMC filter volume in the achievable power density.

This paper is structured as follows. Section II presents the requirements for the filter design along with design assumptions and the input data, namely the frequency spectra of interest and the characteristics of the boost inductors. The DM filter design procedure is presented in Section III, where the assumptions used in the design and the detailed choice of components are given. The definition of the CM filter design is shown in Section IV, with emphasis in the selection of materials and components. Section V illustrates the experimental results achieved for the three-phase rectifier by presenting the final filter structure and CE measurements according to CISPR 22. Finally, conclusions are presented, showing the necessity of further improving CE DM filtering techniques, since power densities of  $50 \text{ kW/dm}^3$  are to be expected in the next years [2] bringing even tougher demands for input filters.

## II. EQUIVALENT CIRCUITS AND REQUIREMENTS

The design procedure starts by defining equivalent circuits used to evaluate CM and DM noise sources and to design appropriate filtering circuits. As the prime objective of the filtering circuits is to reduce emissions at frequencies typically lower than 1 MHz, the definition of very accurate models is not mandatory as long as safe margins are respected. This is because including higher order parasitics, such as magnetic and capacitive couplings among components and printed circuit board (PCB) impedances, strongly increases the modeling effort and does not present relevant effect the circuits at such frequencies. The uncertainties in obtaining very precise simulation models, which include most of the parasitic effects observed in a prototype, also supports this practice. These parasitic impedances are critical for the filter layout and components construction, but are not essential for the input filter design. For these reasons, the circuits presented in Figure 2 are employed in this work, where the voltages  $u_{CM}$ ,  $u_{DM}$ , the inductors  $L_{boost}$  and the capacitance  $C_g$  models the power converter CM and DM noise source circuits.

Capacitance  $C_g$  is a lumped representation of all stray capacitances from the power circuit and load to the protective earth (PE). Not considering load and assuming that the heatsink is bonded to PE,  $C_g$  represents mainly the capacitances from the semiconductors to the heatsink. Typically, impedance  $C_g$  is distributed and presents resistive and inductive portions. Thus, one capacitor at the output of the rectifier represents worst-case except from strong resonances, which are possible at higher frequen-

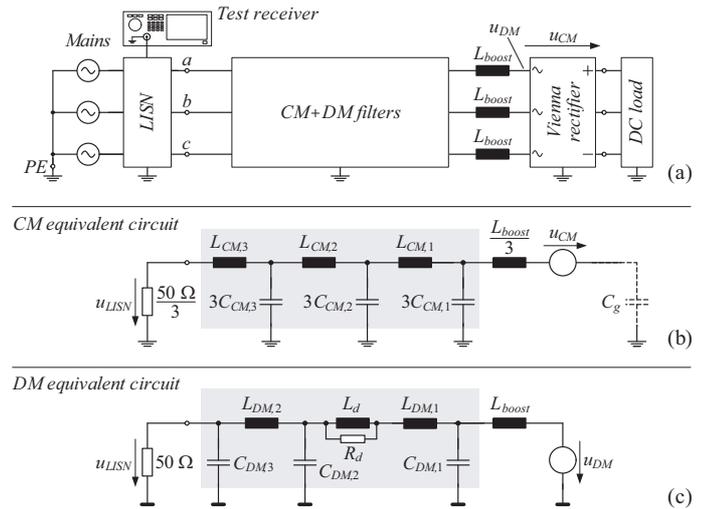


Fig. 2. Standard test setup for conducted emission and simplified equivalent circuits for differential mode. The employed DM and CM filter topologies are also shown.

cies. The maximum value calculated for the capacitance values from the power semiconductors is around 300 pF, typical capacitances from test loads are in the range 200 pF to 2 nF. The value used for the design is  $C_g = 2 \text{ nF}$ . Higher capacitances between load and PE are not specifically considered, since a CM choke can be used at the DC-link terminals limiting the influence of any DC load. Inductors  $L_{boost}$  model the input inductors of the rectifier, which influence CM and DM current paths. Impedance measurements of the built inductors show an inductance of approximately  $30 \mu\text{H}$  and a self-resonance frequency around 8.5 MHz.

The design of the filters is performed in the frequency domain, since the required attenuation is defined in terms of frequency and suitable impedance models for the filtering components are at hand for this domain. Therefore, the estimation of frequency spectra for DM and CM voltages and/or currents is required. A simple simulation with ideal devices presenting rise and fall times close to zero and without the inclusion of parasitic elements is able to provide spectra which are conservative, except at the frequencies close to the characteristic frequencies related to the rise and fall times due to over-voltages and oscillations. Another point which can be neglected in this simulation is the inclusion of the line impedance stabilization network (LISN) circuits, once the voltage spectra do not sensibly change. At last, the circuit is considered to be perfectly balanced. The simulation circuit can be as in Figure 1 except that the EMC filter is removed and the switches are replaced by ideal ones. For the considered power converter, the boost inductors are included in the simulation as ideal inductors, but are also seen as part of the input filters. The spectrum of the input currents change with the inclusion of the other filter components and, for that reason, the input currents spectra are not used for the design of the filters.

For the CM design the relevant spectrum is of the voltage between the DC-link mid-point  $MP$  and the terminals  $A_1$ ,  $B_1$  and  $C_1$  (cf. Figure 1) with the CM voltage  $u_{CM}$  given by

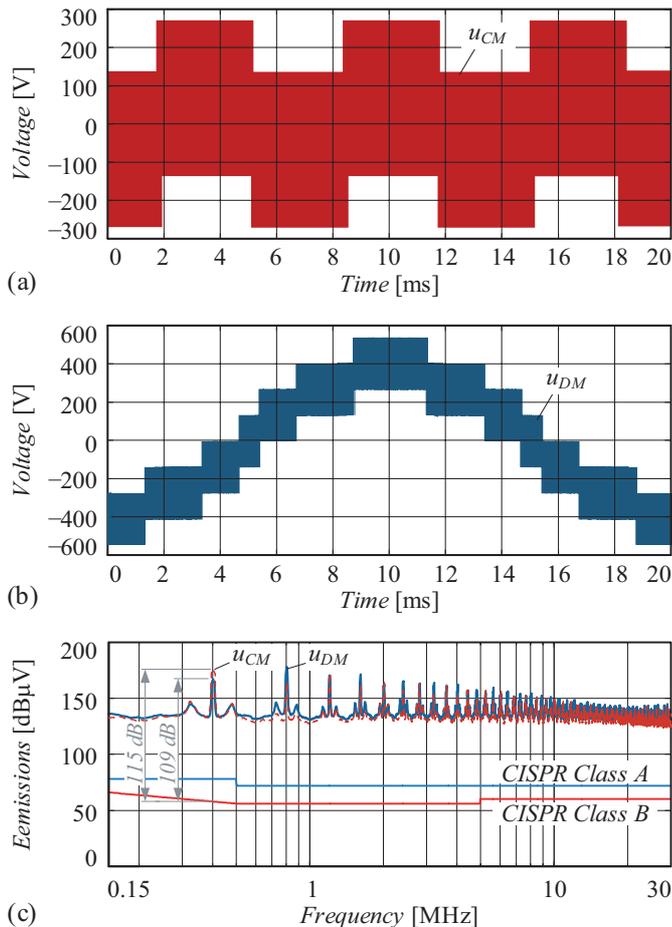


Fig. 3. Waveforms and spectra from the rectifiers' simulation results: (a) Time behavior of the CM voltage  $u_{CM}$ ; (b) Time behavior of one of the DM voltages  $u_{DM}$ ; (c) Conducted emissions predicted spectra for both voltages for the worst case QP detection (linear sum of the harmonic inside the resolution bandwidth [13]).

$$u_{CM} = u_{MP} - \frac{u_{A1} + u_{B1} + u_{C1}}{3}. \quad (1)$$

Considering symmetrical spectra for the three phases, the DM filter spectrum of interest is one of the DM voltages at terminals  $A_1$ ,  $B_1$  and  $C_1$ . The DM voltage  $u_{DM}$  is taken for phase A as

$$u_{DM} = \frac{2}{3} \cdot u_{A1} - \frac{1}{3} \cdot u_{B1} - \frac{1}{3} \cdot u_{C1}. \quad (2)$$

These spectra are compared to the limits at the frequency of interest  $f_{int}$  which is 150 kHz for switching frequencies lower than 150 kHz or the switching frequency itself for higher frequencies. The 150 kHz frequency is the lower frequency of interest for CE measurement according to CISPR 22 [14]. This leads to the required attenuation,  $Att_{req}$ , at the frequency of interest

$$Att_{req}(f_{int}) = 20 \cdot \log \left[ \frac{U_{CM/DM}(f_{int})}{1 \mu V} \right] - Limit(f_{int}). \quad (3)$$

The simulation results are presented in Figure 3 for nominal conditions, which, as required by the CE test

specifications [14], is the worst-case emission condition since the fastest rise and fall times are observed for voltages and currents. Figure 3(a) shows the time behavior of  $u_{CM}$ , which is composed of voltage steps with a value of  $U_o/6$  and presents a strong third harmonic component with respect to the mains frequency. The differential voltage  $u_{DM}$  is plotted in Figure 3(b) and is responsible for the sinusoidal shaping of the input currents with voltage steps of  $U_o/6$  and  $U_o/3$ .

The design must also take into account the specified CE measurement, which in this case is done with two types of detector, the quasi-peak (QP) and average (AVG), presenting both non-linear behavior. For this work, only the QP detector is considered and its behavior is modeled as proposed in [13], by linearizing it. Accordingly, the voltage spectra shown in Figure 3(c) account for a maximum value for the QP measurement, which leads to slightly over dimensioned filters, but as uncertainties, such as components tolerances, are present this is seen as acceptable. It is observed that, at  $f_s = 400$  kHz, both spectra present the worst condition for the filter design task and attenuations of:

$$\begin{aligned} Att_{req,CM} &= -121 \text{ dB @ } f_s = 400 \text{ kHz} \\ Att_{req,DM} &= -115 \text{ dB @ } f_s = 400 \text{ kHz} \end{aligned} \quad (4)$$

are required in order to fulfill CISPR 22 Class B requirements with a 6 dB margin.

### III. DM FILTER DESIGN

The DM filter design is based on the simplified models presented in section II, where equivalent circuits are defined and used to evaluate CM and DM noise sources. The filter topology used for the DM design is shown as a single-phase equivalent in Figure 2. Three-stages are chosen based on power levels and attenuation requirements [8].

The inclusion of the filter generates a displacement in the input currents. Assuming that the rectifier presents resistive behavior and that the inductors are low impedances at the line frequency, at light load the capacitive currents drained by the capacitors generate leading currents in the mains and a limit for the displacement angle constrains the maximum capacitance value. In this work, the maximum input current displacement angle is set to  $\Phi_{in,max} = 5^\circ$  for an output power of 10%, equivalent to a power factor higher than 0.995, leading to a maximum capacitance of  $C_{max} = 5.3 \mu F$ .

On the other hand, capacitors  $C_{DM,1}$  limit the voltage ripple at the input of the converter and a minimum amount of capacitance is required in order to maintain a voltage source characteristic and, thus, the proper operation of the PWM converter. For this reason, the allowable voltage ripple at the input of the power converter is limited to  $\Delta U_{N1,max} \leq 5\%$  of the peak rated phase voltage. The input capacitors  $C_{DM,1}$  can be calculated with the approximation,

$$C_{DM,1} \geq \frac{\Delta I_{N1,max}}{8 \cdot f_s \cdot \Delta U_{N1,max}}, \quad (5)$$

where  $\Delta I_{N1,max}$  is the maximum current ripple in the

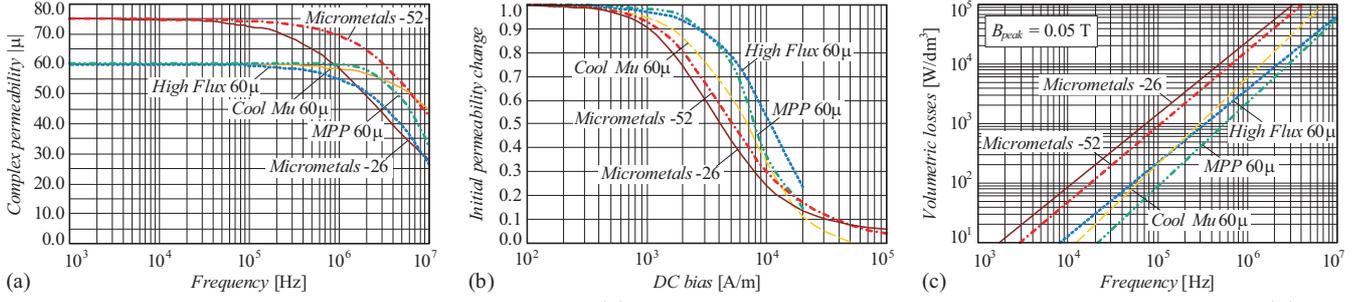


Fig. 4. Properties of core materials for DM inductors: (a) Magnitude of the complex permeability versus frequency; (b) Per unit change in permeability in dependency of the DC bias; (c) Volumetric losses in dependency of frequency for a peak flux density of 50 mT.

boost inductors. Assuming,  $\Delta I_{N1,max} = 0.25(\sqrt{2} \cdot I_{N1}) \cong 5.3$  A,  $\Delta U_{N1,max} = 0.02(\sqrt{2} \cdot U_{N1}) \cong 6.5$  V, and  $f_s = 400$  kHz, the minimum value for the input capacitors is  $C_{DM,1} \geq 260$  nF.

Minimum inductance for the boost inductors is required for the normal operation of the rectifier. For this design the allowable switching frequency ripple is  $i_{boost,max} = 25\%$  of the peak input current  $I_{N1,peak}$ . High frequency losses can not be neglected and the design aims in minimizing overall losses. Optimization has been performed in [15], however it is not within the scope of this work. Nevertheless, the boost inductors can be designed for,

$$L_{boost} \geq \frac{0.7 \cdot U_o / 2}{6 \cdot f_s \cdot \Delta I_{N1,max}} \cong 23 \mu\text{H}. \quad (6)$$

The DM currents are composed of a large component at the mains frequency and a relatively small high frequency ripple due to the attenuation given by the boost inductors and capacitors  $C_{DM,1}$ . For this reason, the cross sectional area of the core  $A_e$  is determined by saturation and not by core losses. Furthermore, the high frequency losses in the winding are also comparatively small and can be neglected. The other parameter that defines the core is the required winding area  $A_w$ .

The filter inductance  $L_{DM,i}$  and rated current are related to the size of the inductor  $A_e A_w$  (area product of a core) by,

$$L_{DM,i} \cdot I_{N1,peak} \cdot I_{N1,rms} = k_w \cdot J_{max} \cdot B_{peak} \cdot A_e \cdot A_w. \quad (7)$$

The volume of the filter inductor  $V_L$  is calculated with,

$$V_L = k_{geo} \cdot (A_e \cdot A_w)^{\alpha_{geo}}. \quad (8)$$

There, the parameters  $k_{geo}$  and  $\alpha_{geo}$  account for the geometry of the core (toroidal, planar, etc). Assuming that a dimension grows proportionally with the other ones,  $\alpha_{geo}$  is usually taken as 3/4.

To choose an appropriate material for the comparison of core materials is done in Figure 4 for different types of iron powder materials. From the comparison, material High Flux is chosen, with a initial permeability of  $\mu_r = 160$ . Furthermore, the volumetric coefficient for the material High Flux with  $\mu_r = 160$  is given by,  $k_L \cong 3.95 \cdot 10^{-3} \frac{\text{m}^3}{\text{H} \cdot \text{A}^2}$ .

The volume of the capacitors to be used in the filters is approximated by a curve generated by Minimum Square fitting of the volumes calculated for commercially available X2 type capacitors [16]. The approximation curves along with the calculated values for discrete capacitors also suggest a volume dependency with the stored energy. Surface mount devices are chosen, which are rated as X2 capacitors [16], which volumetric coefficient is,  $k_{C,X2,cer} \cong 16.4 \cdot 10^{-6} \frac{\text{m}^3}{\text{F} \cdot \text{V}^2}$ .

Assuming that the volume of the components is directly related to their stored energy, the volumetric coefficients for inductors  $k_L$  and capacitors  $k_C$  are defined as in

$$Vol_L = k_L \cdot L_{DM,i} \cdot I_{N1}^2 \quad (9)$$

$$Vol_C = k_{C,X2,cer} \cdot C_{DM,i} \cdot U_{N1}^2. \quad (10)$$

The minimization of the volume can then be performed with the following procedure.

#### A. Analytical Volume Minimization of DM Filters

Two equations define the volume minimization problem, the attenuation at the frequency of interest  $f_{int}$ , that represents the main constraint, and the filter volume, which shall be minimized.

An asymptotic approximation of the attenuation  $Att$ , for frequencies much higher than the corner frequency, is used,

$$\frac{1}{Att(f_{int})} \cong (2\pi \cdot f_{int})^6 \cdot L_{boost} \cdot \prod_{i=1}^2 L_{DM,i} \cdot \prod_{i=1}^3 C_{DM,i}. \quad (11)$$

What is left to derive is the individual values for the components  $L_{DM,i}$  and  $C_{DM,i}$ . As seen in the Appendix, the equal distribution on inductors and capacitors lead to the smallest total values. Thus, only two variables are left to minimize the volume  $L_{DM}$  and  $C_{DM}$ . The required attenuation  $Att_{req}$  equation (cf. (11)) is simplified to,

$$\frac{1}{Att_{req}} \cong (2\pi \cdot f_{int})^6 \cdot L_{boost} \cdot L_{DM}^2 \cdot C_{DM}^3. \quad (12)$$

Requirements related to control issues must also be considered and, in order to provide passive damping that cause minimum losses and avoiding oscillations, RL networks are included in the choice of the topologies. Considering a damping network as shown in Figure 5, where

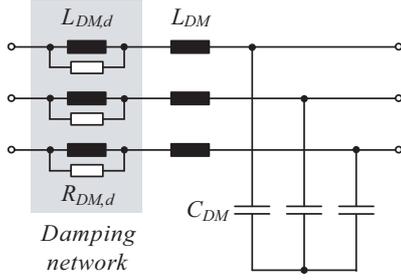


Fig. 5. Three-phase filter stage with damping network.

the inductor  $L_{DM,d}$  of the damping network has the same value as the filtering inductor  $L_{DM}$ , the number of inductors in the first filter stage is doubled and the total volume of the filter  $Vol_{DM}$  is given by,

$$Vol_{DM} = 9 \cdot (Vol_{L_{DM}} + Vol_{C_{DM}}) + 3 \cdot Vol_{L_{boost}}. \quad (13)$$

The solution for a minimal volume is given for,

$$\frac{\partial Vol_{DM}}{\partial C_{DM}} = 0, \quad (14)$$

and the final values for the components are given by,

$$C_{DM} = \frac{I_{N1}}{4\pi f_{int} \cdot U_{N1}} \cdot \sqrt[5]{\frac{36 \cdot k_L^2 \cdot U_{N1}}{\pi f_{int} \cdot L_{boost} \cdot Att_{req} \cdot k_C^2 \cdot I_{N1}}} \quad (15)$$

$$L_{DM} = \frac{U_{N1}}{6\pi f_{int} \cdot I_{N1}} \cdot \sqrt[5]{\frac{36 \cdot k_C^3 \cdot U_{N1}}{\pi f_{int} \cdot L_{boost} \cdot Att_{req} \cdot k_L^3 \cdot I_{N1}}} \quad (16)$$

Thus, minimal volume filters can be designed based on the ratings of the components and the required filter attenuation assuming that parasitic elements do not strongly influence the attenuation at the frequency of interest, which is typically valid. This minimization procedure eliminates the need for a numerical optimization procedure [11, 12], thus simplifying the design of minimum volume EMC filters.

### B. Parallel RL Damping Design

The topology with parallel RL damping network is shown in Figure 5. As for the previous topology, minimum output impedance is required for given attenuation and filter elements [17]. The characteristic resistance  $R_o$  and frequency  $f_o$  are defined in the same way as,

$$R_o = \sqrt{\frac{L_{DM}}{C_{DM}}} \quad (17)$$

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{DM} \cdot C_{DM}}}, \quad (18)$$

and the ratio of the inductors as,

$$n = \frac{L_{DM,d}}{L_{DM}}, \quad (19)$$

it follows that the optimum resistance ratio  $Q_{opt}$  for this topology is,

$$Q_{opt} = \frac{R_{DM,d, optimum}}{R_o} = \frac{1+n}{n} \sqrt{\frac{2 \cdot (1+n) \cdot (4+n)}{(2+n) \cdot (4+3n)}}, \quad (20)$$

so that, for optimum damping the damping resistance is,

$$R_{DM,d} = R_o \cdot \frac{1+n}{n} \cdot \sqrt{\frac{2 \cdot (1+n) \cdot (4+n)}{(2+n) \cdot (4+3n)}}. \quad (21)$$

From this result, the maximum output impedance  $|Z_{out}|_{max}$  is,

$$|Z_{out}|_{max} = R_o \cdot \frac{\sqrt{2 \cdot (1+n) \cdot (2+n)}}{n}, \quad (22)$$

at a frequency  $f_{peak}$  of,

$$f_{peak} = f_o \cdot \sqrt{\frac{2+n}{2 \cdot (1+n)}}. \quad (23)$$

### C. Filter Design

The DM filter design procedure is presented in the block diagram of Figure 6. The diagram shows that the first tasks are to define the main filter components considering the given constraints. This is where the volumetric optimization takes place. The final steps are to design the passive damping network and to deduct the values of the leakage inductance of CM chokes from the required inductance to design the DM inductors. As seen in Figure 6, the maximum amount of capacitance  $C_{max}$  per phase is limited due to the required power factor at light load. From (4), the required attenuation in absolute numbers is  $Att_{req} \cong 1.778 \cdot 10^{-6}$  @  $f_{int} = f_s = 400$  kHz.

The rated current for the inductor is given by,

$$I_{N1} = \frac{P_o}{3 \cdot \eta \cdot U_{N1, min}} = \frac{P_o}{3 \cdot 0.96 \cdot 0.8 \cdot U_{N1}} \cong 18.9 \text{ A}, \quad (24)$$

where  $\eta = 0.96$  is the expected efficiency of the PWM converter and  $U_{N1, min} = 0.8 \cdot U_{N1}$  is the minimum input voltage.

All the required values for the calculation of the components which lead to the minimum DM filter volume are defined and plugging them into (15) and (16) gives  $C_{DM} \cong 2.57 \mu\text{F}$  and  $L_{DM} \cong 2.10 \mu\text{H}$ .

Results for the proposed volume minimization procedure are depicted in Figure 7. It is seen the volume and attenuation surfaces in dependency of the DM inductance  $L_{DM}$  and capacitance  $C_{DM}$ . The surfaces take into consideration a detailed model, with the following estimated parasitic elements: equivalent series resistance (ESR), inductance (ESL), losses and parallel capacitance.

It is seen from that the sum of three DM capacitors  $3 \cdot C_{DM} = 7.71 \mu\text{F}$  is larger than the total maximum capacitance per phase  $C_{max} = 5.3 \mu\text{F}$ . For this reason, the components must be dimensioned for the largest total capacitance per phase. Dividing the total capacitance per

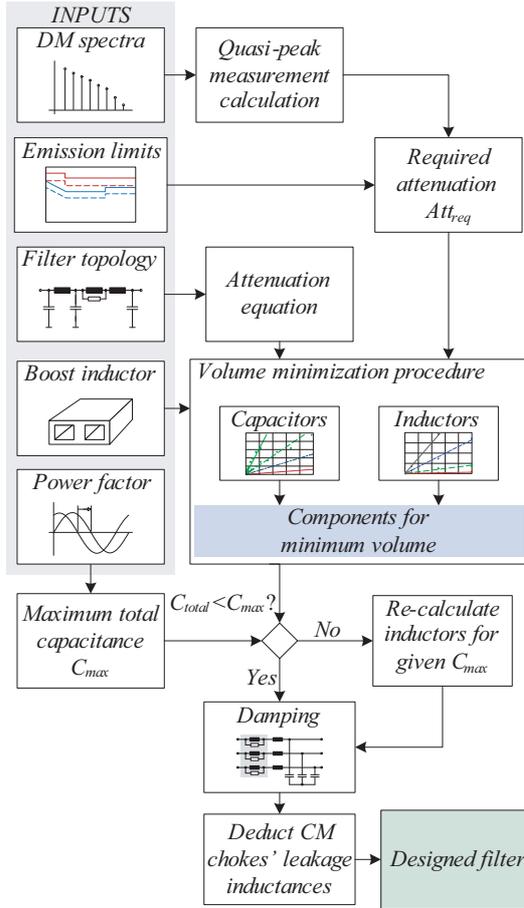


Fig. 6. Flowchart showing the input DM filter design procedure.

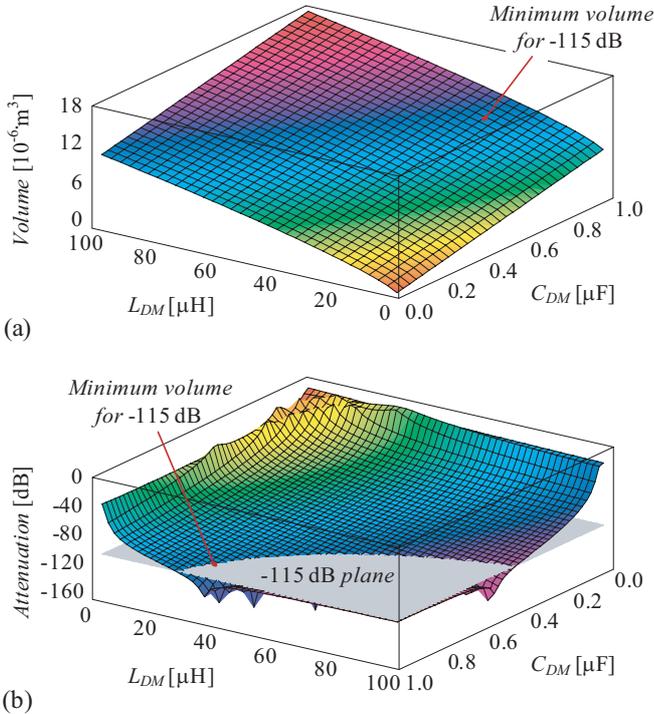


Fig. 7. Volume and attenuation surfaces for the DM filter design with Molypermaloy cores and X2 capacitors. (a) Volume dependence on  $L_{DM}$  and  $C_{DM}$  values; (b) Attenuation at  $f_s = 400$  kHz for  $L_{DM}$  and  $C_{DM}$  values and  $-115$  dB plane (gray). Colors correspond to colors in (a).

phase by three and re-calculating  $L_{DM}$  for the required attenuation, leads to,

$$C_{DM} \cong 1.77 \mu\text{F} \text{ and } L_{DM} \cong 3.67 \mu\text{H}, \quad (25)$$

which are employed for the implementation of the DM filter. As the obtained value for the DM capacitance is not commonly available, a different distribution of the capacitors has been employed in practice. The first filter stage has a total capacitance of  $2.0 \mu\text{F}$ , while the other two stages present  $1.5 \mu\text{F}$ . The DM inductors have the specification shown in Table I.

TABLE I  
Specifications for the DM inductors  $L_{DM,i}$ .

Parameter	Value
Core manufacturer	Magnetics
Core material	High Flux
Core part number	58928-A2
Magnet wire diameter	1.5 mm
Number of turns	13

#### IV. CM FILTER DESIGN

The first task in the CM filter design is to choose an appropriate filter topology. These filters are typically built with inductors and capacitors in a low-pass arrangement, which can have many stages and different configurations. Multi-stage filters have the potential to lower the total filter size and costs. Reference [8] defines the conditions and requirements at which each topology presents an advantage. For the case at hand, a three-stage topology is presented in Figure 2 in its single-phase equivalent.

Equipment safety regulations [18] play an important role, since restrain the allowable earth leakage current; define requirements for capacitors between an input line and PE, and; define insulation requirements for CM inductors and filter construction. Earth leakage current  $I_{PE,rms,max}$  is typically limited to 3.5 mA, even for the case where one of the phases is lost. Thus, the total capacitance  $C_{CM,sum} = \sum C_{CM,i}$ , where  $i = 1 \dots 3$ , between any of the input phases and the PE is bounded to a maximum of approximately,

$$C_{CM,sum} \leq \frac{I_{PE,rms,max}}{1.1 \cdot U_{N1,max} \cdot 2\pi \cdot 50 \text{ Hz}} \cong 44 \text{ nF} \quad (26)$$

Safety also requires Y2 rated capacitors. Due to these restrictions a series of Y2 ceramic capacitors [16] is chosen, which presents a maximum capacitance of 4.7 nF per SMD package, leading to compact construction and low parasitics. Since other capacitances are present in the circuit (arrestors, stray capacitances, etc) and values present tolerances, some margin is provided so that  $C_{CM,sum} = 7 \cdot 4.7 \text{ nF} = 32.9 \text{ nF}$ , to be divided in the filter stages.

The most important elements of the CM filter are the coupled CM inductors [19]. These are designed based on

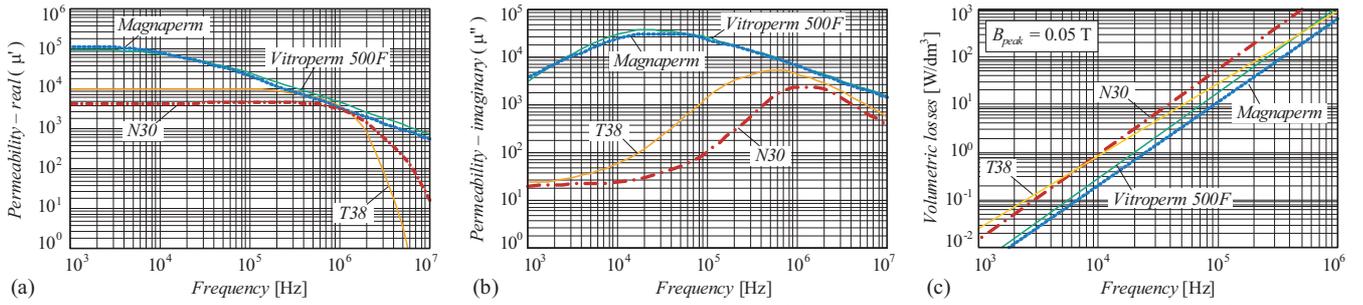


Fig. 8. Properties of different core materials suitable for CM inductors: (a) Real part of complex permeability; (b) Imaginary part of complex permeability; (c) Volumetric losses in dependency of frequency for a peak flux density of 50 mT.

their required impedance at a given frequency because core magnetic materials present a non-constant complex permeability with frequency. An imaginary part  $\mu''$  increases the total impedance and the CM choke behaves as a series RL connection. The proper choice of core materials leads to compact and effective inductors, with reduced parasitics. The main characteristics for CM reduction for some popular and high performance magnetic materials are shown in Figure 8. Two types of ferrite (N30 and T38), a nanocrystalline (VITROPERM 500F) and an amorphous material (MAGNAPERM) are compared. It is observed that the real part of the permeability of all materials is similar in the 0.2 to 2 MHz range, but the non-ferrite materials present higher permeabilities for other frequencies. The imaginary part is lower for the ferrites. Even core losses are higher for these ferrites. Core losses are usually not considered when designing CM chokes, but when high switching frequencies (400 kHz for this design) are employed, this shall be considered. The maximum flux density are  $B_{sat,VITROPERM} = 1.2$  T,  $B_{sat,MAGNAPERM} = 0.6$  T, while it is lower than 0.3 T for the ferrites. This comparison shows that CM inductors can be smaller by applying materials with high permeability and saturation point. Given these reasons, VITROPERM 500 F is chosen for the CM chokes. This material presents good thermal stability as well. Employing core materials with higher permeability reduces the risk of saturation, however stray inductances which are typically employed as DM inductances are reduced causing the need to increase DM filters.

The design of the inductors is based on the following assumptions:

- possible asymmetries, parasitic capacitances and the effect of the tolerances are neglected;
- ambient temperature equals 45°C and the maximum temperature rise is 60°C;
- a single winding layer is allowed in order to reduce parasitics;
- iterative choice of the maximum flux density  $B_{max}$  and current density  $J_{max}$  is performed;
- discrete values determined by the limited choice of cores and wire diameters are approximated by continuous functions.

Based on these design guidelines, a series of inductor designs is conducted for different frequencies and current ratings. The results are summarized in Figure 9. Figure 9 presents the used maximum current density  $J_{max}$

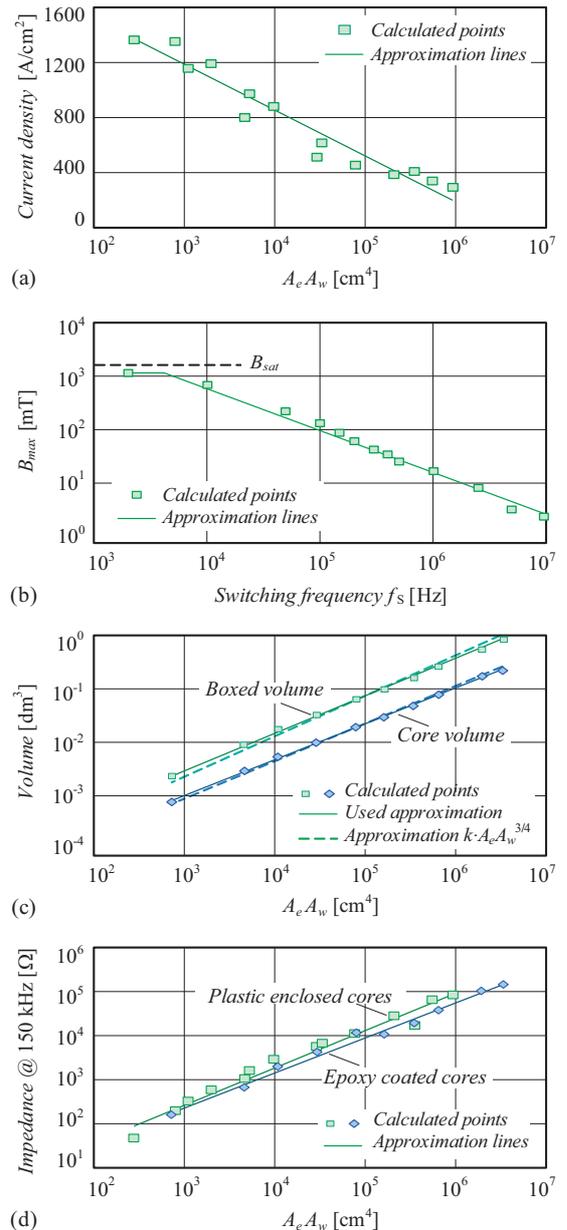


Fig. 9. Curves for core material VAC VITROPERM 500F: (a) Dependency of an inductor's boxed and core volume on area product  $A_e A_w$  of the used material. (b) Impedance at 150 kHz and 15 A RMS as a function of area product for two core types namely, epoxy coated cores and cores with a plastic enclosure. (c) Maximum current density as a function of the area product. (d) Maximum flux density versus switching frequency.

(Figure 9(a)) and flux density  $B_{\max}$  (Figure 9(b)) as functions of the core product of areas  $A_e A_w$  and switching frequency  $f_s$ , respectively. In Figure 9(c) the dependency of the volume of an inductor to its product of areas  $A_e A_w$  is depicted along with the core volume. This dependency is usually considered with a power of  $3/4$ , but for the analyzed case a lower factor is used leading to closer approximations. Finally, based on these considerations and on the material's complex permeability curves an equation for the maximum achievable CM choke impedance  $Z_{choke}$  for a given product of areas and switching frequency is empirically derived [20],

$$Z_{choke}(f_{\text{int}}) \cong 10^{2.243 - 2 \cdot \log(I_{N1}) + 0.181 \cdot \log(|f_{\text{int}} \cdot \mu(f_{\text{int}})|) \log(A_e \cdot A_w)} \quad (27)$$

Equation (27) presents an R-squared value higher than 0.939 for frequencies in the range  $150 \text{ kHz} < f_{\text{int}} < 10 \text{ MHz}$ , when compared with the calculated values. Solving (6) for the product of areas leads to the core size and its volume can be calculated with the help of the curves depicted in Figure 9(d). This approach is useful in an optimization procedure where a minimum total volume for the filters and power converter are searched.

The value of the CM inductors among the different filter stages can, in principle, be performed in the same way as the DM inductors (cf. section VI). That means that equal inductors are to be placed in all filter stages so that the total inductance is reduced and attenuation is maximized. Following this procedure and examining Figure 2 leads to three CM inductors of equal value, which impedance at the frequency of interest is required to be

$$Z_{choke,des} \cong 1.38 \text{ k}\Omega @ f_{\text{int}} = 400 \text{ kHz}. \quad (28)$$

The attenuation equation for this circuit is extremely long and for the sake of clarity it is omitted here. However, it can be numerically solved for finding this required impedance employing equal filter capacitors and assuming a purely resistive impedance for the equal inductors.

The CM inductor which is at the input of the rectifier  $L_{CM,1}$  must withstand a higher CM voltage and for this reason it was required a larger core for this inductor. The CM voltage across this inductor can be computed from the equivalent circuit shown in Figure 10. The boost inductor typically presents an impedance that is much lower than  $L_{CM,1}$  and  $L_{CM,1}$  has an impedance which is much higher than the capacitor  $3C_{CM,1}$ . For these reasons, a simplified expression can be employed, which only takes the capacitances into account, as in,

$$U_{L1} \cong U_{CM} \cdot \frac{C_g}{C_g + 3 \cdot C_{CM,1}}. \quad (29)$$

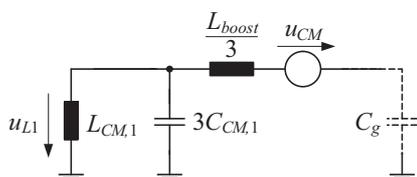


Fig. 10. Simplified circuit for computing the CM voltage across  $L_{CM,1}$ .

**TABLE II**  
Specifications for the CM inductor  $L_{CM,1}$ .

Parameter	Value
Core part number	T6000-6-L2020-W423
Core dimensions [mm]	OD: 32.7 / ID: 17.7 / H: 12.5
Magnet wire diameter	2.0 mm
Number of turns	$3 \times 8$
Impedance @ 400 kHz	1481 $\Omega$

**TABLE III**  
CM inductors  $L_{CM,2}$  and  $L_{CM,3}$ .

Parameter	Value
Core part number	T6000-6-L2025-W380
Core dimensions [mm]	OD: 27.8 / ID: 13.7 / H: 12.7
Magnet wire diameter	1.8 mm
Number of turns	$3 \times 7$
Number of layers	1
Impedance @ 400 kHz	1239 $\Omega$

For the case at hand, the peak voltage at the switching frequency is calculated as  $U_{CM} \cong 136.6 \text{ V} @ f_{\text{int}} = 400 \text{ kHz}$ . A total capacitance to ground is assumed to be 2 nF. Capacitance  $C_{CM,1}$  is taken as a third of the maximum capacitance per phase, so that,  $C_{CM,1} = \frac{C_{CM,sum}}{3} = 14.6 \text{ nF}$ .

Thus, the expected peak CM voltage at the switching frequency is  $U_{L1} \cong 5.94 \text{ V} @ f_{\text{int}} = 400 \text{ kHz}$ , which is used for computing the flux density at the designed inductor as well as core losses.

Using the calculated required impedance  $Z_{des}$  and the peak CM voltage  $U_{L1}$ , the design algorithm leads to the inductor specification as shown in Table II

As seen in Table II the achieved impedance of  $L_{CM,1}$  is higher than  $Z_{des}$ . With this, the inductance of the other two inductors can be reduced. The CM voltage across these inductors is very low and can be neglected. With this, Table III shows the design data for  $L_{CM,2}$  and  $L_{CM,3}$ .

## V. EXPERIMENTAL VERIFICATION

The rectifier's construction views are shown in Figure 11. The rectifier is designed for compactness. Thus, trade-offs among thermal, electrical, EMC and mechanical functions are required. The filter layout follows design rules to reduce interaction within filter elements and presents a straight line forward current flow. The current flows from the input terminals through the EMC filter, the current sensors and boost inductors, which links it to capacitor board. From this board the current flows through the power module into the output capacitors. In the tested version of this system, the input filter has been placed in a separate printed circuit board in order to reduce the coupling to the power circuits.

The final filter circuit is shown in Figure 12, where the CM filter is also integrated in the structure. Interesting information is that the final boxed volume of the

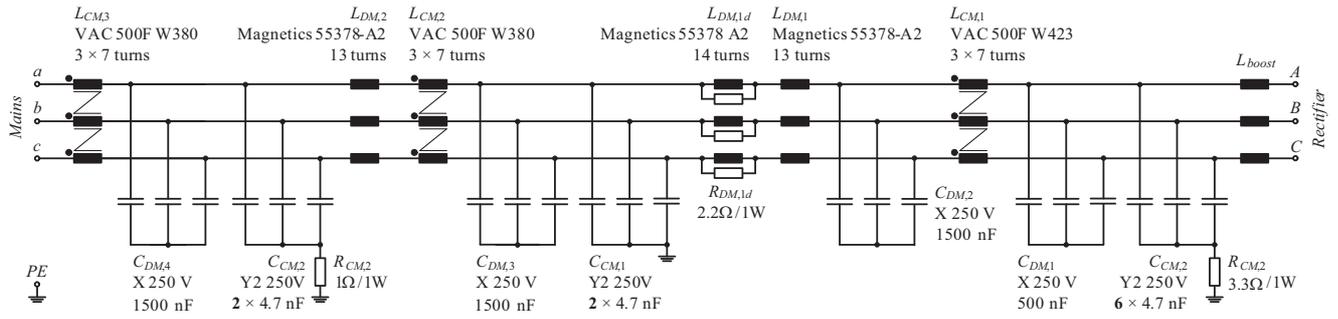


Fig. 12. Complete circuit schematic for the designed filter with the specifications of the main components.

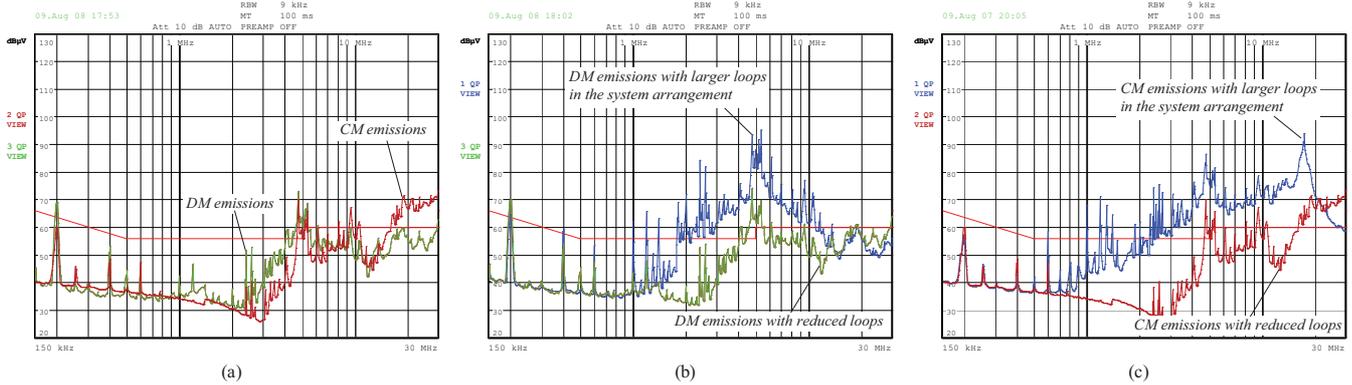


Fig. 13. Measured CM and DM conducted emissions.

complete filter is approximately 2.4 times larger than the sum of all individual components, meaning that interconnections, forced air-cooled system and PCB account for nearly 60% of the employed space. That leaves room for improvements through research on inter-components coupling reduction.

Due to thermal and digital processing restrictions, the switching frequency needed to be reduced to  $f_s = 200$  kHz. This will be increased in a redesign of the system.

Experimental results from conducted emissions (QP) measurements, according to CISPR 22, are shown in Figure 13. A three-phase noise separator [13] has been used in order to allow the separate evaluation of DM and CM. Figure 13(a) depicts the measured emission levels for CM

and DM. For the DM emissions, the first harmonic is below the designed point (400 kHz) and, thus larger than predicted. These results are obtained in an open system, where no special shield was used. This explains for the worsening of the performance for higher frequencies. Nevertheless, the filter design procedure proves efficient since the components are designed for the switching frequency.

A comparison of the influence of cabling and grounding configurations in the emissions is presented in Figure 13(b) and Figure 13(c). DM emissions are shown in Figure 13(b) for two different system configurations. CM emissions are presented in Figure 13(c). It is seen that, for the same components and boards, the influence of the geometrical configuration of the interconnections and associated loops, is enormous. These effects can not be accounted for before hand in the proposed modeling, since they depend upon the 3-D geometry HF effects. This is beyond the scope of this work, however references [21–23] give a good overview on the subject. Furthermore, electromagnetic solvers are being researched [24, 25] as tools to be employed still in the design phase of a power converter system.

## VI. CONCLUSIONS

This work proposes a design procedure for the EMC filters to be employed with a three-phase rectifier unit in order to fulfill CISPR 22 Class B requirements related to conducted emissions. The design procedure is explained; where a volumetric optimization is carried out taking into consideration different aspects related to the subject, such as electrical safety, power factor and damping of resonances. The presented procedure avoids the necessity of using numerical optimization routines and allows for the

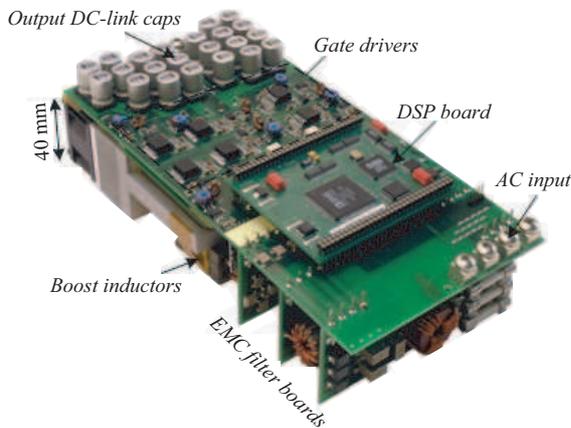


Fig. 11. Top view on rectifier with the EMC filter DSP board, gate drivers and electrolytic dc output capacitors.

analytical calculation of the total filter volume as function of the rated power and switching frequency, therefore helping in the early determination of the optimum switching frequency for a given rectifier specification. It is also possible to extend the proposed procedure to single-phase applications considering the given symmetries adopted in this work. The experimental verification of the proposed filter design procedure is shown, where it is identified that the system physical configuration has a large influence in the final emissions performance. These effects shall be target for future research, so that computer aided design and virtual prototyping can be fully implemented.

#### APPENDIX — Minimum Inductance for a Given Attenuation

Starting from a general filter as shown in Figure 14, a relation between the components can be found as in the following.

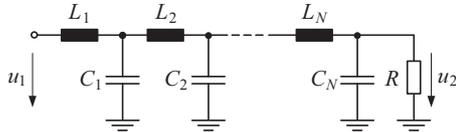


Fig. 14. Multi-stage LC filter configuration.

The attenuation for the multi-stage LC filter of Figure 14 is approximated for frequencies much higher than the cutoff frequency of the filter by,

$$Att(\omega)|_{\text{HF}} = \left| \frac{U_2(\omega)}{U_1(\omega)} \right| = \frac{1}{\omega^{2N} \cdot \prod_{j=1}^N L_j \cdot \prod_{j=1}^N C_j}. \quad (30)$$

Assuming that the capacitors  $C_j$  are known and that a given attenuation  $Att_{req}$  is required at a frequency  $\omega_{req}$ , (30) can be rewritten,

$$\frac{1}{Att_{req} \cdot K_g} = \prod_{j=1}^N L_j, \quad (31)$$

where,

$$K_g = \omega_{req}^{2N} \cdot \prod_{j=1}^N C_j. \quad (32)$$

A maximum inductance  $L_{max}$  is defined as the sum of all inductors  $L_j$ ,

$$L_{max} = \sum_{j=1}^N L_j. \quad (33)$$

Supposing that all inductors have the same value, then,

$$L_j = \frac{L_{max}}{N}, \quad (34)$$

and the attenuation is given by,

$$\frac{1}{Att_{req} \cdot K_g} = \left( \frac{L_{max}}{N} \right)^N. \quad (35)$$

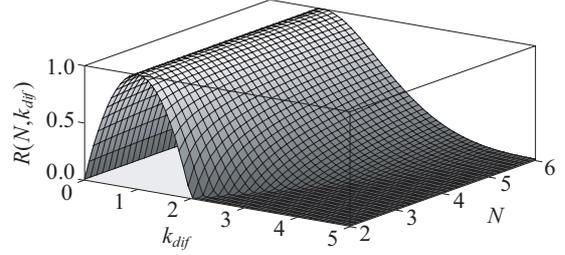


Fig. 15. Ratio  $R(N, k_{dif})$  between the attenuation obtainable with all inductors presenting equal inductance values and the attenuation for which a single inductor presents a different inductance value.

Having the premise that one of the inductors has a different value  $L_{dif}$ , defined by,

$$L_{dif} = \frac{k_{dif} \cdot L_{max}}{N} \quad (36)$$

$$L_j = L_{max} \cdot \frac{N - k_{dif}}{N \cdot (N - 1)}, \quad (37)$$

with  $k_{dif} \geq 0$ .

The attenuation equation for this new condition is,

$$\frac{1}{Att_{req} \cdot K_g} = \frac{k_{dif} \cdot (N - 1)}{N - k_{dif}} \cdot \left( \frac{L_{dif} \cdot (N - k_{dif})}{K \cdot (N - 1)} \right)^N. \quad (38)$$

Dividing (38) by (35) leads to the ratio  $R(N, k_{dif})$  (cf. (39)) between the attenuation obtainable for both situations, which is graphically shown in Figure 15.

$$R(N, k_{dif}) = k_{dif} \cdot \left( \frac{N - k_{dif}}{N - 1} \right)^{N-1}. \quad (39)$$

Differentiating  $R(N, k_{dif})$  with respect to  $k_{dif}$  leads to,

$$\frac{\partial R(N, k_{dif})}{\partial k_{dif}} = -\frac{(N - 1) \cdot (k_{dif} - 1)}{(k_{dif} - N)^2} \cdot \left( \frac{N - k_{dif}}{N - 1} \right)^K. \quad (40)$$

Equating this result to zero leads to the maximum achievable attenuation,

$$\frac{\partial R(N, k_{dif})}{\partial k_{dif}} = 0 \Rightarrow k_{dif, optimum} = 1. \quad (41)$$

As observed in (41),  $k_{dif}$  equal to unity leads to the highest attenuation independent on the number of LC stages. That means that the maximum high frequency attenuation, for a given  $L_{max}$ , is achieved for equal components in all stages, since the structure of (30) is the same for, both, inductances and capacitances. For the lower total inductance, each of the individual inductors have the same value  $L_{DM,i} = L_{DM}$  and this is valid for the capacitors  $C_{DM,i} = C_{DM}$ .

#### Acknowledgment

The authors would like to show their gratitude to the hours spent in the lab by Dr. Simon Round.

## REFERENCES

- [1] F. C. Lee and P. Barbosa, "The state-of-the-art power electronics technologies and future trends," in *IEEE PES Transmission and Distribution Conference and Exposition*, vol. 2, 2001, pp. 1188–1193.
- [2] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "Pwm converter power density barriers," in *Power Conversion Conference - PCC '07*, Nagoya, Japan, 2007, pp. P–9–P–29.
- [3] J. A. Ferreira and J. D. Van Wyk, "Electromagnetic energy propagation in power electronic converters: toward future electromagnetic integration," *Proceedings of the IEEE*, vol. 89, no. 6, pp. 876–889, 2001, 0018-9219.
- [4] Z. Qian, X. Wu, Z. Lu, and M. H. Pong, "Status of electromagnetic compatibility research in power electronics," in *International Power Electronics and Motion Control Conference*, vol. 1, 2000, pp. 46–57 vol.1.
- [5] R. Redl, "Electromagnetic environmental impact of power electronics equipment," *Proceedings of the IEEE*, vol. 89, no. 6, pp. 926–938, 2001, 0018-9219.
- [6] M. J. Nave, *Power Line Filter Design for Switched-Mode Power Supplies*. New York (NY), USA: Van Nostrand Reinhold, 1991.
- [7] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, Mass., USA: Kluwer Academic, 2001.
- [8] A. Nagel and R. W. De Doncker, "Systematic design of emi-filters for power converters," in *Industry Applications Conference*, vol. 4, 2000, pp. 2523–2525 vol.4.
- [9] Y. Zhao, Y. Li, and T. A. Lipo, "Force commutated three level boost type rectifier," in *IEEE Industry Applications Society Annual Meeting*, 1993, pp. 771–777 vol.2.
- [10] P. Karutz, S. D. Round, M. L. Heldwein, and J. W. Kolar, "Ultra compact three-phase pwm rectifier," in *Applied Power Electronics Conference*, 2007, pp. 816–822.
- [11] W. Shen, F. Wang, D. Boroyevich, and Y. Liu, "Definition and acquisition of cm and dm emi noise for general-purpose adjustable speed motor drives," in *IEEE Power Electronics Specialists Conference*, vol. 2, 2004, pp. 1028–1033 Vol.2.
- [12] S. Chandrasekaran, S. Ragon, D. K. Lindner, Z. Gurdal, and D. Boroyevich, "Optimization of an aircraft power distribution subsystem," *AIAA Journal of Aircraft*, vol. 40, no. 1, pp. 16–26, 2003.
- [13] T. Nussbaumer, M. L. Heldwein, and J. W. Kolar, "Differential mode input filter design for a three-phase buck-type pwm rectifier based on modeling of the emc test receiver," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1649–1661, 2006, 0278-0046.
- [14] CISPR, *Information technology equipment - Radio disturbance characteristics - Limits and Methods of Measurement - Publication 22*. Geneve, Switzerland: IEC International Special Committee on Radio Interference - C.I.S.P.R., 1993.
- [15] W. G. Hurley, E. Gath, and J. G. Breslin, "Optimizing the ac resistance of multilayer transformer windings with arbitrary current waveforms," *IEEE Transactions on Power Electronics*, vol. 15, no. 2, pp. 369–376, 2000, 0885-8993.
- [16] Murata, "Chip monolithic ceramic capacitors," 22.08.2007 2007.
- [17] R. W. Erickson, "Optimal single resistors damping of input filters," in *IEEE Applied Power Electronics Conference and Exposition*, vol. 2, 1999, pp. 1073–1079 vol.2.
- [18] IEC, *Safety of Information Technology Equipment - IEC 60950*. Brussels, Belgium: International Electrotechnical Commission - IEC, 1999.
- [19] M. J. Nave, "On modeling the common mode inductor," in *IEEE 1991 International Symposium on Electromagnetic Compatibility*, 1991, pp. 452–457.
- [20] M. L. Heldwein, "Emc filtering of three-phase pwm converters," Ph.D. Thesis, ETH Zurich, 2007.
- [21] N. K. Poon, B. M. H. Pong, C. P. Liu, and C. K. Tse, "Essential coupling path models for non-contact emi in switching power converters using lumped circuit elements," *IEEE Transactions on Power Electronics*, vol. 18, no. 2, pp. 686–695, 2003, 0885-8993.
- [22] S. Wang, F. C. Lee, D. Y. Chen, and W. G. Odenaal, "Effects of parasitic parameters on emi filter performance," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 869–877, 2004, 0885-8993.
- [23] T. C. Neugebauer and D. J. Perreault, "Parasitic capacitance cancellation in filter inductors," *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 282–288, 2006, 0885-8993.
- [24] S. P. Weber, E. Hoene, S. Guttowski, J. John, and H. Reichl, "Predicting parasitics and inductive coupling in emi-filters," in *Applied Power Electronics Conference and Exposition*, 2006, p. 4 pp.
- [25] A. Musing, M. L. Heldwein, T. Friedli, and J. W. Kolar, "Steps towards prediction of conducted emission levels of an rb-igbt indirect matrix converter," in *Power Conversion Conference*, 2007, pp. 1181–1188.

## BIOGRAPHIES

**Marcelo Lobo Heldwein** received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1997 and 1999, respectively, and his Ph.D. degree from the Swiss Federal Institute of Technology (ETH Zurich), Zurich, Switzerland, in 2007.

He is currently working as a Postdoctoral Fellow at the Power Electronics Institute (INEP), Federal University of Santa Catarina (UFSC), Florianópolis, Brazil.

From 1999 to 2001, he was a Research Assistant with the Power Electronics Institute, Federal University of Santa Catarina. From 2001 to 2003, he was an Electrical Design Engineer with Emerson Energy Systems, in São José dos Campos, Brazil and in Stockholm, Sweden.

His research interests include power factor correction techniques, static power converters and electromagnetic compatibility.

Mr. Heldwein is currently a member of the Brazilian Power

Electronic Society (SOBRAEP) and of the IEEE.

**Johann W. Kolar** received his Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria. Since 1984 he has been working as an independent international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel PWM converter topologies, and modulation and control concepts, e.g., the VIENNA Rectifier and the Three-Phase AC-AC Sparse Matrix Converter. Dr. Kolar has published over 250 scientific papers in international journals and conference proceedings and has filed more than 70 patents. He was appointed Professor and Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich on Feb. 1, 2001.

The focus of his current research is on AC-AC and AC-DC converter topologies with low effects on the mains, e.g. for power supply of telecommunication systems, More-Electric-Aircraft and distributed power systems in connection with fuel cells. Further main areas of research are the realization of ultra-compact intelligent converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and EMI filtering, multi-domain/multi-scale modeling and simulation, pulsed power, bearingless motors, and Power MEMS. He received the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005. He also received an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003. In 2006, the European Power Supplies Manufacturers Association (EPSMA) awarded the Power Electronics Systems Laboratory of ETH Zurich as the leading academic research institution in Europe.

Dr. Kolar is a Member of the IEEE and a Member of the IEEJ and of Technical Program Committees of numerous international conferences in the field (e.g. Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). From 1997 through 2000 he has been serving as an Associate Editor of the IEEE Transactions on Industrial Electronics and since 2001 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.