ISOLATED ZVS-PWM DC-DC CONVERTER BASED ON THE VARIABLE CAPACITOR TECHNIQUE

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***Abstract* – This paper introduces a new static power conversion principle, based on the variable capacitance of a capacitor arrangement. As an example of the proposed technique, an isolated ZVS-PWM dc-dc converter topology is proposed. Circuit operation and theoretical analysis, with emphasis on the soft-commutation process, are included in the paper. To validate the theoretical analysis and verify the operation of the converter, a proof-of-concept experimental prototype with 960 W power rating, 400 V input voltage, 48 V output voltage and 100 kHz switching frequency was designed, constructed and tested in a laboratory. An additional attribute of the proposed technique is the reduction of the voltage across the power semiconductors to two-thirds of the dc bus voltage, when the duty cycle is equal to 0.5. The proposed technique can be extended and used to generate several other topologies of isolated and non-isolated dc-dc converters.**

Keywords **– DC-DC Converter, Isolated, Soft Commutation, Variable Capacitance.**

I. INTRODUCTION

Static converters are made up of active and passive components. Modern active components are power semiconductors operating as switches. Ideally, they can be considered as resistors with variable resistance, being null in the conduction state and infinite in the blocked state.

Passive elements are capacitors, inductors and coupled inductors or transformers. Usually, the parameters of these components are constant and independent of the currents, voltages or operating frequencies.

The passive components are used to perform filtering, energy accumulation and insulation, playing no role in controlling the power flow between the input source and the load of a converter.

The active components or switches, by varying the operating frequency or the relative times between the ON or the OFF states, allow the control of the power flow between the external sources, and consequently the internal voltages and currents at their terminals.

The use of variable capacitors has been presented in the literature as a possible technique for the control of resonant converters operating at a constant frequency, since the control variable of these converters is the ratio of the switching frequency to the resonance frequency. The obtaining of a variable capacitor using fixed capacitances, inductances, and power semiconductors, to change the resonance frequency of the series resonant converter was originally introduced in [1].

The use of ceramic capacitors with voltage-dependent capacitance was introduced in [2] to control the resonant frequency of the resonant series converter and in [3] to control the resonant frequency of the LLC resonant converter.

In the solutions presented, although the variable capacitor is used to control the processed power, it remains a passive component of the converter since its variation occurs slowly and not in the frequency of the active elements that operate in the switching frequency, which are the power semiconductors.

A different method presented in [4-6] employs the interdependence between capacitance voltage in variable capacitors, obtained using micro-electro-mechanical techniques (MEMS). The capacitance variation is obtained through the variation. of the parallel plate gap. The capacitor is charged with a fixed charge. The increase in the parallel plate gap of the capacitor resulted in the capacitance decreases and increases in the voltage across the capacitor. Conversely, if the distance between the parallel plates of the capacitor decreases, the capacitance will increase, resulting in a decrease in the voltage across the capacitor.

The capacitor operating principle is better understood with the aid of the circuit shown in Figure 1, in which $C(x)$ represents a variable capacitance capacitor.

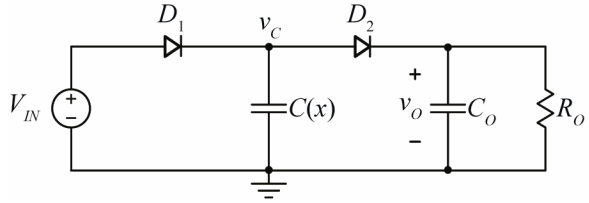


Fig. 1. Step-up dc-dc converter with variable capacitor.

The capacitance of capacitor $C(x)$ varies periodically. In the time interval. Where the capacitance $C(x)$ reach its minimum value $C(x) = C_{min}$, the voltage across $C(x)$ becomes greater than the supply voltage V_{IN} and diode D_1 is blocked. Diode D_2 conducts and part of the energy stored in $C(x)$ is transferred to the output stage formed by C_O and R_O. In this way, the output voltage v_O is greater than the input voltage V_{IN} and the circuit is a voltage step-up. From the instant when the capacitance $C(x)$ reach its maximum, $C(x) = C_{max}$, diode D_2 blocks while the diode D_1

Manuscript received 05/09/2023; first revision 06/16/2023 and accepted for publication 08/28/2023, by recommendation of Editor Telles Brunelli Lazzarin. http://dx.doi.org/10.18618/REP.2023.3.0012

conducts, connecting the capacitor $C(x)$ in parallel with the voltage source V_{IN}. In this time interval, energy is transferred from the source V_{IN} to the capacitor $C(x)$.

The capacitances obtained using the method proposed in [4-6] are in the order of some picofarads, allowing only the processing of very low power.

In the technique proposed in this paper, the variable capacitor can be interpreted as an active element of the circuit, replacing the power semiconductors. Therefore, the frequency of change of capacitance is equal to the switching frequency of the converter differently from the solutions proposed in [1-3].

Currently, there are no capacitors capable of varying their capacitance quickly. To emulate this particular is used the commutation cell is presented in Figure 2.

II. PROPOSED CONVERTER

The power stage of the proposed converter is shown in Figure 2.a. It consists of the semiconductors S_{1a}, S_{1b}, and S_2, two switched capacitors C_X and C_Y, the high frequency isolating transformer T, the magnetizing inductance L_M and the commutation inductance L_C which includes the transformer leakage inductance.

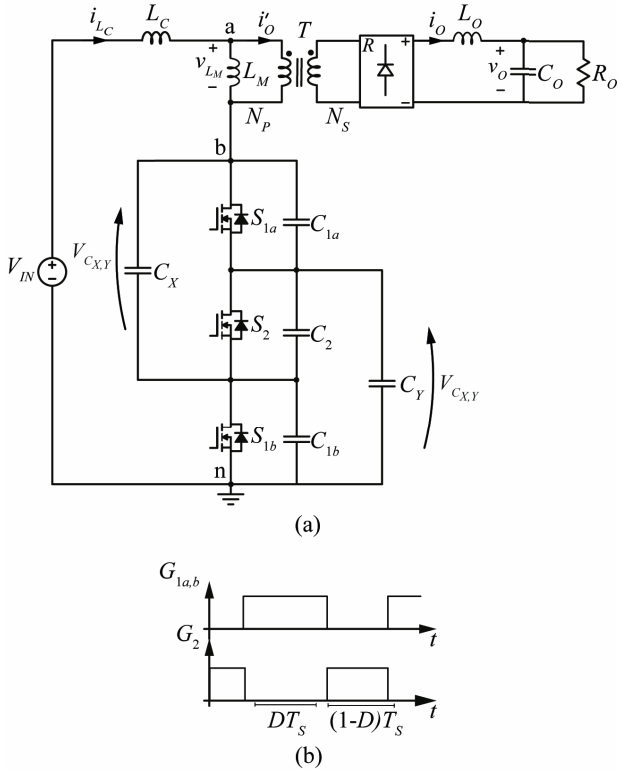


Fig. 2. Proposed isolated dc-dc converter. (a) Power stage. (b) Gate signals.

The output stage consists of the diode rectifier R and the filtering stage L_O and C_O. The input voltage source is denoted by V_{IN} and the load by the resistor R_O.

The capacitors C_{1a}, C_{1b}, and C_2 are auxiliary commutation capacitors.

The gate signals of the power semiconductors ($G_{1a,b}$ e G_2) are shown in Figure 2.b. Switches S_{1a}, and S_{1b} are driven by the same signal. The control of the converter is carried out by PWM modulation, with a constant frequency and variable duty cycle D.

III. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

The arrangement formed by switches S_{1a}, S_{1b}, and S_2, with capacitors C_X and C_Y, and ideal components, is shown in Figure 3.a, and its two topological states are shown in Figures 3.b and 3.c, for the time intervals ($0 - DT_S$) and ($DT_S - T_S$), respectively.

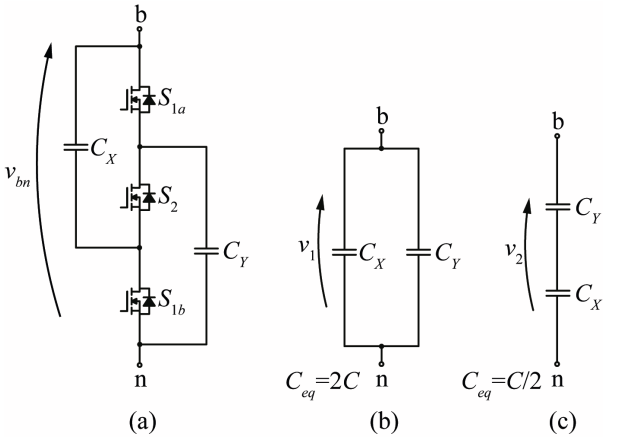


Fig. 3. (a) Arrangement for obtaining variable capacitance. (b) Equivalent circuit for the time interval ($0 - DT_S$). (c) Equivalent circuit for the time interval ($T_S - DT_S$).

In the time interval ($0 - DT_S$), semiconductors S_{1a} and S_{1b} are closed while S_2 is open. Thus, the two C_X and C_Y, are associated in parallel. Since $C_X = C_Y = C$, the equivalent capacitance is $C_{eq} = 2C$.

In the time interval ($T_S - DT_S$), semiconductors S_{1a} and S_{1b} are open and S_2 is closed. Hence, capacitors C_X and C_Y are associated in series and the equivalent capacitance is $C_{eq} = C/2$. Therefore, the described arrangement functions as a variable capacitor.

Since the average values of the voltages across the inductors L_M and L_C in steady state are equal to zero, it can be concluded that the average value of the voltage across the terminals bn, $\overline{V_{bn}}$ is equal to V_{IN}. Thus,

$$\overline{V_{bn}} = V_{IN}. \quad (1)$$

The change in the capacitance across the terminals bn causes an alternating component of voltage to appear superimposed on its average value. The corresponding waveforms are shown in Figure 4.

During the time interval $(0-DT_S)$, shown in Figure 3.b, the equivalent capacitance is equal to $2C$ and the total charge is given by

$$Q_{Total} = Q_{C_X} + Q_{C_Y} = 2Q\,. \tag{2}$$

The charge of each of the capacitors over the time interval $(0-DT_S)$ is given by

$$Q = C \cdot v_1\,. \tag{3}$$

From (3) it is defined that $v_1 = Q/C$.

In the time interval $(T_S - DT_S)$, shown in Figure 3.c, the capacitors are connected in series. So, the equivalent capacitance is $C/2$. The charge corresponding to the equivalent capacitance is Q. The voltage between the terminals bn during the time interval $(T_S - DT_S)$, denote by v_2, is defined as

$$v_2 = \frac{2Q}{C}\,. \tag{4}$$

Rearranging (4) we obtain $Q/C = v_2/2$. From (3) it is defined that $Q/C = v_1$. It can be concluded that

$$v_2 = 2 \cdot v_1\,. \tag{5}$$

In the steady state, the average value of the alternating component of the voltage across the terminals ab is zero. Therefore,

$$(V_{IN} - v_1) \cdot D = (v_2 - V_{IN}) \cdot (1-D). \tag{6}$$

Substitution of (5) in (6) yields

$$(V_{IN} - v_1) \cdot D = (2 \cdot v_1 - V_{IN}) \cdot (1-D). \tag{7}$$

Thus, the voltages v_1 and v_2 are given by (8) and (9), respectively.

$$v_1 = \frac{V_{IN}}{2-D}\,. \tag{8}$$

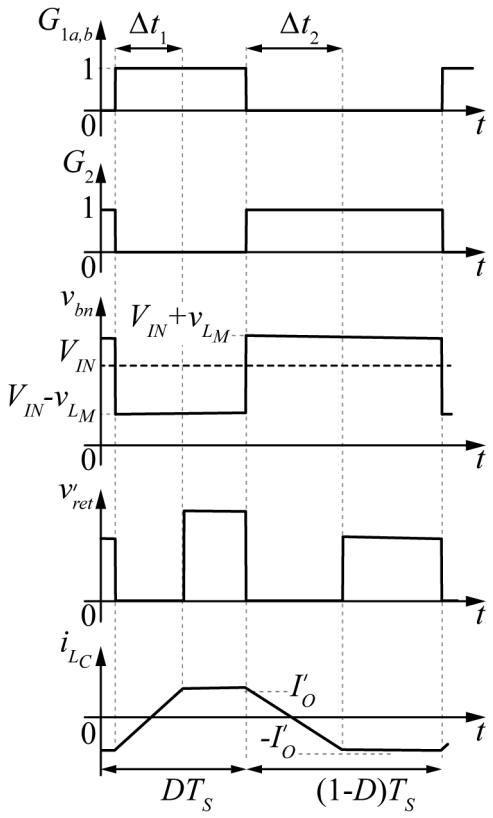


Fig. 4. Typical waveforms of the proposed converter.

$$v_2 = \frac{2 \cdot V_{IN}}{2-D}\,. \tag{9}$$

Equations (8) and (9) show that the alternating component of voltage v_{bn} depends only on the input voltage V_{IN} and the duty cycle D.

V. ANALYSIS OF THE IDEAL CONVERTER WITH $L_C \neq 0$

Figure 5 shows the equivalent circuit of the converter. To simplify the analysis, we assume that L_C is located after the magnetizing inductance L_M and before the rectifier stage, and that all components were referred to primary side of the transformer.

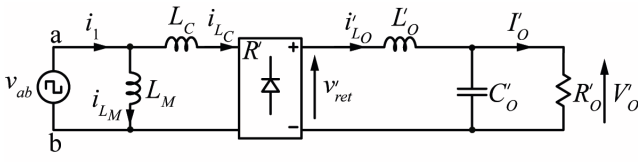


Fig. 5. The equivalent circuit of the proposed ideal converter with the inclusion of the inductance L_C, and all parameters referred to the primary side of the transformer.

The typical and relevant waveforms for describing the operation of the converter with ideal components and $L_C \neq 0$ are shown in Figure 4.

During the time intervals Δt_1 and Δt_2 in which $\left|i_{L_C}\right| < I'_O$, all diodes of the rectifier stage are in conduction, the voltage at its output be zero, causing a reduction in the effective duty cycle and consequently in the average value of the load voltage.

A. Duty Cycle Loss

The voltage across the inductor L_C is equal to $V_{IN} - v_1$ during the time interval Δt_1 and equal to $2 \cdot v_1 - V_{IN}$ during the time interval Δt_2. The current excursion Δt_2 in L_C is equal to $2 \cdot I'_O$ in both stages of operation. Therefore, the voltage across L_C is given by

$$v_{L_C} = L_C \frac{\Delta I}{\Delta t}. \tag{10}$$

Thus, the duration of time intervals Δt_1 and Δt_2 are defined in (11) and (12), respectively.

$$\Delta t_1 = \frac{2L_C \cdot I'_O}{V_{IN}} \cdot \left(\frac{2-D}{1-D}\right) \tag{11}$$

$$\Delta t_2 = \frac{2L_C \cdot I'_O}{V_{IN}} \left(\frac{2-D}{D}\right). \tag{12}$$

The reduction of the duty cycle is given by

$$\Delta D = \frac{\Delta t}{T_S}. \tag{13}$$

Substituting (11) and (12) in (13) we find

$$\Delta D_1 = \frac{2 \cdot f_S \cdot L_C \cdot I'_O}{V_{IN}} \cdot \left(\frac{2-D}{1-D}\right) \tag{14}$$

$$\Delta D_2 = \frac{2 f_S \cdot L_C \cdot I'_O}{V_{IN}} \left(\frac{2-D}{D}\right). \tag{15}$$

B. Static Gain and Output Characteristics

From the waveforms shown in Figure 4, we obtain the average rectified voltage, given by

$$V'_O = V_{IN} \frac{(1-D)}{(2-D)} \left(D - \Delta D_1\right) + V_{IN} \frac{D}{(2-D)} \left(1 - D - \Delta D_2\right). \tag{16}$$

Hence, substitution of (14) and (15) in (16) and proper rearrangement yields is define the static voltage gain G of the converter, given by

$$G = \frac{V'_O}{V_{IN}} = \frac{2D \cdot (1-D)}{(2-D)} - \frac{4 f_S \cdot L_C \cdot I'_O}{V_{IN}}. \tag{17}$$

Let us define the normalized load current referred to the transformer primary side by

$$\overline{I}'_O = \frac{4 f_S \cdot L_C \cdot I'_O}{V_{IN}}. \tag{18}$$

Substitution of (18) in (17) gives

$$G = \frac{2D(1-D)}{2-D} - \overline{I}'_O. \tag{19}$$

Note that the equivalent capacitance does not appear explicitly in the static gain expression. This is because the energy transferred from the voltage source V_{IN} to the load does not depend on the average capacitance value of the equivalent capacitor, but rather on the instantaneous values that are equal to $2 \cdot C$ and $C/2$ during the time intervals $(0 - DT_S)$ and $(T_S - DT_S)$, respectively.

Equation (19) is plotted in Figure 6, for various values of $\overline{I}'_O$, as a function of the duty cycle D. The maximum voltage gain value occurs when $D = 0.586$. As usual, the static gain decreases with increasing $\overline{I}'_O$, due to the reduction of the effective duty cycle.

The load characteristic of the ideal converter, with all quantities referred to the transformer primary side, defined by equation (19), which is represented graphically in Figure 7.

The voltage drops across the commutation inductor L_C reduces the value of the load voltage with increasing current, which is a common property of all isolated ZVS-PWM DC-DC with output LC filter.

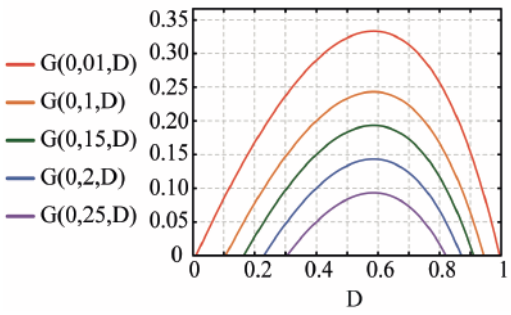


Fig. 6. Voltage static gain depending on D for different values of $\overline{I}'_O$.

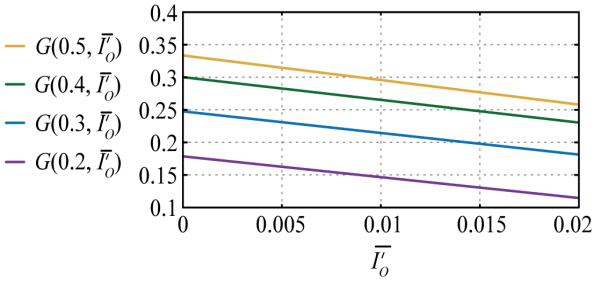


Fig. 7. Load characteristic of the proposed converter for several values of the duty cycle D.

C. Semiconductors Voltage Stress

The voltage across the switches is given by

$$v_S = \frac{V_{IN}}{2-D} \tag{20}$$

with values within the range $\frac{V_{IN}}{2} \le v_S \le V_{IN}$ for duty cycles within the range $0 \le D \le 1$ Therefore, the voltage across the power semiconductors is two-thirds of V_{IN} when $D = 0.5$.

The voltage across the secondary windings of the transformer is equal to $2 \cdot v_{L_M} / n$. During the second time interval $(T_S - DT_S)$ the diode D_{R1} is blocked and the voltage across it is defined by:

$$v_{D_{R1}} = 2\left(\frac{V_{IN} - v_1}{n}\right) = \frac{2 \cdot V_{IN}}{n}\left(\frac{1-D}{2-D}\right). \tag{21}$$

In the first-time interval (DT_S) the diode D_{R2} current flow is blocked. The voltage across D_{R2} is defined by

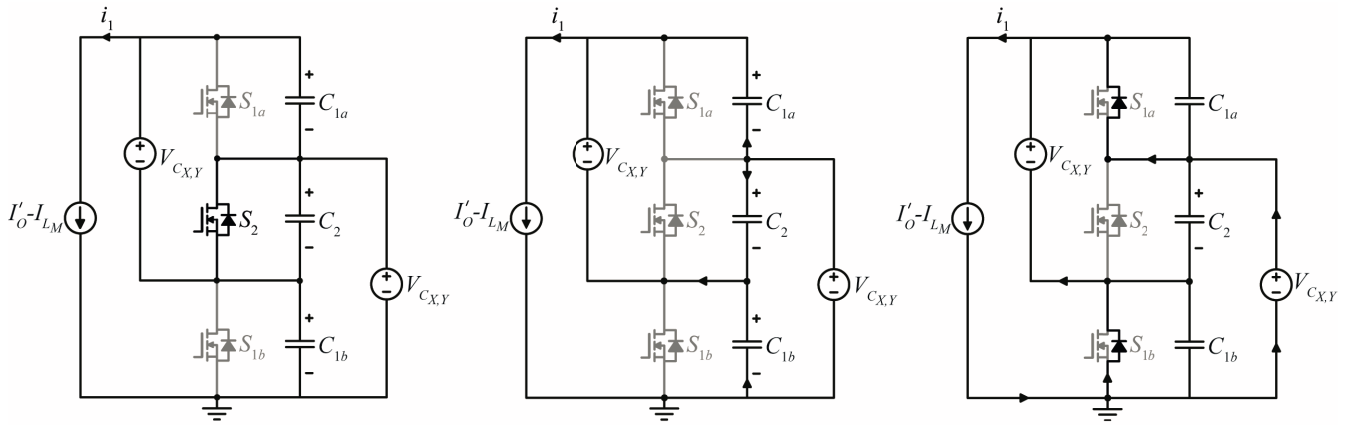
$$v_{D_{R2}} = 2\left(\frac{V_{IN} - v_2}{n}\right) = \frac{2 \cdot V_{IN}}{n}\left(\frac{D}{2-D}\right). \tag{22}$$

From (21) and (22), it can be noticed that the voltage across D_{R1} decreases and the voltage across D_{R2} increases with the increases in the value of the duty cycle D. The voltage across theses diodes become equal when the duty cycle is $D = 0.5$.

VI. COMMUTATION ANALYSIS

To analyze the commutation, the equivalent circuit of the converter shown in Figure 2 is used. The commutation capacitors C_{1a}, C_{1b} and C_2, which are the same, are included and connected in parallel with the power semiconductors. An appropriate dead time is introduced between the gate signals of the switches.

To simplify the analysis, the alternating component of the magnetizing current was ignored. Thus, $i_{L_M} = I_{L_M}$, where I_{L_M} denotes the average value of the magnetizing current.



(a) (b) (c)

Fig. 8. Topological states for commutation analysis when S_2 is gated OFF. (a) Before S_2 turns OFF. (b) Charge of capacitor C_2 and discharge of capacitors C_{1a} and C_{1b}. (c) Just before S_{1a} and S_{1b} are gated ON.

The switching of S_{1a}, S_2, and S_{1b} occurs similarly. However, the turn-off commutation of S_2 is more critical, since the energy available in the commutation inductor L_C to charge and discharge the commutation capacitors at turn OFF of S_2 is less than that available for the commutation of S_{1a} and S_{1b}. Therefore, only the turn OFF analysis of the power semiconductor S_2 is presented. Identical approach can be used to find the equations for the turn off analysis of S_{1a} and S_{1b}.

At the instant before the switch S_2 is turned OFF, the current is given by

$$i_1 = I'_O - I_{L_M}. \tag{23}$$

Before the instant $t = t_0$ the power semiconductor S_2 conducts the current i_{L_C} while S_{1a} and S_{1b} continue open. This topological state is represented in Figure 8.a, in which $v_{C_{1a}} = v_{C_{1b}} = V_{C_{X,Y}}$, $v_{C_2} = 0$ and $v_{C_X} = v_{C_Y} = V_{C_{X,Y}}$.

At the instant $t = t_0$ the switch S_2 is turned OFF and the commutation begins. The corresponding topological state is shown in Figure 8.b. The capacitor C_2 charges linearly with a constant current, while C_{1a} and C_{1b}, discharge linearly, also with a constant current. The turn OFF of S_2 is theoretically lossless with ZVS.

At the $t = t_2$, $v_{C_2} = V_{C_{X,Y}}$ and $v_{C_{1a}} = v_{C_{1b}} = 0$. The diodes in antiparallel with the switches S_{1a} and S_{1b} start to conduct the current i_1. Semiconductors S_{1a} and S_{1b} must be gated ON while the respective diodes are conducting, so that they start to conduct at zero voltage without switching losses.

The current in capacitor C_2 during the time interval ($t_0 - t_{C2}$) is given by

$$i_{C_2} = \frac{i_1}{3}. \tag{24}$$

Substituting (23) in (24) we find

$$i_{C_2} = \frac{I_{L_M} - I'_O}{3}. \quad (25)$$

The commutation time t_{C2} is determined by

$$t_{C2} = \frac{C_2 \cdot V_{C_{X,Y}}}{i_{C_2}}. \quad (26)$$

Substitution of (25) in (26) gives

$$t_{C2} = \frac{3 \cdot C_2 \cdot V_{IN}}{(2-D) \cdot (I'_O - I_{L_M})}. \quad (27)$$

The converter parameters must be chosen properly so that the dead-time t_d is greater than the time t_{C2}.

The typical and relevant waveforms for this commutation are shown in Figure 9.

According to (27), t_{C2} depend on V_{IN}, I'_O and D. For a constant output voltage V_O, regulated by the voltage controller of the converter, the duty cycle D decreases with an increase in the input voltage V_{IN}, increasing the switching time t_{C2}, as follows from (27). Similarly, there is an increase in t_{C2} when the processed power decreases, with a consequent decrease in I'_O.

Therefore, the commutation parameters must be adjusted to the maximum value of the input voltage and the chosen the maximum value of the input voltage and the chosen minimum value for the processed power, usually close to the nominal power value.

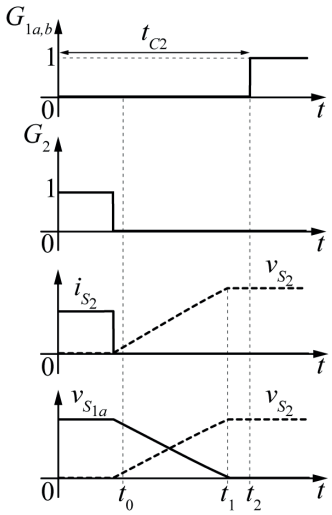


Fig. 9. Typical waveforms for the commutation initiated when S_2 is gated OFF. (a) Gate signals. (b) Voltage and current in S_2. (c) Voltage S_{1a} and S_2.

VII. DESIGN METHODOLOGY

In order to validate the theoretical analysis of the proposed topology, a proof-of-concept prototype was designed based on the specifications presented in Table I.

TABLE I
Converter Specification

Symbol	Quantity	Value
P_O	Rated power	900 W
V_{IN}	Input Voltage	400 V
V_O	Output voltage	48 V
f_S	Switching frequency	100 kHz

Initially, the specification and construction of the transformer were carried out, since the values of the magnetization and the leakage inductance influences the static voltage gain and the commutation of the converter. The transformer turns ratio as well as the leakage and magnetization inductance values are shown in Table II. The currents in the secondary and tertiary windings are equal to half of the output current. Therefore, 300 AWG 38 wires were needed in parallel for each of the windings. So, it was decided to use Litz wires. For the primary winding of the transformer, two Litz 150X38 wires were used.

The value of the commutation inductance is defined respecting two conditions: a) it does not result in a loss of cyclic ratio greater than that specified; b) be large enough to store the energy necessary for the complete discharge of the commutation capacitors [7]. The values obtained for the commutation capacitances and the commutation inductance are shown in Table II.

The voltage stresses across switches S_{1a}, S_{1b} and S_2 are defined by (20). For the values specified in Table II, the voltage across S_{1a}, S_{1b} and S_2 is approximately 258 V.

The effective value of the current through S_{1a} and S_{1b} is approximately 2.12 A and the current through S_2 is 2.74 A. As the purpose of the prototype is only to validate the theoretical analysis results, we chose to use components available in the laboratory. The available switch that best meets design requirements was the SiC MOSFET model SCT3120AL, with rated voltage and current equal to 650 V and 21 A, respectively, and ON resistance equal to $0.12\ \Omega$.

The value of the capacitances C_X and C_Y, must ensure that the converter operate in partial charge mode ($f_s \tau > 0,2$), in order to avoid excessive losses in the switches, and that the capacitors voltage ripple be maintained within the limits specified for the converter [7]

The transformer and output power stage are shown in Figure 10, where the transformer secondary voltage is rectified by the half-bridge Schottky diodes D_{R1} and D_{R2}. It is important to prevent overvoltage across the diodes, caused by the interaction between the transformer leakage inductance and the capacitors of the diodes D_{R1} and D_{R2}. Two voltage clamps are therefore needed across the diodes,

which are represented by D_a, and R_a for D_{R1}, and D_b, C_b and R_b for D_{R2}. The resistors R_a and R_b serve to transfer part of the clamp charge to the output capacitor C_O [8].

TABLE II
Components Specifications

Symbol	Parameters	Value
C_1, C_2	Switched capacitances	25 μF
C_O	Output filter capacitance	1000 μF
L_O	Output filter inductance	27.78 μH
n	Transformer turns-ration	1.57
L_M	Magnetizing inductance	184.6 μH
-	Transformer leakage inductance	3.4 μH
-	Auxiliar commutation inductance	6.39 μH
L_C	Total commutation inductance	11.19 μH
D_{R1}, D_{R2}	Output rectifier diodes	MBR40250TG
S_{1a}, S_2, S_{1b}	Power semiconductors	SCT3120AL /650-V
t_d	Dead-time	200 ns
D_a, D_b	Clamping diodes	MBR40250TG
R_a, R_b	Clamping resistors	7.5 kΩ
C_a, C_b	Clamping capacitors	330 nF

The threshold voltage across the diode D_{R1}, given by (21), is approximately 175 V and the threshold voltage across the diode D_{R2}, given (22), is approximately 140 V. The current through the diodes is equal to the output current, 18.75 A. Thus, 40 A and 250 V Shottky diodes were selected.

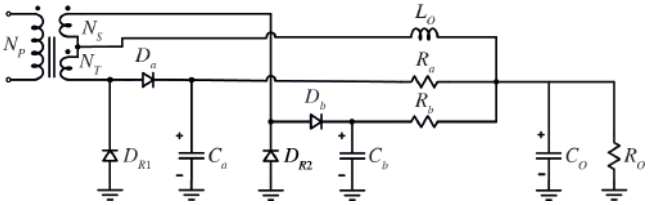


Fig.10. Transformer and output stage of the proof-of-concept experimental prototype of the proposed DC-DC converter.

The equations for the output inductance and capacitance (C_O and L_O) determination are identical to those employed in the half-bridge converter [9].

VIII. EXPERIMENTAL RESULTS

The proof-of-concept prototype designed and built with the specifications given in Table I.is shown in Figure 11.

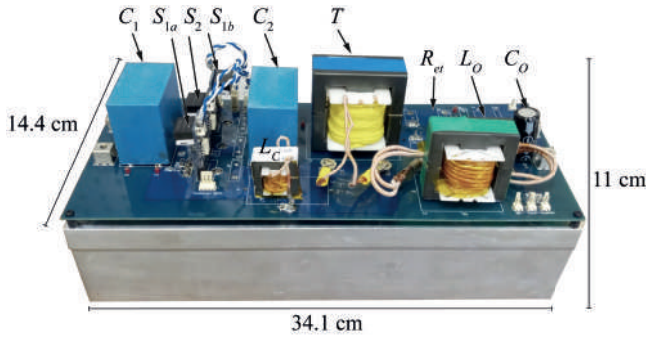


Fig. 11. Proof-of-concept experimental prototype of the proposed DC-DC.

MOSFETS S_{1a}, S_2 and S_{1b} are gated using the PWM signals shown in Figure 12 which are generated by a F28069M DSP controller. An appropriate dead-time between the gate signals is included to prevent both switches from conducting simultaneously, causing a short circuit. The dead time is also necessary for the realization of commutation with ZVS. The specification of the dead time and the components used in the prototype are presented in Table II.

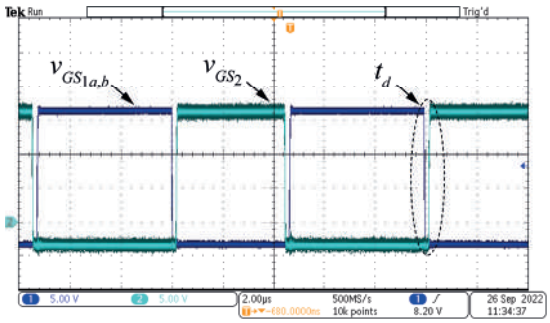


Fig. 12. Gate signals with duty cycle equal to 0.55 and dead time equal to 200 ns. Where $V_{GS_{1a,b}}$ and V_{GS_2} represented the command signals on S_{1a}, S_{1b} and S_2 respectively. t_d represented the dead time. Voltage scale: 5 V/Div. Time scale:2µ s/Div.

The selected dead-time combined with the other parameters that take part in the commutation allows the converter to operate with ZVS when operated from 30% to 100% of the rated power load [10]. Figure 13 shows the waveforms during the time interval in which the MOSFET S_{1a} is turned ON and the MOSFET S_2 is turned OFF with ZVS, when the converter operates at 50% the rated power.

Figure 13 shows that the voltage across the switch S_{1a} reaches zero before S_{1a} and S_{1b} are gated ON. Therefore, S_{1a} and S_{1b} turn OFF with ZVS. The value of v_{DS_2} remains null until the switch S_2 is gated OFF. Therefore, S_2 turns OFF with ZVS.

The turn OFF of S_2 is the critical commutation, since the current available to perform this commutation is smaller than that available at the instant the MOSFETS S_{1a} and S_{1b} are turned OFF. Thus, if the circuit parameters allow S_2 to

commutate with ZVS, switches S_{1a} and S_{1b} also commutate with ZVS.

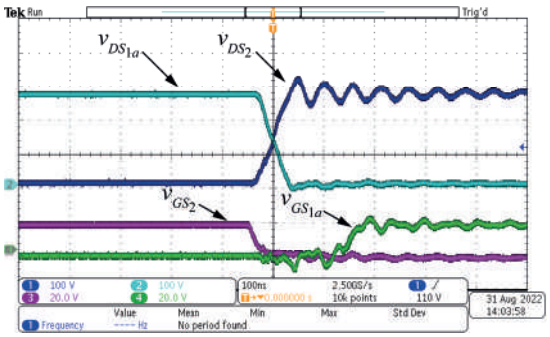


Fig. 13. Gate signals and voltage stress of power semiconductors S_{1a} and S_2 when S_2 is turned OFF and S_{1a} ON. Where $v_{DS_{1a}}$ represented the voltage across S_{1a} and v_{DS_2} represented the voltage across S_2. Voltage scale: a) $v_{DS_{1a}}$ e v_{DS_2} : 100 V/Div.; b) $v_{GS_{1a}}$ e v_{GS_2} : 20 V/Div.. Time scale: 100n s/Div.

Figure 14 shows the relevant switching waveforms in which S_{1a} and S_{1b} are turned OFF. The voltage v_{DS_2} reaches zero before S_2 is gated ON and is equal to zero at the instant S_{1a} is turned OFF. Therefore, S_{1a} and S_{1b} turn OFF and S_2 turns ON with ZVS.

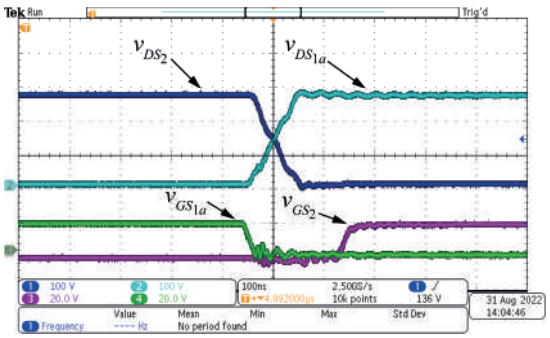


Fig. 14. Gate signals and voltage stress of power semiconductors S_{1a} and S_2 when S_{1a} and S_{1b} are turned OFF and S_2 is turned ON. Voltage scale: a) $v_{DS_{1a}}$ e v_{DS_2} : 100 V/Div.; b) $v_{GS_{1a}}$ e v_{GS_2} : 20 V/Div.. Time scale: 100n s/Div.

Figure 15 shows the waveforms of the currents through the output filter inductor and the commutation inductor L_C. It can be noted that the instantaneous value of i_{L_C} is greater at the instant S_{1a} and S_{1b} are turned OFF than that which occurs at the instant S_2 is turned OFF.

Figure 16 shows the voltage waveforms across the MOSFETS S_{1a} and S_2, that values are close to two-thirds of the input DC voltage for the converter operating with $D = 0.55$, which is in agreement with the results obtained by the theoretical analysis. The voltages across S_{1a} and S_2 are equal to the value of the voltage v_i across the capacitors C_X and C_Y, which are defined by (20)

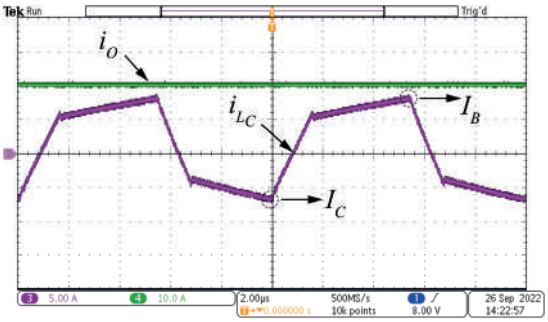


Fig. 15. Currents i_O in the output filter inductor and i_{L_C} in the inductor L_C. I_B is value of the current L_C at the instant S_{1a} and S_{1b} are gated OFF and I_C at the instant S_2 turns OFF. Current scale: a) i_O : 10 A/Div.; b) i_{L_C} : 5 A/Div.; Time scale: 2µ s/Div.

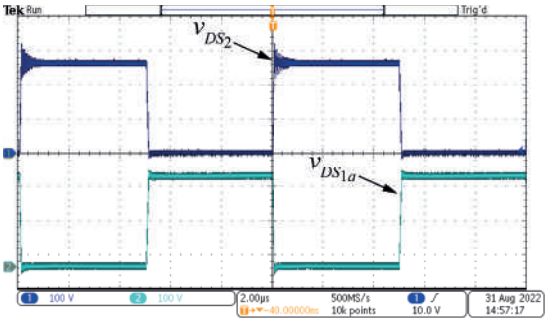
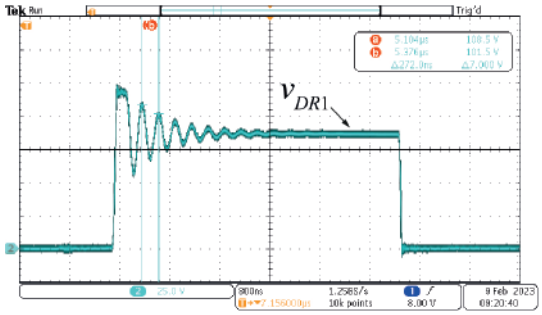


Fig. 16. Voltages v_{DS_2} and $v_{DS_{1a}}$ across the power semiconductors S_2 and S_{1a}, respectively. Voltage scale: 100 V/Div.. Time scale: 2µ s/Div.

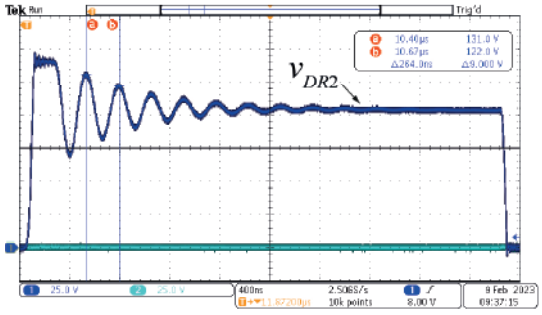
Figure 17 shows the voltage waveform across the diodes D_{R1} and D_{R2} of the output diode rectifier. It can be noticed the existence of overvoltage across the diodes due to the interaction between their capacitances and the leakage inductance of the transformer added to the other parasitic inductances. The peak value of these voltages are limited by the clamping circuit shown in Figure 10. These oscillations also occur in other dc-dc converters with output LC filter.

The experimental output characteristics of the converter for different duty cycle values are shown in Figure 18. The trend lines are linear and are in agreement with the results obtained by the theoretical analysis presented in Figure 7. These output characteristics are similar to those of the FB-ZVS-PWM and the HB-ZVS-PWM converters.

The efficiency curve of the proof-of-concept experimental prototype was measured with a Tektronix power analyzer (PA3000). The experimental curve is shown in Figure 19 in which a maximum efficiency of 93.62% occurs at 62% of the rated power. At rated power, the measured efficiency is 91.80%. The experimental distribution of losses is shown in Figure 20, for the converter operating at rated power.



(a)



(b)

Fig. 17. Voltages across the diodes D_{R1}, $v_{D_{R1}}$ and voltage across D_{R2}, $v_{D_{R2}}$. Voltage scale: 25 V/Div.. Time scale: 400n s/Div.

The experimental output characteristics of the converter for different duty cycle values are shown in Figure 18. The trend lines are linear and are in agreement with the results obtained by the theoretical analysis presented in Figure 7. These output characteristics are similar to which of the FB-ZVS-PWM and the HB-ZVS-PWM converters.

The efficiency curve of the proof-of-concept experimental prototype was measured with a Tektronix power analyzer (PA3000). The experimental curve is shown in Figure 19 in which a maximum efficiency of 93.62% occurs at 62% of the rated power. At rated power, the measured efficiency is 91.80%. The experimental distribution of losses is shown in Figure 20, for the converter operating at rated power.

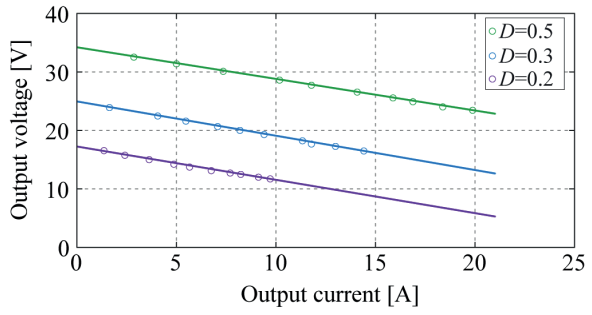


Fig. 18. Experimental output characteristics of the proposed converter.

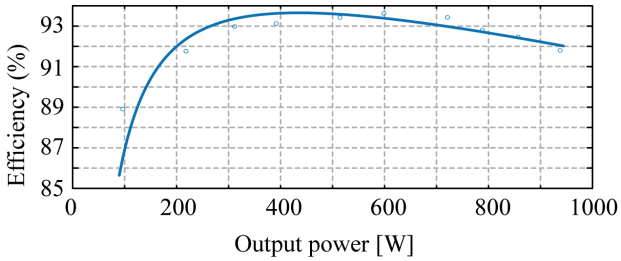


Fig. 19. Experimental efficiency curve of the proof-of-concept laboratory prototype of the proposed converter.

Three types of losses basically occur in the converter. The first type is the constant and independent losses of the power delivered to the load, which in this measurement is equal to 13.99% of the total losses. The second type is the losses proportional to the power, formed basically by the power dissipated by the average value of the current in the diodes, which correspond to 20.55% of the total losses. The third type of losses are the conduction losses of the equivalent semiconductor resistances, capacitors and magnetic devices. The experimental measured value of these losses corresponds to 65.46% of the total losses. These losses can be substantially reduced when synchronous rectifiers, optimized magnetic devices, and power semiconductors with lower equivalent resistance are used.

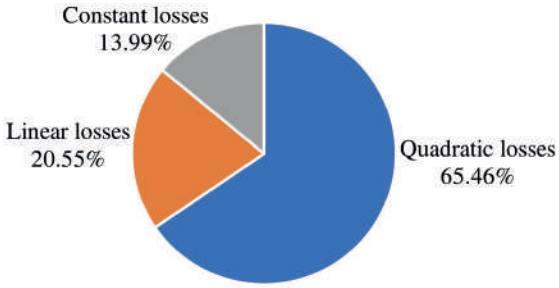


Fig. 20. Measured distribution of losses in the converter power stage.

According to the theoretical determination of the losses in the different components of the power stage, 41.07% occur in the transformer, 21.36% in the rectifier diodes, 14.83% in the MOSFETs, 8.67% in the output inductor, 7.5% in the voltage clamping circuit of the diodes, and 6.55% in the auxiliary commutation inductor.

V. Comparison With the Asymmetric HB-ZVS-PWM Converter

This section compares the proposed converter and the asymmetric HB-ZVS-PWM converter [11], whose power stage diagram is shown in Figure 21.

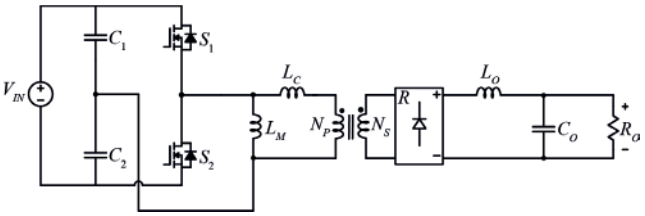


Fig. 21. Power stage diagram of the asymmetric HB-ZVS-PWM Converter [11].

In this analysis, we assume that the two converters operate with identical input voltage, output voltage, power delivered to the load and switching frequency. We will also consider zero switching losses and ideal all components except active semiconductors. We will then compare the conduction losses in the transistors of the two converters. Let us consider the power MOSFET ON-resistance proportional to 2.5 power of its break-down voltage [12], given by

$$R_{ON} = \beta V^{2.5}. \tag{28}$$

A. Asymmetric HB-ZVS-PWM Converter Conduction Losses

The rms values of currents in switches S_1 and S_2 of the converter shown in Figure 28 are given by (29) and (30) respectively [10].

$$I_{S_1,rms} = 2\left(1-D_1\right)\sqrt{D_1}\cdot I_O \frac{N_S}{N_P} \tag{29}$$

$$I_{S_2,rms} = 2D_1\sqrt{1-D_1}\cdot I_O \frac{N_S}{N_P}. \tag{30}$$

D_1 is the duty cycle in Asymmetric HB-ZVS-PWM Converter.

The transistors S_1 and S_2 conduction losses are defined by (31) and (32), respectively.

$$P_{S_1} = R_{ON}\cdot I^2_{S_1,rms} \tag{31}$$

$$P_{S_2} = R_{ON}\cdot I^2_{S_1,rms} \tag{32}$$

Substitution of (29) and (30) in (31) and (32) yields, respectively

$$P_{S_1} = R_{ON}\cdot D_1\left(1-D_1\right)^2\cdot I_O^2\left(\frac{N_S}{N_P}\right)^2 \tag{33}$$

$$P_{S_2} = R_{ON}\left(1-D_1\right)D_1^{\,2}\cdot I_O^2\left(\frac{N_S}{N_P}\right)^2. \tag{34}$$

The total power lost by conduction is the sum of P_{S_1} and P_{S_2}. Therefore:

$$P_1 = 2R_{ON}\cdot I_O^2\left(\frac{N_S}{N_P}\right)^2\left[\sqrt{D_1}\left(1-D_1\right)+D_1\sqrt{1-D_1}\right]. \tag{35}$$

Substituting (28) into (35) we find

$$P_1 = 2\beta\cdot V_{IN}^{2.5}\cdot I_O^2\left(\frac{N_S}{N_P}\right)^2\left[\sqrt{D_1}\left(1-D_1\right)+D_1\sqrt{1-D_1}\right]. \tag{36}$$

B. Proposed Converter Transistor Conduction Losses

It can be demonstrated that the rms value of the current in the switches S_{1a} and S_{1b} the converter shown in Figure 2 is given by

$$I_{S_{1ab},rms} = 2\sqrt{D_2}\cdot I_O \frac{N_{S1}}{N_{P1}}\left(\frac{1-D_2}{2-D_2}\right) \tag{37}$$

and that the rms current in switch S_2 is

$$I_{S_2,rms} = 2\sqrt{1-D_2}\cdot I_O \frac{N_{S1}}{N_{P1}}\left(\frac{D_2}{2-D_2}\right). \tag{38}$$

The total conduction losses P_2 in these semiconductors is given by

$$P_2 = R_{ON}\left(2I^2_{S_{1ab},rms}+I^2_{S_2,rms}\right). \tag{39}$$

Substitution of (28), (29) and (30) into (39) yields

$$P_2 = 4\beta\left(\frac{V_{IN}}{2-D_2}\right)^{2.5}\cdot I_O^2\left(\frac{N_{S1}}{N_{P1}}\right)^2\left[\frac{D_2\left(1-D_2\right)}{2-D_2}\right]. \tag{40}$$

C. Relationship Between Transistor Conduction Losses

The transformer ratio of turns of the asymmetric HB-ZVS-PWM converter is given by

$$\frac{N_S}{N_P} = \frac{V_{O1}}{2D_1\left(1-D_1\right)V_{IN}} \tag{41}$$

while the transformer ratio of turns of the proposed converter is

$$\frac{N_{S1}}{N_{P1}} = \frac{V_{O2}}{2D_2\left(1-D_2\right)V_{IN}}. \tag{42}$$

The relationship between the transistor conduction losses of the two converters is

$$\frac{P_2}{P_1} = \frac{4\beta\left(\frac{V_{IN}}{2-D_2}\right)^{2.5}\cdot I_O^2\left(\frac{N_{S1}}{N_{P1}}\right)^2\left[\frac{D_2\left(1-D_2\right)}{2-D_2}\right]}{2\beta\cdot V_{IN}^{2.5}\cdot I_O^2\left(\frac{N_S}{N_P}\right)\left[\sqrt{D_1}\left(1-D_1\right)+D_1\sqrt{1-D_1}\right]}. \tag{43}$$

Substituting (41) and (42) into (43) and making $D = D_1 = D_2$ and $V_O = V_{O1} = V_{O2}$ we find

$$\frac{P_2}{P_1} = \frac{4D\left(1-D\right)\left(2-D\right)}{\left(2-D\right)^{2.5}}. \tag{44}$$

Figure 22 shows the relationship between the conduction losses of the transistors of the two converters as a function of the duty cycle, for $D \le 0.5$. According to this result, in the worst case, which occurs when $D = 0.5$, the conduction losses in the active semiconductors are approximately equal to half of the similar losses that occur in the asymmetric HB-ZVS-PWM converter. Although the proposed converter uses three transistors, their conduction losses are lower because they are subjected to lower voltages, and consequently have lower conduction resistances. Therefore, with the use of appropriate power semiconductors, the efficiency of the proposed converter is higher than its asymmetric HB-ZVS-PWM counterpart.

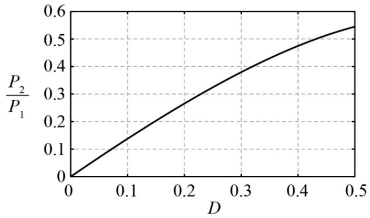


Fig.22. Relationship between the transistor conduction losses.

VI. CONCLUSIONS

A new topology of isolated ZVS-PWM DC-DC converter, with an LC filter in the output stage, which operation is based on the concept of a variable capacitor, was proposed. The variable capacitance is obtained with the use of two capacitors and three MOSFETS. The static gain as a function of the duty cycle and the external characteristics are similar to those of the asymmetric HB-ZVS-PWM converter [11], however with lower voltage stress on the power semiconductors.

The measured performance of an example 960 W dc-dc converter, with an input voltage of 400 V and output voltage of 48 V agreed well with theoretical predictions. The converter being studied is one more option available for design engineers of isolated DC-DC converters, with high power density and high efficiency.

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BIOGRAPHIES

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