CONFIGURATION 5S: A BI-DIRECTIONAL AC-DC CONVERTER

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***Abstract* – This paper proposes a bi-directional ac-dc converter to be applied in Energy-Control-Center (ECC) in order to interface dc variables, such as battery energy storage system and ac conventional utility grid. Such power electronic solution guarantees: (*i*) bi-directional power flow between dc and ac converter sides, (*ii*) independent control in both sides, (*iii*) high level of integration, and (*iv*) implementation of two functions using a unique power conversion stage. Despite proposing a new solution, this paper presents an analysis of the converter in terms of: PWM strategy, dc-link capacitor variables, switches variables, low-pass-filter specification employed at the output converter sides and a comparison with a conventional solution. Simulation and experimental results are presented as well.**

***Keywords* – Bi-directional Converter, Dc-ac Converter, Static Converter.**

I. INTRODUCTION

The concepts of micro-grid and nano-grid have been considered as interesting solutions, since they provide decentralized energy generations instead of large centralized facility operating alone. The main advantages of those solutions are [1]: (*i*) higher reliability, (*ii*) use of renewable energy with low pollution, which permits the plants to be near enough to the cities, (*iii*) reducing or eliminating the need for central dispatch, (*iv*) reducing the long-distance losses related to transmission lines, etc.

The implementation of the so called micro-grid and nano-grid is possible due to development reached by the power electronics field, and one important equipment in this scenario is the Energy-Control-Center (ECC), which is composed of a bi-directional ac-dc power converters used to interface the utility ac grid and either renewable energy sources or battery energy storage [2]. Figure 1 shows a typical application where the ECC can be employed. This device must deal with the interface between ac and dc universes with features such as independent control and soft-start at both converter sides. A direct solution of this device consists of a bi-directional dc-dc converter connected to an H-bridge converter through a dc-link capacitor, which means six power switches, as presented in [2].

Bi-directional power electronic converters with the ability to handle controlled voltage/current at both sides of converters are crucial in the scenario of distributed generation system [3],[9],[10], especially those ones with battery energy storage. The work presented in [4] brings a state-of-the-art of non isolated bi-directional dc-dc converters for applications in hybrid electric vehicles.

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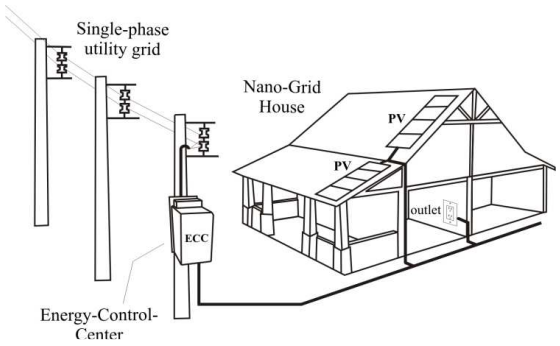


Fig. 1. Home nano-grid environment where the Configuration 5S can be applied.

In [5] was presented a bi-directional inverter that is connected in parallel to the utility system, operating as an Uninterruptible Power Supply. The configuration proposed in [6] can be used for both grid-connection and stand-alone modes with a single power processing stage and a high frequency link inverter. In [7] was proposed a dc-dc converter to be used in photovoltaic systems.

This paper proposes a bi-directional converter with five switches to be applied in applications in order to interface a dc and ac voltages, as observed in Figure 2. Such power electronic solution will be named as Configuration 5S and it guarantees: (*i*) bi-directional power flow between dc and ac converter sides, (*ii*) controllability in both sides, (*iii*) high level of integration, and (*iv*) implementation of two functions using an unique power conversion stage. The main advantage of this converter is the reduced switch count when compared to the conventional solution. Despite proposing a new solution, this paper presents a deep analysis of the converter in terms of: PWM strategy, dc-link capacitor variables, switches variables, low-pass-filter specification employed at the output converter sides and suitable control strategy. Simulation and experimental results are presented as well.

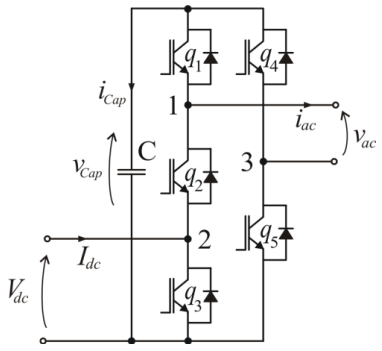


Fig. 2. Proposed converter: Configuration 5S.

II. DESCRIPTION OF THE PROPOSED CONVERTER

The proposed converter is composed of five power switches q_1, q_2, q_3, q_4 and q_5 arranged in only two legs. The first leg is constituted by three switches q_1, q_2 and q_3 while the second one is composed of only two switches q_4 and q_5. A binary variable is associated with each switch, i.e., $q_x = 1$ is used when the switch is closed, and $q_x = 0$ when the power switch is open, with $x = 1,2,3,4,5$. Notice that, as observed in the conventional converter (with two switches by leg), the switches in each leg cannot be turned on simultaneously, which will avoid a short-circuit through dc-link capacitor. In this sense, for the second leg, the switches q_4 and q_5 must be controlled in a complementary way. On the other hand, eight possible switching states could be obtained for the first leg, since there are three switches with two switching states each ($q_x = 1$ and $q_x = 0$). Many of these switching states are prohibited, as far as it means either a short-circuit, as mentioned before, or one of the unwanted switching states. For instance, when is trying to generate, at the same time, a positive voltage at point "2" (see Figure 2) and a negative voltage at point "1". Table I shows all possible states with the indication of no-prohibited ones, which are highlighted in the table. Those no-prohibited states (4, 6 and 7) of the first leg plus the well-known switching states of the second leg are employed to guarantee controlled variables at both ac and dc converter sides.

Figure 3 shows the equivalent circuits of the Configuration 5S, highlighting how each voltage has been obtained for both converter sides. For the dc side, just two values are possible $V_{dc} = 0$ [see Figs. 3(a)-3(d)] or $V_{dc} = V_{Cap}$ [see Figs. 3(e)-3(f)], while for the ac converter side three values are verified: $v_{ac} = 0$ [see Figs. 3(a), 3(d) and 3(f)], $v_{ac} = V_{Cap}$ [see Figs. 3(c) and 3(e)], or $v_{ac} = -V_{Cap}$ [see Figure 3(b)] which allows this side of the converter to be connected to the utility grid.

As far as this converter must generate waveforms with harmonic voltage limits at point-of-common coupling location, a PWM strategy and a low-pass-filter have been employed for this purpose, as discussed in the next sections.

TABLE I
Indication of prohibited switching states of the first leg (with switches q_1, q_2 and q_3).

States	q_1	q_2	q_3	Prohibited States
1	0	0	0	Yes
2	0	0	1	Yes
3	0	1	0	Yes
4	0	1	1	No
5	1	0	0	Yes
6	1	0	1	No
7	1	1	0	No
8	1	1	1	Yes

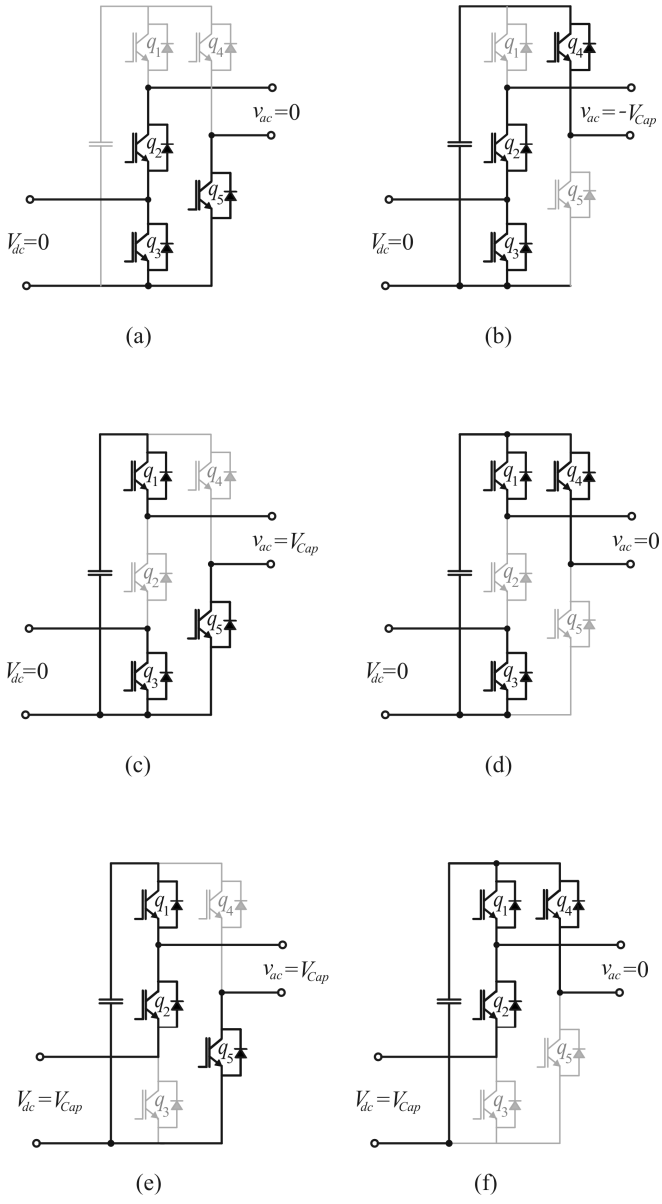


Fig. 3. Equivalent circuits of the Configuration 5S.

III. PWM TECHNIQUE

The gating signals of the switches must be obtained to avoid the prohibited states presented in Table I as well as to guarantee independent voltage control at both converter sides. Notice that all gating signals of switches employed in the Configuration 5S are obtained directly from the comparison of reference voltages v_{ac}^*, V_{dc}^* (and combination between them) with the triangular carrier wave, as observed in Figure 4. In this figure V_{ac}^* is the amplitude of the voltage v_{ac}^*.

The switch q_2 must be turned on when either q_1 or q_3 is open and must be turned off when both q_1 and q_3 are closed to avoid short-circuit of the source. To do so, an "exclusive or" logic (XOR) can be used, as in Figure 4. It is worth to mention that, in the leg with three switches is not possible to generate the voltage at point 1 (see Figure 2) at lower value than that at point 2, in the same way, it is not possible to pro-

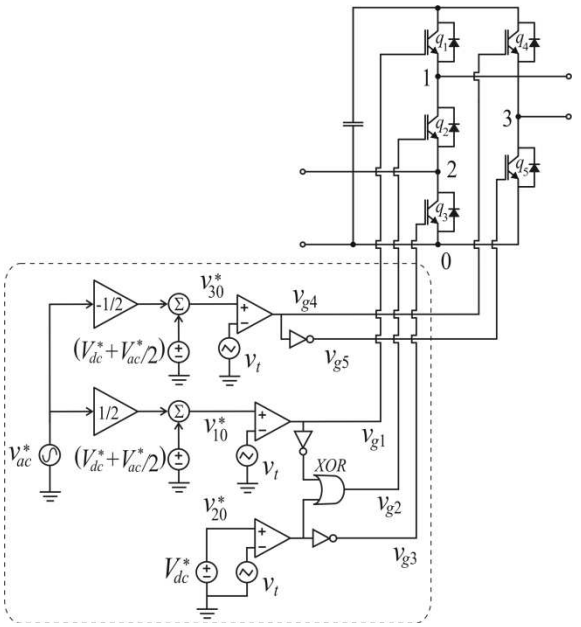


Fig. 4. PWM strategy.

duce a voltage at point 2 higher than that at point 1. This can be implemented just adding an offset value in the reference of the ac voltage, as done in Figure 4. The reference waveforms used in both legs, as well as the gating signals for each switch are presented in Figure 5, in this figure $V^*_{offset} = V^*_{dc} + V^*_{ac}/2$. To test the capability of Configuration 5S to generate independent and controlled ac and dc voltages, as well as to test the PWM strategy presented in Figure 4, a simple circuit has been considered, as observed in Figure 6(a). Figure 6(b) shows from top to bottom: v^*_{ac}, v_{ac}, v'_{ac}, V^*_{dc} and V'_{dc}; where v'_{ac} and V'_{dc}

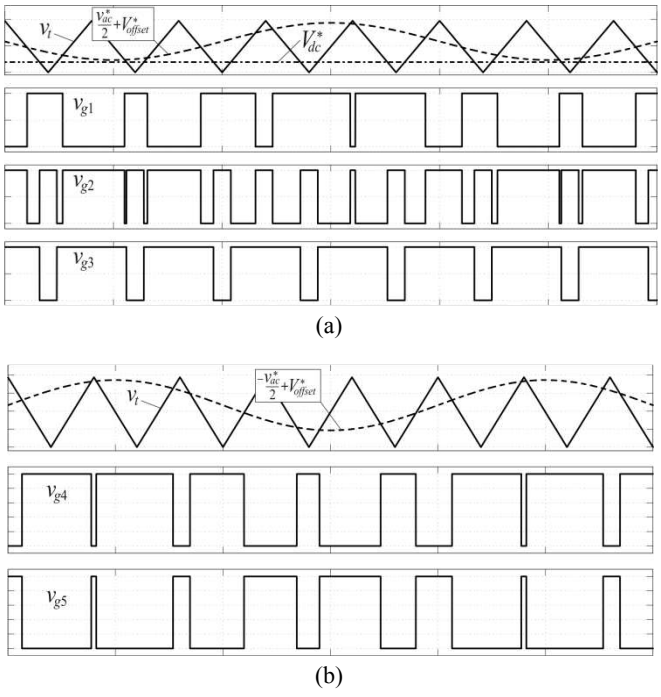
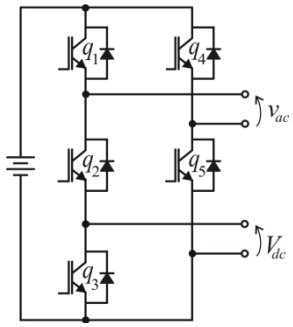
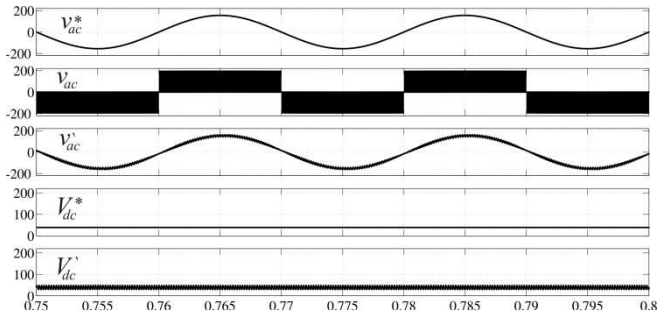


Fig. 5. Waveforms associated to: (a) the leg with three switches and (b) the leg with two switches.



(a)



(b)

Fig. 6. (a) Circuit used to test the PWM strategy. (b) Waveforms generated at ac and dc converter sides.

are the output variables of the low-pass-filter applied to v_{ac} and V_{dc}, respectively.

These filters have been used to avoid a high-frequency components presented on the voltages (v_{ac} and V_{dc}), and to make it clear that the waveforms (v'_{ac} and V'_{dc}) in fact follow their references v^*_{ac} and V^*_{dc}. In such results the amplitude of v^*_{ac} and V^*_{dc} are set to be $180V$ and $40V$, respectively. In the next section, it will be presented details about the low-pass-filters placed at outputs of the Configuration 5S to able it to be connected as grid interface converter.

IV. LOW-PASS-FILTER SPECIFICATION

Figure 7 shows the position in which low-pass-filters must be placed in the proposed converter, aiming to reduce the switching frequency ripple while achieve rapid dynamic response and good stability margin, as discussed in [8].

A. Low-Pass-Filter at ac converter side - LPF_{ac}

Figure 8 shows three options for the implementation of LPF_{ac}. Notice that the filters presented in Figs. 8(a) and 8(b) can be considered as particular cases of the LCL filter showed in Figure 8(c). For instance, L-filter type is the LCL-filter with $C_f = R_2 = L_2 = 0$. In this sense, the complete math development will be done for the LCL filter, and the other cases can be obtained directly from the LCL filter.

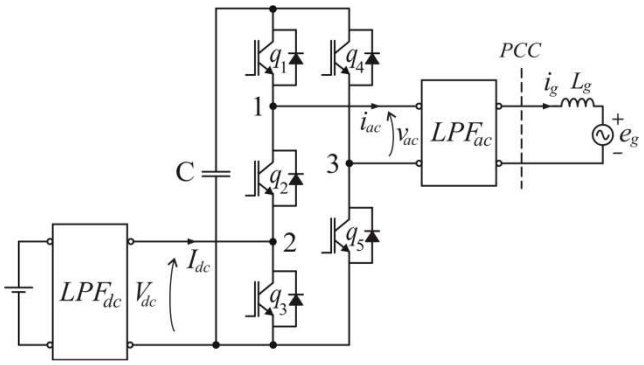


Fig. 7. Positioning of the low-pass filters.

By using Kirchhoff's law for the circuit depicted in Figure 8(c), it yields

$$i_{ac} - i_c - i_g = 0 \quad (1)$$

$$v_{ac} - v_c = i_{ac}(R_1 + sL_1) \quad (2)$$

$$v_c - e_g = i_g[(R_2 + R_g) + s(L_2 + L_g)] \quad (3)$$

$$v_c = i_c(\frac{1}{sC_f} + R_c) \quad (4)$$

Considering (1)-(4) it is possible to establish the block diagram of the LCL filter as depicted in Figure 9, which will be used for the analysis with the help of Bode Diagrams, as presented in the sequence.

Considering the grid as an ideal voltage source, i.e., it represents a short circuit for harmonic frequencies. The transfer function of the LCL filter is given by

$$\frac{i_g}{v_{ac}} = \frac{1+sR_cC_f}{s^3\alpha+s^2\beta+s\chi+\delta} \quad (5)$$

where $\alpha = (L_g + L_2)L_1C_f$,

$\beta = C_f((L_g + L_2)(R_c + R_1) + L_1(R_c + R_g + R_2))$

$\chi = L_g + L_2 + L_1 + C_f(R_c(R_g + R_2) + R_cR_1 + (R_g + R_2)R_1)$

and $\delta = R_g + R_2 + R_1$.

The demonstration of the equation (5) is furnished in Appendix. Figure 10 presents the Bode Diagram showing the influence of the filter type applied to the proposed converter. Notice that, the LCL and LC filters have almost the same behavior, which are both much better than that observed for the L-type filter. On the other hand, the LCL filter presents a drawback related to the attenuation in low frequencies, which means in practical aspects more voltage at dc-link capacitor to generate the desired level of ac voltage.

Table II shows the parameters used to test the different filters presented in Figure 8. For all cases, the line parameters are $L_g = 2mH$ and $R_g = 0.1\Omega$.

Figure 10 presents an important figure of merit for the choose of the low-pass-filter to be used in the Configuration 5S, but it is not enough. Other points must be considered in this analysis, for instance, the influence of line parameters variation, as depicted in Figs. 11 and 12.

Figure 11 shows how the L_g parameter can change the performance of the low-pass-filter for the LC-type filter.

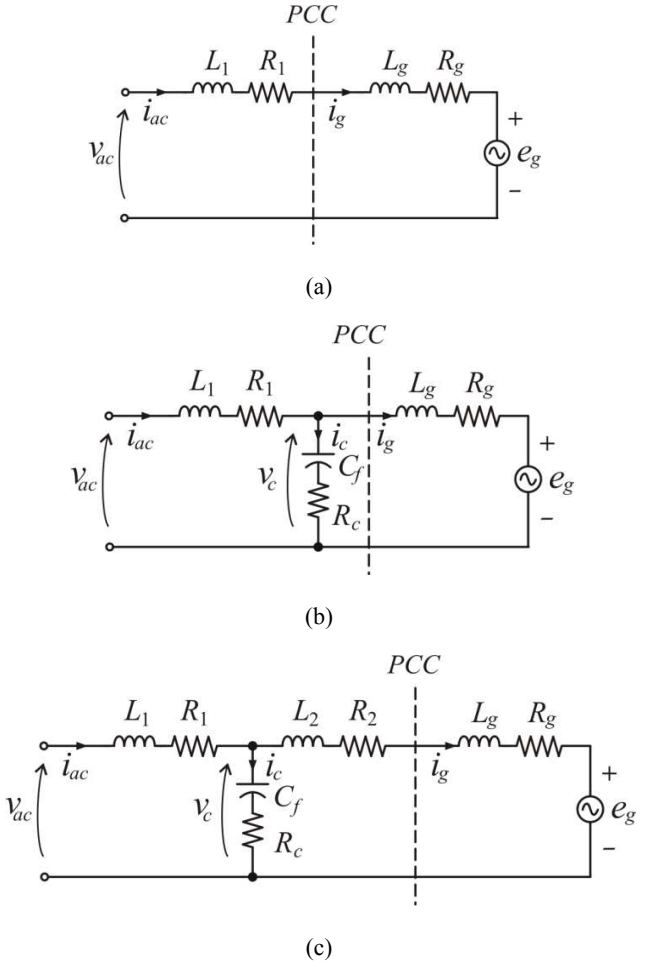


Fig. 8. Three options of LPF: (a) L-type filter, (b) LC-type filter, and (c) LCL-type filter.

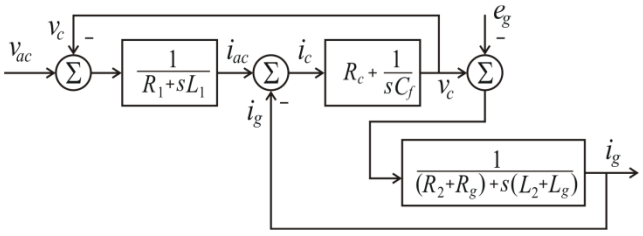


Fig. 9. Block diagram of the LCL filter.

On the other hand, LCL-type filter performance practically does not change considering the same variation of L_g, as observed in Figure 12.

B. Low-Pass-Filter at dc converter side - LPF_{dc}

Considering the filters presented in Figure 8 and the specific demand of the dc side, the LCL filter presents lesser interest compared to L and LC filters, since it has zero-frequency attenuation higher than that other ones.

TABLE II
Parameters used for the filters test.

L-Type	LC-Type	LCL-Type
$L_{1f} = 1mH$	$L_{1f} = 1mH$	$L_{1f} = L_{2f} = 1mH$
$R_{1f} = 0.05\Omega$	$R_{1f} = 0.05\Omega$	$R_{1f} = R_{2f} = 0.05\Omega$
	$C_f = 45\mu F$	$C_f = 45\mu F$
	$R_c = 1\Omega$	$R_c = 1\Omega$

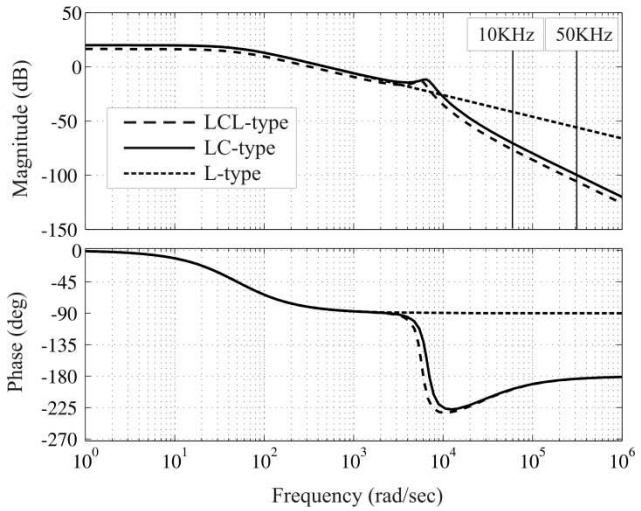


Fig. 10. Bode diagram showing the influence of the filter type.

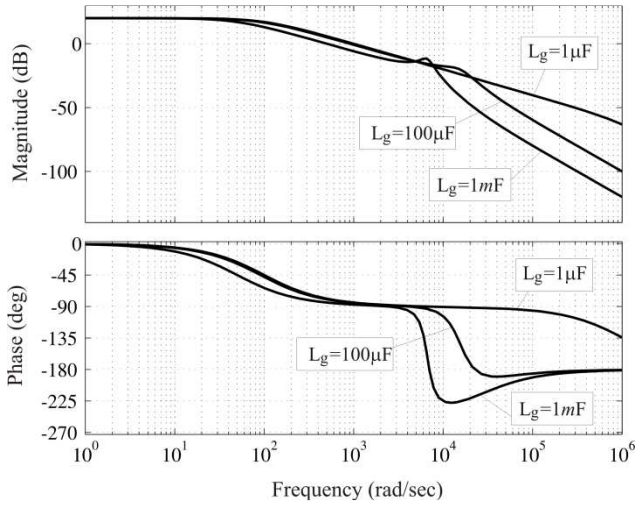


Fig. 11. Bode diagram showing the influence of L_g for LC filter.

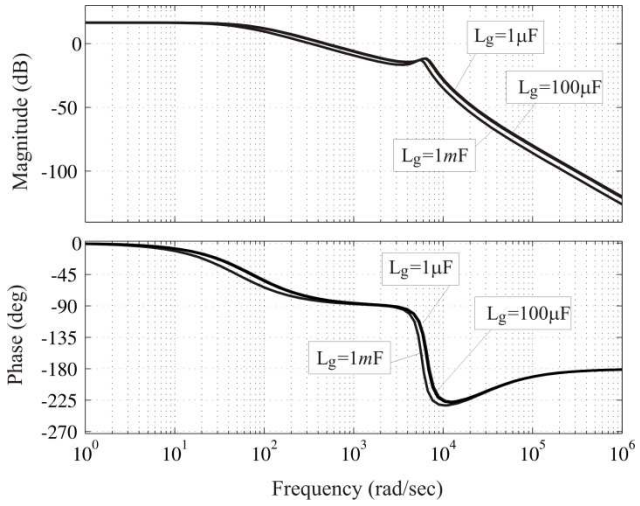


Fig. 12. Bode diagram showing the influence of L_g for LCL filter.

V. CONFIGURATION 5S – SPECIFICATION

In this section the variables related to both dc-link capacitor and switches are specified in terms of power delivered, power consumed and reference voltages.

A. Dc-link Capacitor Variables

The dc-link capacitor current (i_{Cap}) can be written as follows:

$$i_{Cap} = q_1 q_2 I_{dc} + (q_4 - q_1) i_{ac} \tag{6}$$

where $q_1 q_2 = \bar{q}_3$ is the variable that indicates when the switch q_3 is turned off, which yields

$$i_{Cap} = \bar{q}_3 I_{dc} + (q_4 - q_1) i_{ac} \tag{7}$$

where $q_1 = v_{10}^*/V_{Cap}^*$, $q_4 = v_{30}^*/V_{Cap}^*$ and $\bar{q}_3 = v_{20}^*/V_{Cap}^*$, then it turns out that

$$i_{Cap} = (P_{dc} - p_{ac})/V_{dc}^* \tag{8}$$

The required capacitor voltage is specified in terms of the desired voltages, as follows

$$V_{Cap}^* = v_{ac}^* + V_{dc}^* \tag{9}$$

B. Switches Variables

The blocking voltage processed by each switch is equal to the dc-link voltage. On the other hand, the currents following through the switches are given in Table III. In this table EC means equivalent circuits as presented in Figure 3.

TABLE III
Current in the switches.

EC	q_1	q_2	q_3	q_4	q_5
Fig. 3(a)	0	$-i_{ac}$	$-i_{ac}+I_{dc}$	0	i_{ac}
Fig. 3(b)	0	$-i_{ac}$	$-i_{ac}+I_{dc}$	$-i_{ac}$	0
Fig. 3(c)	i_{ac}	0	I_{dc}	0	i_{ac}
Fig. 3(d)	i_{ac}	0	I_{dc}	$-i_{ac}$	0
Fig. 3(e)	$i_{ac}-I_{dc}$	$-I_{dc}$	0	0	i_{ac}
Fig. 3(f)	$i_{ac}-I_{dc}$	$-I_{dc}$	0	$-i_{ac}$	0

VI. COMPARISON WITH CONVENTIONAL SOLUTION

In this section will be presented a comparison in terms of the current and voltage ratings of the switches used in the conventional (see Figure 13) and proposed solutions. Notice that, both solutions present the same functionality, i.e., bi-directional power flow and independent control at ac and dc outputs.

A direct comparison of the proposed and conventional circuits reveals a reduction of one power switch as an advantage for the proposed converter, as well as the reduction of its drive circuitry to generate the gating signal.

As mentioned before, all switches of the proposed topology presents the same blocking voltage, given by (9). On the other hand, the blocking voltage of the conventional topology presented in Figure 13 is given by either v_{ac}^{*} or V_{dc}^{*}. In terms of the currents flowing through the switches, it turns out that, for the conventional configuration, four switches (q_2, $\overline{q_2}$, q_3, $\overline{q_3}$) deal with i_{ac}, while two switches (q_1, $\overline{q_1}$) deal with I_{dc}. Comparing this verification with the information observed in Table III, it implies a slight disadvantage for the proposed configuration, since the switches q_1 and q_3 will deal with $i_{ac}-I_{dc}$ and $-i_{ac}+I_{dc}$, respectively. In this sense, two power switches in the proposed solution must be redesigned in terms of current ratings. It is worth to mention that, even considering that, the proposed and conventional solution have almost the same efficiency, basically due to the reduction of one switch, which compensates the current redesign of switches q_1 and q_3, and voltage redesign of the switches employed in the conventional circuit.

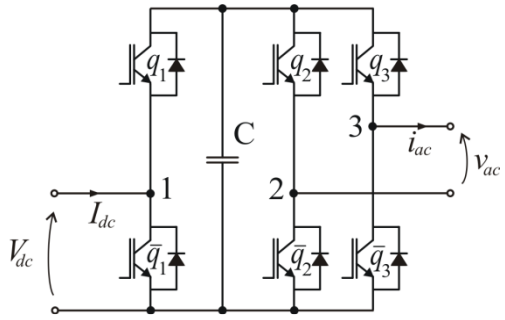
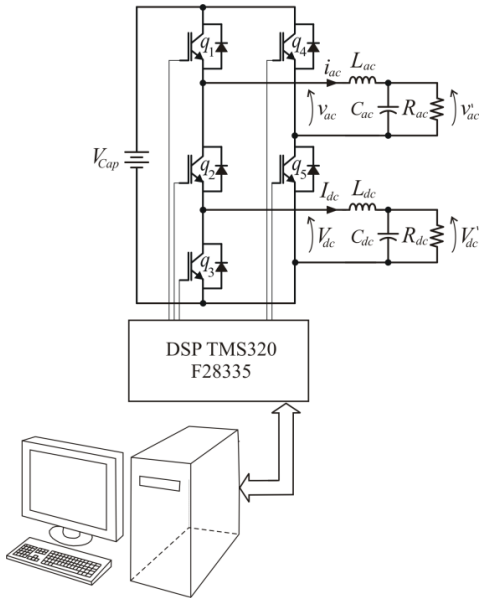


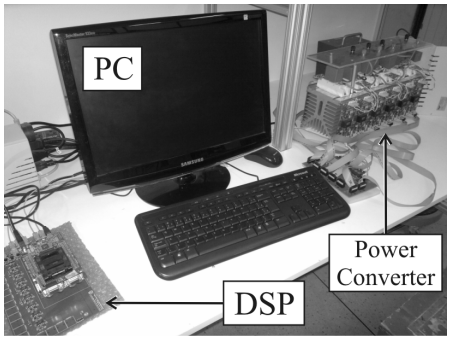
Fig. 13. Conventional grid interface converter presented in [2].

VII. SIMULATED AND EXPERIMENTAL RESULTS

The proposed converter has been implemented with PSIM software as well as in the laboratory setup for validation procedures. Figure 14(a) shows the electrical circuit employed in the experimental setup, with the power switches being controlled by DSP TMS320F28335. Figure 14(b) depicts a photo of the whole system, while Figure 14(c) shows a detailed view of the converter.



(a)



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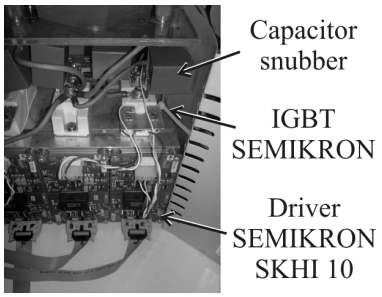

(c)

Fig. 14. (a) Electrical circuit employed in the experimental setup. (b) Photo of the experimental setup. (c) Power converter details.

The data used to obtain the results are: *i*) $V_{Cap} = 100V$, *ii*) $L_{ac} = L_{dc} = 2mH$, *iii*) $C_{dc} = 2200\mu F$, *iv*) $C_{ac} = 450\mu F$, *v*) $R_{ac} = R_{dc} = 19.5\Omega$, and *vi*) $V_{dc}^{*} = 30V$, $V_{ac}^{*} = 60V$.

The simulation results presented in Figure 15 shows the variables associated with ac and dc sides of the converter, i.e. from top to bottom, voltage at the inductor L_{dc} (v_{Ldc}), output voltage at dc side after the dc filter ($V_{dc}^{'}$), output voltage at ac side before the ac filter (v_{ac}) and ac current i_{ac}.

Figure 16 shows the voltages of the five switches q_1-q_5 of the Configuration 5S, as expected from the theoretical studies, all of them have the same blocking voltage. To demonstrate the independent output control at ac and dc converter sides, Figure 17 shows the currents i_{ac} and $I_{dc}$with a step transient of I_{dc}, even considering this scenario with a hard transient of I_{dc}, the current i_{ac} is not affected by that.

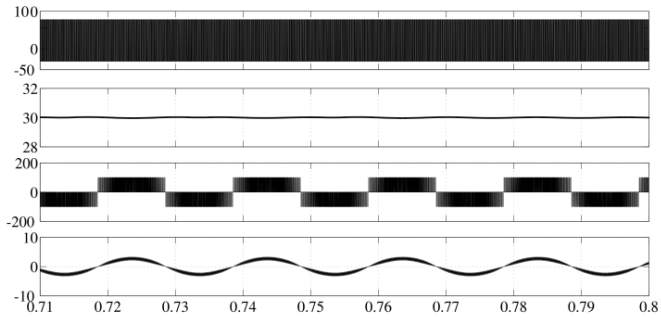

Fig. 15. Simulated results: (from top to bottom) v_{Ldc}, V_{dc}', v_{ac} and i_{ac}.

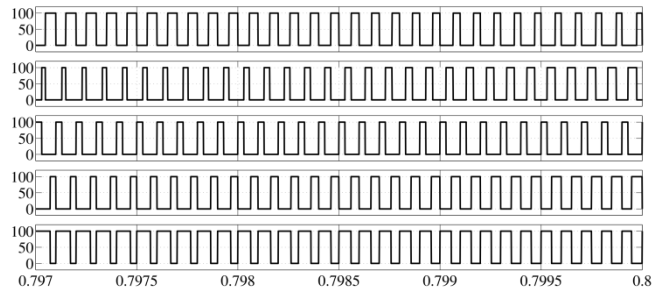

Fig. 16. Simulated results of the voltages of switches q_1-q_5.

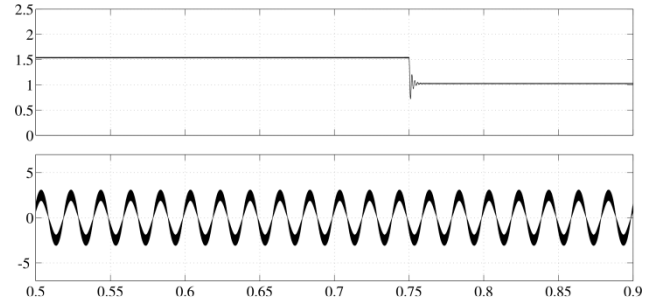

Fig. 17. Simulated results: (top) I_{dc} and (bottom) i_{ac} with a step transient of I_{dc}.

The experimental outcomes presented in Figure 18 shows the variables associated with ac and dc sides of the converter, i.e. from top to bottom, voltage at the inductor L_{dc} (v_{Ldc}), output voltage at dc side after the dc filter (V_{dc}'), output voltage at ac side before the ac filter (v_{ac}) and ac current (i_{ac}).

Using the average function of the oscilloscope, the same set of experimental results is depicted in Figure 19. Notice that v_{Ldc} is not showed in this figure since its medium value is zero. Figure 20 depicts the gating signals of the switches q_1, q_2 and q_3, while Figure 21 shows gating signals of the switches q_4 and q_5.

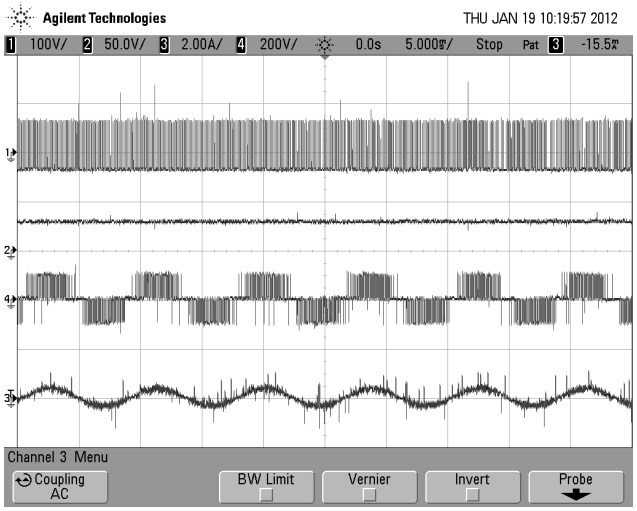

Fig. 18. Experimental results: (from top to bottom) v_{Ldc}, V_{dc}', v_{ac} and i_{ac}.

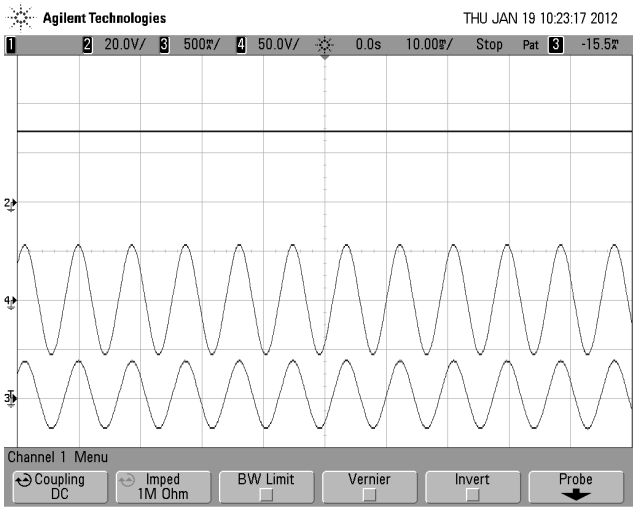

Fig. 19. Experimental results: (from top to bottom) V_{dc}', v_{ac} and i_{ac} with average function of the oscilloscope.

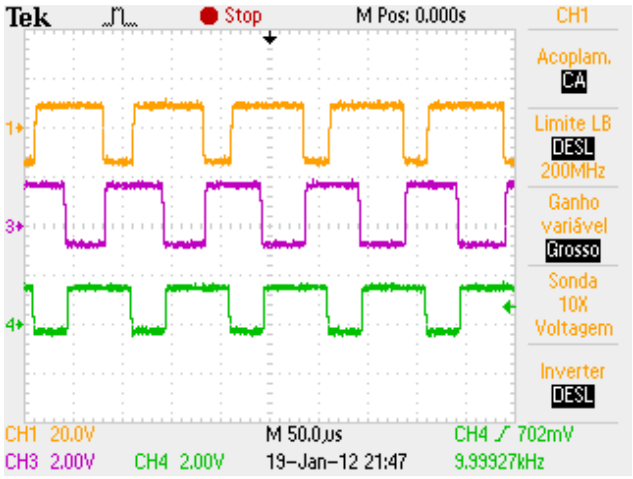

Fig. 20. Experimental results: (from top to bottom) v_{g1}, v_{g2} and v_{g3}. (20*V*/*div* for all channels)

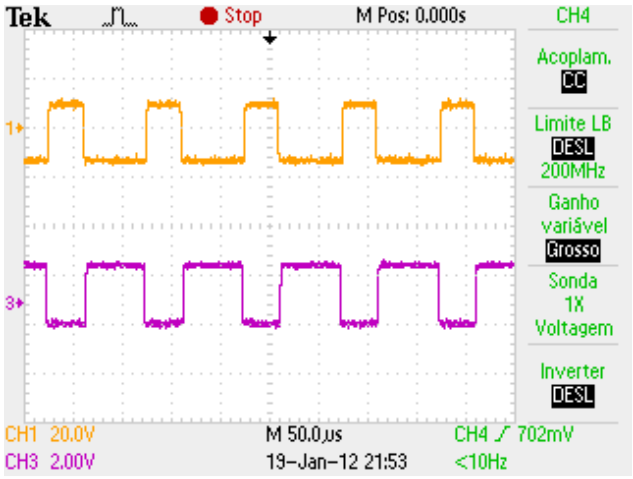

Fig. 21. Experimental results: (from top to bottom) v_{g4} and v_{g5}. (20*V*/*div* for both channels)

Another set of outcomes are presented in Figures 22 and 23. These figures aim to show the ability of the proposed converter to handle bidirectional power flow among three different elements (B1, B2 and R) connected through the configuration 5S, where B1 (100V) and B2 (12V) are batteries and R (12Ω) is a resistive load. Figure 22 depicts the ways of power flow considering three different scenarios: (*i*) the energy going from B1 to both B2 and R, see Figure 22(a); (*ii*) the energy going from B2 to R, see Figure 22(b); and (*iii*) the energy going from B2 to both B1 and R, see Figure 22(c).

Figure 23 (top) shows the current control needed to guarantee those scenarios observed in Figure 22, while Figure 23 (bottom) shows the values of powers P_R, P_{B1} and P_{B2}, in which positive value of P_{B1} means energy generated and positive values of P_R and P_{B2} mean energy consumed. Hence, until $t = 0.75s$, since a positive current is imposed in B2, the energy generated by B1 is consumed by B2 and R. From $t = 0.75s$ to $t = 1.5s$ all energy consumed by R is furnished by B2. After $t = 1.5s$, due to the higher negative value of I_{dc} the excess of energy goes back to B1, since B2 is generating more energy than that consumed by R.

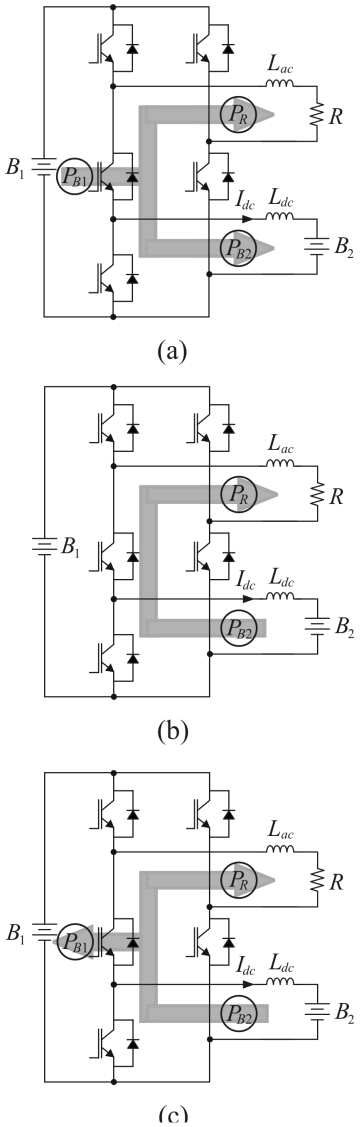

Fig. 22. Power flow among elements: (a) energy generated by B1 is consumed by B2 and R, (b) energy consumed by R is furnished by B2, (c) B2 generates energy to both R and B1.

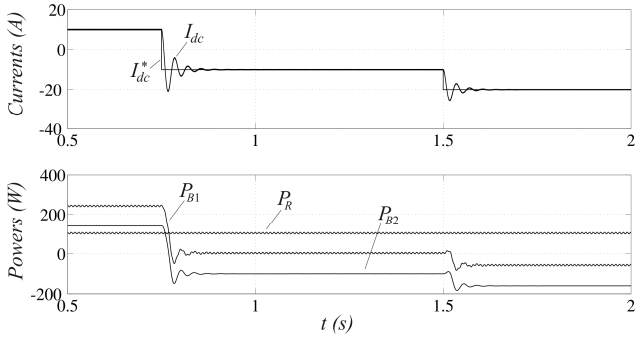

Fig. 23. (top) Current control applied to B1. (bottom) Power flow among the elements.

VIII. CONCLUSION

This paper proposes a bi-directional ac-dc converter with five power switches, which was named as Configuration 5S. The Energy-Control-Center (ECC) is one possible application of this topology, since it can be applied to interface dc variables, such as battery energy storage, and ac variables, such as conventional utility grid. Such power electronic solution guarantees: (*i*) bi-directional power flow between dc and ac converter sides, (*ii*) controllability in both sides, (*iii*) high level of integration, and (*iv*) implementation of two stages (dc-dc and dc-ac) using a unique power conversion stage. The main points treated throughout the paper were: description of the converter (Section II), PWM strategy (Section III), filter specification (Section IV), specification of the converter (Section V), comparison (Section VI) and selected outcomes (Section VII). As advantages of this converter, it is possible to sort: high level of integration with a single converter implementing two stages (ac and dc) and the same functionality of the conventional solution, but with the elimination of one power switch and its drive circuitry. As disadvantage, the power switches of the Configuration 5S must be redesigned, when compared to the conventional topology.

APPENDIX

The demonstration of equation (5) follows in the sequence. Considering (3) and (4) and admitting that for the filter analysis e_g it is set to be zero, it yields:

$$i_g\left[\left(R_2 + R_g\right) + \mathrm{s}\left(L_2 + L_g\right)\right] = i_c\left(\frac{1}{\mathrm{sC_f}} + R_c\right) \qquad (10)$$

$$i_c = i_g \frac{s^2 C_f\left(L_2+L_g\right)+sC_f\left(R_2+R_g\right)}{sC_f R_c+1} \qquad (11)$$

Equation (2) can be written as

$$v_{ac} = v_c + i_{ac}(R_1 + sL_1) \qquad (12)$$

Substituting (4) and (1) in (12), it turns out that

$$v_{ac} = -i_c\left(\frac{1}{\mathrm{sC_f}} + R_c\right) + (i_c + i_g)(R_1 + sL_1) \qquad (13)$$

Considering (11) in (13) it is possible to determine directly the equation (5).

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BIOGRAPHY

Euzeli Cipriano dos Santos Junior received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Federal University of Campina Grande, Campina Grande, Brazil, in 2004, 2005, and 2007, respectively. From 2006 to 2007, he was a Visiting Scholar with Electric Machines and Power Electronics Laboratory, Texas A&M University, College Station. From August 2006 to March 2009, he was a Professor at the Federal Center of Technological Education of Paraiba, Brazil. From December 2010 to March 2011, he was a Visiting Professor at the University of Siegen, Germany, sponsored by DAAD/CAPES. Since March 2009, he has been with the Department of Electrical Engineering, Federal University of Campina Grande, where he is currently Professor of Electrical Engineering. His research interests include power electronics and electrical drives. Since 2010 he is the IEEE Student Branch Counselor of the UFCG.