SOME DESIGN CONSIDERATIONS FOR HIGH-POWER HIGH-VOLTAGE DC/DC CONVERTER WITH IMPROVED POWER DENSITY AND EFFICIENCY

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***Abstract* – This paper presents the findings of a R&D project connected to the development of 50 kW auxiliary power supply for the high-voltage DC-fed commuter trains. The aim was to design a new-generation power converter utilizing high-voltage IGBT modules, which can outpace the predecessor (6.5 kV IGBT based two-level half-bridge DC/DC converter) in terms of power density, i.e. to provide more power for smaller volumetric space. The topology proposed is 3.3 kV IGBT based three-level neutral point clamped half-bridge with the high-frequency isolation transformer and the current doubler rectifier that fulfils all the targets imposed by the designers. Despite an increased component count the proposed converter is very simple in design and operation. The paper provides an overview of the design with several recommendations and guidelines as well as the feasibility and performance comparison of the proposed converter with the 6.5 kV IGBT based two-level half-bridge DC/DC converter.**

***Keywords* - high-power DC/DC converter, rolling stock, high-voltage IGBTs, three-level inverter, current doubler rectifier, cost-effectiveness, assembly.**

I. INTRODUCTION

Electric traction is one of the major present-day solutions for environmental problems. Electric traction is safe, economical, reliable and with a minimum environmental impact. The latest demands for energy efficient, reliable and safe rolling stock require new technologies for the design of power electronic converters in the railway applications. The auxiliary power supply converter (APS) is one of the basic systems used in rolling stock. It provides low-voltage power to every onboard electrical system and equipment on a rail vehicle, including those that are critical to its safety and operability (like brakes or lighting systems). In brief, APS represents a step-down DC/DC converter, transforming high voltage (HV) from the traction catenary (3.0 kV DC in the case of a high-voltage DC catenary) to a lower voltage (350 V DC) for the onboard electric facilities. It is obvious that a failure within this system would render the whole vehicle non-operational, resulting in a financial loss, operational problems to the rolling stock owner and discomfort to passengers.

Regarding to the specific design rule, converters based on the IGBT technology for the catenary voltages of 3.0 kV DC are only possible with IGBTs with the blocking voltage not lower than 6.0 kV. The 6.5 kV IGBT modules (EUPEC, ABB, IXYS, DYNEX, etc.) recently implemented are basically designed for 3.0 kV DC rolling stock applications with their high demands on reliability concerning thermal cycling capability. Single HV IGBT has the voltage blocking capability two times the nominal catenary voltage level, which copes with the requirements for the rolling stock power electronics. Such transistors offer an attractive possibility to avoid series connection of IGBTs (for proper blocking voltage), providing higher efficiency, power density and reliability than the combined HV switch designs. Thus, the concept of 50 kW rolling stock APS was developed and implemented at the Department of Electrical Drives and Power Electronics of Tallinn University of Technology in 2007. Based on two-level half-bridge topology with state-of-the-art 6.5 kV IGBTs, the APS has shown an outstanding performance as well as light weight and excellent compactness [1].

The most serious problem reported is a high power dissipation and limited switching frequency (up to 1 kHz) of 6.5 kV IGBTs. All these factors limit the efficiency of a power converter at 90-92%. In addition, the feasibility issue was raised: single 6.5 kV IGBT based converters provide excellent reliability due to minimal required component number, but the high manufacturing costs and enormous market prices for 6.5 kV IGBTs kill all of their benefits. To improve the efficiency and feasibility of the high-voltage IGBT based APS it is proposed to implement the three-level neutral point clamped (NPC) half-bridge topology with 3.3 kV dual IGBT modules (figure 1).

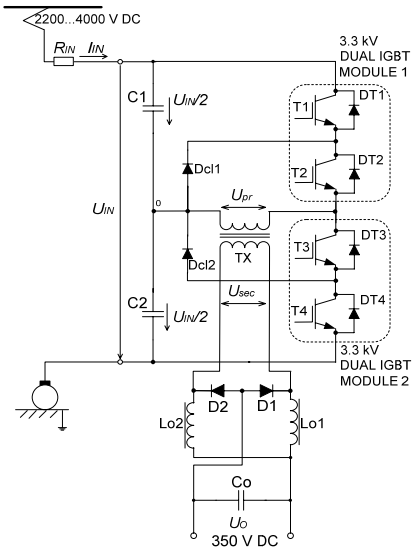

Fig. 1. Proposed three-level NPC half-bridge DC/DC converter topology with a current doubler rectifier.

As is seen from figure 1, the three-level NPC half-bridge topology can be easily derived from the two-level half-bridge

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topology with series connected transistors by the introduction of clamping diodes Dcl1 and Dcl2, which balance out voltage sharing between series connected top and bottom side transistors.

The three-level half-bridge DC/DC converters have been analyzed and discussed in [2-7], but these investigations were mostly connected with low power (≤ 8 kW) low-to-middle voltage (≤ 1.3 kV) applications. In this paper, first the three-level half-bridge isolated DC/DC converter topology will be evaluated for high-voltage (≥ 2 kV) high-power (≥ 10 kW) applications.

II. DESIGN AND OPERATION OF THE PROPOSED CONVERTER

The key specific feature of the catenary-fed rolling stock converters is that they must operate normally despite the widely changing input voltage. The boundaries of the input voltage are presented in Table 1 (minimal and maximal input voltages). In the normal steady-state operation of the transformer-isolated half-bridge converter, the relation $U_{in}D$ (where U_{in} is the input voltage and $D=t_{on}/T_{sw}$ is the transistor duty cycle) is constant. In converters with wide input voltage variations, to provide constant volt-seconds over the primary winding of the isolation transformer, the maximum duty cycle D_{max} must always be associated with the minimal input voltage $U_{in,min}$ and the minimum duty cycle D_{min} must correspond to the maximal input voltage $U_{in,max}$. The input voltages and the corresponding duty cycles of the developed converter are presented in Table 1. Further analysis will mostly be based on these boundary operating points.

TABLE 1
Converter input voltages and corresponding duty cycles

Input voltage	$U_{in,min}$	$U_{in,max}$
	2.2 kV DC	4.0 kV DC
Duty cycle	D_{max}	D_{min}
	0.4	0.22

A. Three-level half-bridge NPC inverter

The operation of a three-level half-bridge NPC inverter can be divided to four operating modes - two conduction and two freewheeling modes. The first - the positive conduction mode - operates when T1 and T2 are on and T3 and T4 are off. In that mode the current flows from the catenary and through transistors T1, T2, the isolation transformer TX, and the capacitor C2. The second mode - the positive freewheeling mode - when T1 and T4 are off, T2 and T3 are on and Dcl1 is conducting. This mode is followed by the negative conduction mode (T1 and T2 are off and T3 and T4 are on) and the negative freewheeling mode (T1 and T4 are off, T2 and T3 are on and Dcl2 is conducting). The timing diagrams of inverter switches and resulting primary voltage waveforms of the isolation transformer in different operating points are presented in figure 2.

Neglecting losses and transients, the operating conditions of the inverter switches in the three-level configuration could be described as:

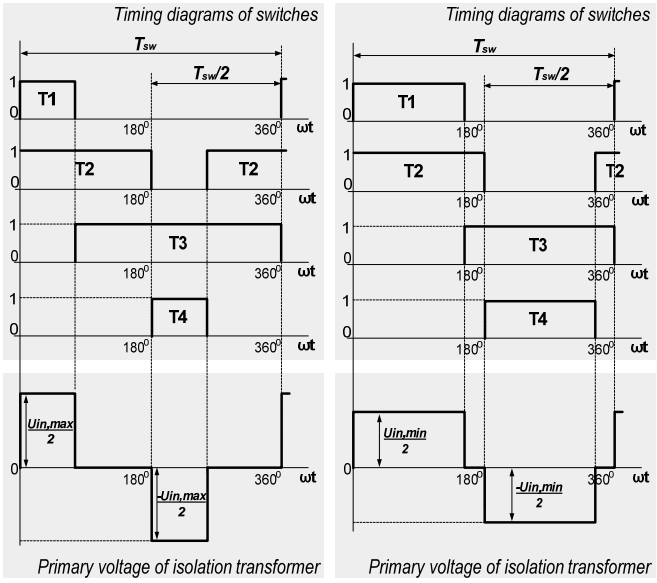
$$U_{CE,\max} = \frac{U_{in,\max}}{2}. \quad (1)$$

$$I_{C,\max} = \frac{P_O}{U_{in,\min} \cdot D_{\max}}. \quad (2)$$

Where:

$U_{CE,max}$ - Maximal collector-emitter voltage of the transistor.
$I_{C,max}$ - Maximal collector current.
$U_{in,max}$ - Maximal input voltage of the converter.
$U_{in,min}$ - Minimal input voltage of the converter.
D_{max} - Maximum duty cycle of the transistor.
P_O - Output power of the converter.

Thus, each transistor in the three-level NPC topology is operating with half the input voltage and the same collector current as with the conventional two-level topology. This fact provides a possibility of faster 3.3 kV IGBT modules to be implemented, thus achieving higher power density of the converter (reduced heatsink requirements due to lower losses for the same switching frequency or reduced passive components due to increased switching frequency).



(a) (b)

Fig. 2. Timing diagrams of switches of the proposed three-level half-bridge NPC inverter and resulting primary voltage waveforms of the isolation transformer: at maximal (a) and minimal (b) input voltages.

Theoretically, to control a three-level inverter, four PWM generators are needed. The proposed external logic circuit presented in figure 3 allows the required number of independent PWM channels to be effectively reduced by two in cases of symmetric PWM control. The control is made very easy: outer transistors T1 and T4 are controlled directly from the PWM generators of a microcontroller, while inner switches T3 and T2 are drived by the inversions of the corresponding control PWM signals. These inversions are derived by the external inverter logic (NOT gate) realized by the logic IC - 74HT04 HEX inverter.

Since the IGBTs are not ideal switches and have a certain turn-on and turn-off delay times, a situation can occur where three devices T1, T2, T3 or T2, T3, and T4 are simultaneously conducting. Having three devices conducting at the same time would result in the short circuit of the corresponding input capacitor C1 or C2 and the IGBTs

would be destroyed. In order to prevent short circuit, it is necessary to add a dead time t_d between the original and the inverted PWM signal, as shown in figure 3. A control pulse from the microcontroller sets the pin PWM1 high and the capacitor C1 will be charged over resistors R1 and R2. The comparator compares that voltage with its reference voltage and toggles the output if the reference voltage has been reached. If the PWM signal returns to low, then the capacitor C1 will be discharged over the diode D1 and the comparator toggles the output back to zero. The same dead time generator is implemented for the inverted control channel as well.

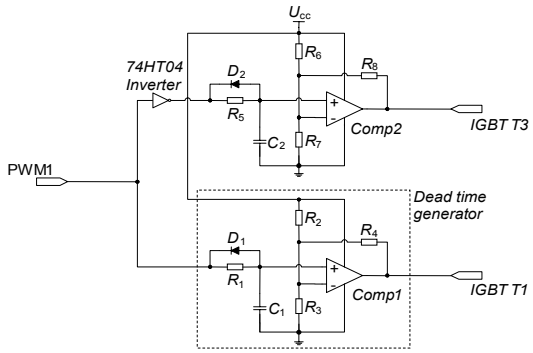


Fig. 3. Proposed control signal inverter circuit with an integrated dead time generator.

Figure 4 shows the experimental waveforms of collector-emitter voltages (500 V/div) of the top-side transistors T1 and T2. The switching frequency of transistors is 2 kHz. The input voltage of converter is 2.2 kV and the operating duty cycle 0.4.

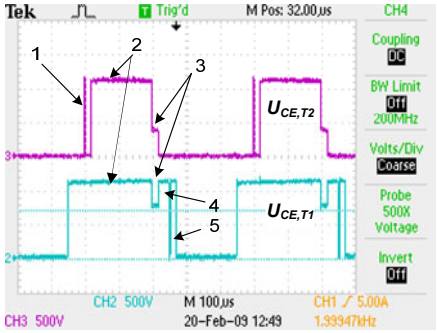


Fig. 4. Experimental waveforms of collector-emitter voltages of the top-side transistors T1 and T2 at input voltage 2.2 kV and duty cycle 0.4.

The switching transients presented in figure 4 mostly depend on operating conditions and component properties and according to labels 1...5 in figure 4 could be generally described as follows:

Label 1 - when transistor T2 is turned off, the leakage inductance of the transformer primary winding draws the current through freewheeling diodes DT3 and DT4. During that period a voltage peak occurs on the transistor T2.

Label 2 - the bottom-side transistors are conducting and full input voltage is evenly shared between the top-side transistors T1 and T2.

Label 3 - the outer transistor T4 is turned off and clamping diode Dcl2 starts to conduct. Instead of full input voltage now only half of the value is applied to the top-side transistors. The voltage sharing between transistors T1 and T2 in this time instant can be clearly seen in figure 4 (referred to as "3").

Label 4 - after the dead time transistor T2 is turned on and its collector-emitter voltage drops to zero. The voltage across T1 increases to half of the input voltage.

Label 5 - transistor T3 is turned off and the leakage inductance of the transformer primary pushes the current through freewheeling diodes DT1 and DT2. The voltage across T1 drops to zero. After the transformer leakage energy has been utilized the voltage across T1 increases to its previous value. Practically, by increasing the transformer leakage inductance and/or decreasing dead time the zero-voltage switching (ZVS) can be achieved for outer transistors T1 and T4 [8].

B. Isolation transformer and current doubler rectifier

To further improve the power density of the APS it was decided to implement the current doubler rectifier (CDR) on the output stage of the converter (figure 1). The main problems of the full-bridge rectifier (FBR) used in the previous design [1] were the increased losses of the transformer secondary winding due to high secondary current and the very high conduction losses of the rectifier bridge caused by the current having to go through two diodes in each half-cycle.

In contrast to the full-bridge rectifier, the current doubler topology inhibits several advantages: the total volume of the two filter inductors might be equal or even smaller than the inductor of the full-bridge due to their lower operating frequency and lower current ratings [9, 10]. Further tradeoffs can be made in order to reduce inductor sizes by lowering the inductance value and relying more strongly on the ripple current cancellation effect of the two inductors. Additionally, the current-doubler rectifier offers a potential benefit of better distributed power dissipation, which might become a vital benefit for the APS converters in terms of power density. The filter inductances can be estimated by (3).

$$L_{O1} = L_{O2} = \frac{U_O \cdot (1-D)}{\Delta I_L \cdot f_{sw}}. \qquad (3)$$

Where:

U_O - Output voltage of the converter.
D - Operating duty cycle of the converter.
ΔI_L - Output inductor ripple current.
f_{sw} - Switching frequency of the converter.

In cases of electrolytic capacitors, the value of capacitance could be evaluated as:

$$C_O = \frac{80 \cdot 10^{-6} \cdot \Delta I_L}{\Delta U_O}. \qquad (4)$$

Where:

ΔU_O - Output voltage ripple of the converter.

The specificity of the CDR related to the isolation transformer is that the secondary winding's amplitude voltage $U_{sec,CDR}$ is twice as high as that of the full-bridge $U_{sec,FBR}$. Thus the current doubler transformer features doubled secondary turns number of the full-bridge one. On the other hand, the secondary current of the isolation transformer is half the output current in case of CDR (5).

Thus, the cross-section of a wire required for the secondary winding could be twice reduced in contrast to the full-bridge transformer (6).

$$I_{sec(rms)CDR} = \frac{P_O}{2 \cdot U_O} \cdot \sqrt{2 \cdot D} \,. \quad (5)$$

$$I_{sec(rms)FBR} = \frac{P_O}{U_O} \cdot \sqrt{2 \cdot D} \,. \quad (6)$$

Each inductor of the CDR topology conducts only half the output current, which in turn gives a possibility of reduced copper loss and better distributed power dissipation than with the full-bridge design. The rms inductor current of the CDR topology is:

$$I_{Lo(rms)} = \sqrt{\left(\frac{P_O}{2 \cdot U_O}\right)^2 + \frac{\left(\frac{P_O}{U_O} \cdot K_{ri}\right)^2}{12} \cdot \left(\frac{1-D}{1-2 \cdot D}\right)^2} = \quad (7)$$

$$= \frac{P_O}{2 \cdot U_O} \cdot \sqrt{1 + \frac{K_{ri}^2}{3} \cdot \left(\frac{1-D}{1-2 \cdot D}\right)^2} \,.$$

Where:

K_{ri} - Output current ripple factor of the converter.

One of the specific benefits of the CDR is the output ripple current cancellation [11]. Two output inductors operate with a 180º phase shifting and could provide the output ripple current cancellation that depends on the operating duty cycle. Figure 5 shows that in the discussed application, the effect of the maximum output ripple current cancellation occurs at the minimum input voltage when the operating duty cycle is maximal.

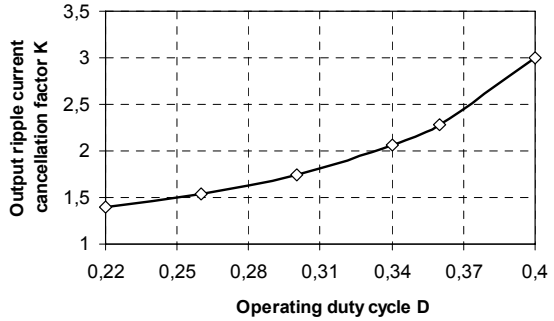


Fig. 5. Output ripple current cancellation factor as a function of the operating duty cycle of the proposed converter.

The worst operating point in the CDR in the presented application is at the maximal input voltage when the duty cycle is changing to its minimum. The ripple current cancellation factor $K=\Delta I_L/\Delta I_O$ is shifting towards the minimum value of 1.4 (figure 5). Thus, the selection criteria for the output inductors for the described application could be derived:

$$L_{O1} = L_{O2} = \frac{U_O \cdot (1 - D_{min})}{\frac{P_O}{U_O} \cdot K_{ri} \cdot f_{sw} \cdot K_{min}} = 5.57 \cdot \frac{U_O^2}{P_O \cdot f_{sw}} \,. \quad (8)$$

Where:

D_{min} - Minimum duty cycle of the converter (0.22).

K_{min} - Minimal ripple current cancellation factor.

K_{ri} - Desired output current ripple factor (K_{ri} =0.1).

In contrast to the full-bridge rectifier where the single inductor is operating at double the switching frequency, the inductors in CDR are operating at two times lower frequency and with the higher current ripple ΔI_L, thus requiring more inductance for the same output current ripple ΔI_O. In some cases, where the frequency response does not matter, it is more feasible to damp the output current ripple by adding extra capacitance to the output filter, thus minimizing demands for inductance.

III. PERFORMANCE EVALUATION OF THE NEW CONVERTER

A. Inverter performance

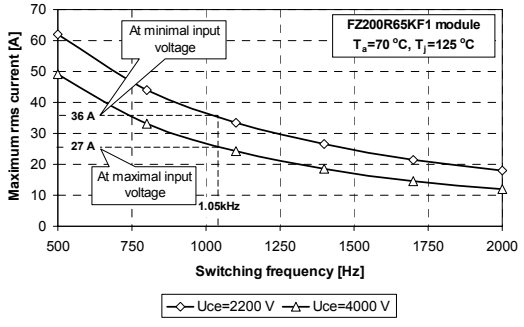
In the discussed application, the rated power of the primary inverter is 50 kW (power losses of the isolation transformer, secondary rectifier and output filter are neglected). Both topologies were evaluated and compared at the operating points presented in Table 1. The rms collector current of IGBTs in both cases could be derived by (9).

$$I_{C(rms)} = \frac{P_O}{U_{in} \cdot \sqrt{D}} \,. \quad (9)$$

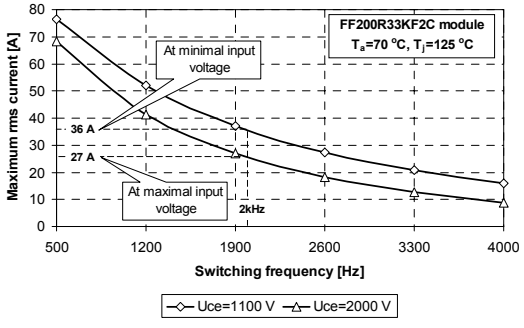
The analysis below relies on the following IGBTs:

- Infineon 3.3 kV/200 A dual IGBT module FF200R33KF2C - in cases of three-level half-bridge;
- Infineon 6.5 kV/200 A single IGBT module FZ200R65KF1 - in cases of two-level half-bridge.

Figure 6 interprets the theoretical switching frequency limits of the FZ200R65KF1 and FF200R33KF2C IGBT modules, imposed by thermal limitations while operating in the hard switching mode and with collector-emitter voltages corresponding to the investigated operating points (Table 1).



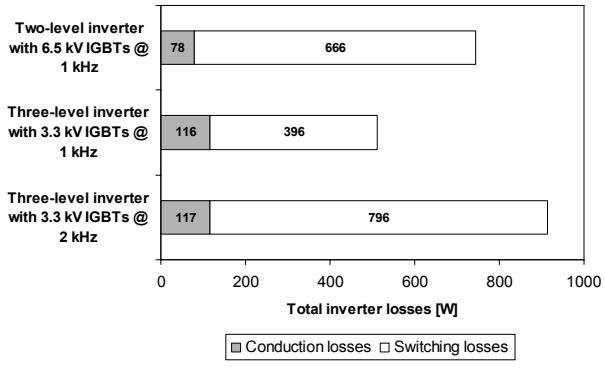
(a)



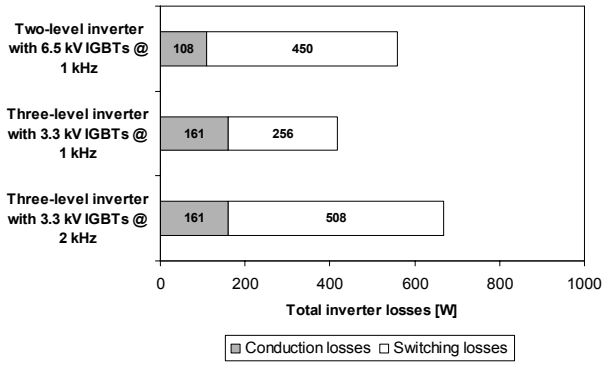
(b)

Fig. 6. Switching properties of 6.5 kV (a) and 3.3 kV (b) IGBT modules in the same operating conditions.

In figure 7 the total inverter loss of the investigated 50 kW inverter topologies is compared with that of different high-voltage IGBTs. The inverters were evaluated in the operating conditions described in Table 1, while the losses of a three-level inverter were studied at two switching frequencies: the same as in the two-level topology (1 kHz) and maximum possible (2 kHz). In cases of 6.5 kV single modules FZ200R65KF1 in the two-level configuration, the total inverter power dissipation for the same switching frequency will be 31% and 25 % higher at maximal and minimal input voltages, correspondingly, as compared to the 3.3 kV dual IGBT modules in the three-level configuration. At their maximum switching performance, the 3.3 kV IGBTs in the three-level configuration are dissipating 23% and 20% more heat at maximal and minimal input voltages, correspondingly, as compared to the two-level inverter.



(a)



(b)

Fig. 7. Comparison of total losses of two- and three-level inverters operating at maximal (a) and minimal (b) input voltages and rated power.

Further analysis of the total inverter power dissipation shows that a specific drawback of the three-level inverter is the conduction losses increased by 30% due to series connection of two transistors (sum of voltage drops) during the conduction period. However, it cannot affect the overall feasibility of this topology in any load conditions. There is some minor power dissipation from clamping diodes Dcl1 and Dcl2 during the positive and negative freewheeling modes, respectively. The dissipated power mostly depends on the leakage inductance of the primary winding and the properties of the diodes implemented. For instance, with the fast recovery epitaxial diodes (FRED) and primary leakage inductance of the isolation transformer used in the project $L_{L,pr} \sim 20$ uH, the worst case power dissipation of clamping diodes Dcl1 and Dcl2 was about 30 W per diode.

Finally, it can be stated that the three-level inverter topology with 3.3 kV IGBTs for the same switching frequency and power rating provides such space saving possibilities as heatsink requirements reduced by a quarter as compared to the two-level 6.5 kV IGBT-based topology. Moreover, it is a remarkable benefit of the 3.3 kV IGBT technology that due to better switching properties they could be operated with at least double switching frequency of those of 6.5 kV counterparts. Taking into account this consideration and for improving the power density, the switching frequency selected for the proposed converter is 2 kHz.

B. Performance of transformer-rectifier stage

The double increase in the switching frequency f_{sw}, utilized from the 3.3 kV IGBTs has had a positive influence on the isolation transformer dimensions and weight, reducing the magnetic core volume (10) and the number of the primary turns (11) for the same transferred power:

$$V_m = 1.5\sqrt{\frac{A \cdot k_{add} \cdot k_t}{k_u}} \cdot \frac{P}{f_{sw}^{\frac{1}{4}} \cdot \Delta T}. \quad (10)$$

$$\varpi_1 = \frac{U_{prI,rms}}{4.44 \cdot f_{sw} \cdot S_m \cdot B_m}. \quad (11)$$

Where:

P - Rated power of the isolation transformer.
k_t - Temperature coefficient of winding resistance.
k_u - Window utilization factor.
k_{add} - Factor assuming increase of the winding resistance with the frequency due to skin and proximity effects.
ΔT - Transformer temperature rise.
A - Core loss per volume per frequency (loss factor).
$U_{prI,rms}$ - rms value of the primary winding voltage at the fundamental frequency.
S_m - Cross-section of the magnetic core.
B_m - Operating flux density of the transformer.

Due to the doubled switching frequency the core volume of the isolation transformer was effectively reduced by 17% for the 50 kVA isolation transformer. Moreover, the isolation transformer for the three-level topology has 14 turns less for the primary winding and 6 additional turns for the secondary, as compared to the two-level one (figure 8).

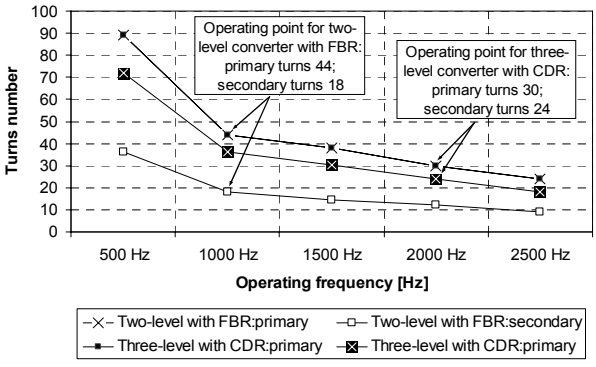


Fig. 8. Number of turns of an isolation transformer as a function of operating frequency for both of the topologies compared.

The reduction of the number of primary turns caused by the higher switching frequency of a three-level inverter with CDR in row with the secondary current twice decreased gives an additional benefit in terms of 92 W smaller power dissipation of the isolation transformer in all operating points. The total loss breakdown shows that core and copper losses are well balanced in cases of the three-level converter, while in the two-level design due to smaller switching frequency the copper losses are prevailing (figure 9).

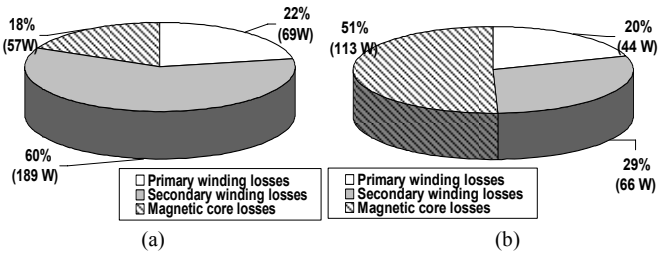


Fig. 9. Power losses breakdown of the 50 kVA isolation transformers designed for two-level (a) and three-level (b) converters.

Due to the number of rectifying diodes reduced twice, in each conduction period the CDR features smaller power dissipation for the same load conditions. The conduction losses of the diode rectifier in cases of FBR and CDR topologies are described by (12) and (13), respectively.

$$P_{FBR} = 4 \cdot I_{D(av)} \cdot U_F = 4 \cdot \frac{I_O}{2} \cdot U_F = 2 \cdot I_O \cdot U_F . \quad (12)$$

$$P_{CDR} = 2 \cdot I_{D(av)} \cdot U_F = 2 \cdot \frac{I_O}{2} \cdot U_F = I_O \cdot U_F . \quad (13)$$

Where:

$I_{D(av)}$ - Average current of the diode.
U_F - Forward voltage drop of the diode.

It should be noted that because of the doubled amplitude voltage value of the secondary winding of the CDR topology, the rectifying diodes with proportionally increased blocking voltage must be used. In the application discussed it was considered to implement the fast recovery epitaxial diodes (FRED) packaged in SOT-227B modules due to the soft recovery and almost negligible switching losses. In dual modules the diodes were connected in parallel, thus the resulting number of diodes was doubled for both topologies. The blocking voltages selected were 1.2 kV and 1.8 kV for the FBR and CDR topologies, respectively. Although the forward voltage drop for the 1.8 kV diodes was 47% higher, the resulting power dissipation of the CDR at rated load conditions was reduced by 27% in comparison with the FBR topology (610 W and 840 W, respectively).

Another source of power dissipation in the output stage of the converter is the output inductor. In FBR topology inductor handles all the output current, while in the CDR the output current is proportionally split between two output inductors. Considering the output ripple cancellation effect and increased operating frequency, the value of the inductance required for CDR design is L_{O1}=L_{O2}=4.8 mH. For the same operating conditions and output ripple limitation, the inductance considered for the FBR topology was the same (L_O=4.8 mH). The required inductor core volume could be estimated by (14).

$$V_{m,i} = \sqrt{\frac{A \cdot k_g \cdot k_{add} \cdot k_t}{k_u}} \cdot \frac{L_O \cdot I_{Lo(rms)}^2 \cdot f_{sw}^{\frac{3}{4}}}{0.3 \cdot \Delta T} \times \times \frac{1 + 3 \cdot e^{\left(1 - \frac{T_{SW}}{t_{on,min}}\right)}}{4} . \quad (14)$$

Where:

L_O - Inductance value.
$I_{Lo(rms)}$ - rms value of a current through the inductor.
k_g - Airgap coefficient.

Because each inductor in the CDR topology is carrying half the output current, the total magnetic core volume in the CDR is 50% smaller than that of a single inductor in the FBR topology. Power losses in inductors could be evaluated by (15).

$$P_i = 13 \cdot \alpha \cdot \Delta T \cdot V_{m,i}^{\frac{2}{3}} . \quad (15)$$

Where:

α - Heat irradiation coefficient.

The total power dissipation of two inductors in the CDR topology were 24% less than that of the single inductor in the FBR topology (580 W and 770 W).

In figure 10 the total loss of the transformer-rectifier stage of both investigated 50 kW converter topologies is compared. By the higher switching frequency available from 3.3 kV IGBTs together with current doubler rectifier implemented the resulting power dissipation of the transformer-rectifier stage was reduced by 26%. Finally, it should be stated that the overall efficiency of the new proposed three-level NPC converter with 3.3 kV IGBTs was increased about 1% as compared to its two-level predecessor with 6.5 kV IGBTs.

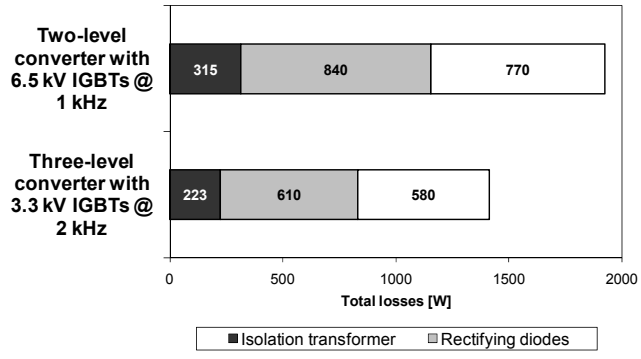


Fig. 10. Comparison of total losses of the transformer-rectifier stage of two- and three-level converters operating at rated power.

IV. FEASIBILITY EVALUATION OF THE NEW CONVERTER

In this section the technical and economic feasibility facts of both topologies will be compared. It should be noted that our feasibility study covers only the high-voltage input inverter stage as the most challenging and costly due to high market prices of high-voltage IGBTs and associated

electronics. The isolation transformer and the output stages of both of the investigated topologies are similar in terms of realization price and physical properties.

A. Packaging

Despite the increased number of transistors in the three-level topology the resulting installation area requirements remain the same (Table 2). Thanks to the dual-transistor modules available for 3.3 kV IGBTs the space-weight constraints imposed by the two-level topology will not be broken. Moreover, due to the 20% reduced height of 3.3 kV IGBT modules, the overall height of the inverter stack was decreased.

TABLE 2
Physical parameters of investigated IGBTs

IGBT type	Length, mm	Height, mm	Width, mm
FF200R33KF2C	140	38	73
FZ200R65KF1	140	48	73

It is evident that the clamping diodes Dcl1 and Dcl2 are additional components in the three-level topology. However, since the average current through these diodes is relatively low, the FRED diodes in compact SOT-227B (Isotop) packages (38 x 25 mm) could be implemented with confidence and with no serious impact on the inverter's dimensions and weight. Figure 11 shows the side-by-side comparison of the of two-level and three-level NPC half-bridge inverter assemblies. It is seen from the picture that the proposed multilevel design provides clear benefits mostly in terms of component mounting density.

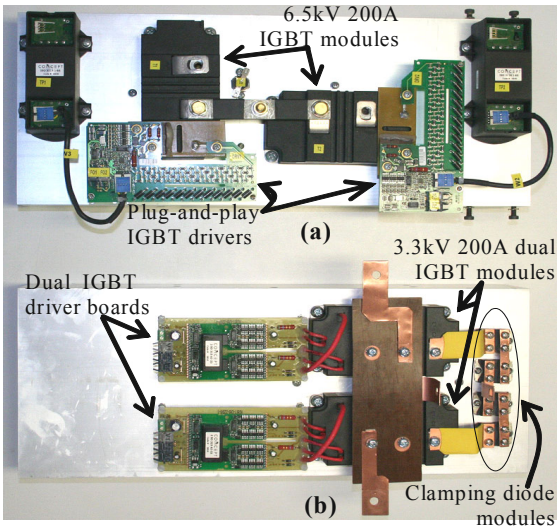


Fig. 11. Side-by-side comparison of two-level (a) and three-level NPC (b) half-bridge inverters.

It is a well-known fact that due to the higher switching frequency the total size and weight of the input high-voltage capacitors could be sufficiently reduced. The proposed three-level half-bridge inverter operated with doubled switching frequency features 50% smaller input capacitors than the two-level topology.

B. Control and protection

As it was reported, although the number of controlled IGBTs is increased by a factor of two, the complexity of the control algorithm and the control system as a whole will not change significantly. The control signals for two additional IGBTs can be derived within the hardware simply by inverting two present PWM signals by the NOT gate logic (figure 3). The only difference is that in contrast to the two-level topology, the control system should process twice the number of error feedbacks from power transistors. Control of dual-IGBT modules can be performed by a single driver core (for example, 2SD315AI-33 from CT-Concept), which gives additional benefits in terms of reliability and system complexity. The number and position of sensors remains unchanged (input and output voltages and currents, central point asymmetry, etc.).

C. Semiconductor price evaluation

Semiconductor price, in particular in high-voltage applications, is one of the essential aspects from the designer's point of view, because the competitiveness of the device produced is always price-dependent. In the case of high-voltage IGBTs, the specially designed dedicated gate drives (*plug-and-play* drivers) should be used. The price of high-voltage semiconductors due to their relative novelty and recently high manufacturing costs is quite high and the feasibility of both investigated topologies seems to be a front row question. Figure 12 shows a comparison of total prices for both of the investigated inverter topologies. Such a huge difference is mostly caused by the over 50% price difference between the 6.5 kV and the 3.3 kV IGBT modules with a collector current of 200 A. As the detailed analysis shows (figure 13), the price of IGBTs accounts for over 70% of the total inverter price in such high-voltage applications and is the determining factor of the final price. Even if two additional clamping diodes are used in the three-level NPC topology, no serious impact on the overall competibility of the proposed solution is achieved.

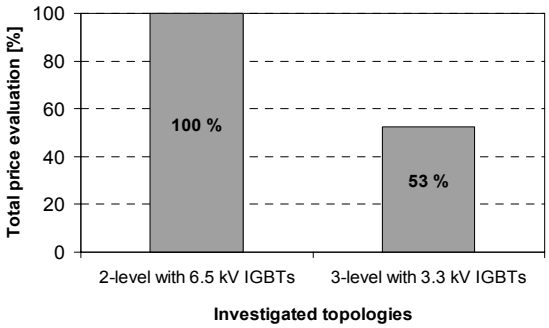


Fig. 12. Comparison of semiconductor price of two- and three-level topologies.

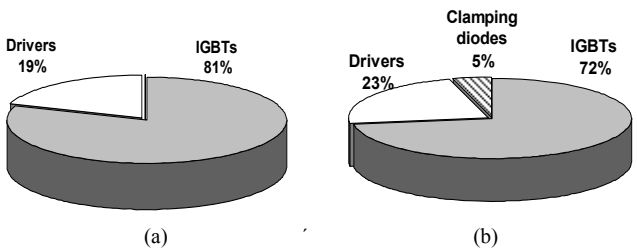


Fig. 13. Distribution of inverter component prices in the 6.5 kV IGBT based two-level (a) and 3.3 kV IGBT based three-level (b) topologies.

V. CONCLUSION

This paper has discussed the galvanically isolated three-level NPC half-bridge DC/DC converter topology with 3.3 kV IGBTs aimed for the high-voltage (≥2.0 kV) high-power (≥10 kW) applications. The proposed converter was comprehensively compared with the 6.5 kV IGBT based two-level half-bridge DC/DC topology. Despite of increased component count the three-level NPC topology could be strongly recommended for such demanding application field as rolling stock because it provides a possibility of transistor implementation with the blocking voltage twice reduced in comparison with conventional two-level configuration, that being especially topical in converters with high voltage transistors (4.5 kV of 6.5 kV IGBTs). For the same transferred power the transistors in the three-level configuration could be operated with at least two times higher switching frequency than in the two-level one. On the other hand, for the same switching frequency the three-level topology with 3.3 kV IGBTs ensures up to 31% less power dissipation than the 6.5 kV IGBT based two-level counterpart.

Thanks to increased switching frequency and current-doubler rectifier implemented in the proposed converter the power dissipation of the isolation transformer was reduced by 30%. Moreover, the 27% and 24% reductions in rectifier and inductor losses respectively, lead to approximately 1% efficiency rise of the proposed converter in comparison with its predecessor. In row with that the three-level topology outpaces the two-level one by more than 20% in terms of power density.

Another essential aspect from the designer's point of view is the total price of inverter switches for different topologies. High voltage IGBTs are the main components of such devices and their prices give a sufficient impact on the final price and, hence, on the overall competitiveness of the device produced. Although in contrast to the two-level topology, the proposed three-level topology utilizes two times more IGBTs and two extra diodes, the 3.3 kV dual IGBT modules implemented give a sufficient 50% price reduction as compared to the 6.5 kV IGBT based counterparts.

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REFERENCES

[1] T. Jalakas, D. Vinnikov, J. Laugis, "Development of 50-kW Isolated DC/DC Converter with High-Voltage IGBTs", *Compatibility in Power Electronics, CPE '07*, pp. 1-6, May-June 2007.

[2] Y. Haroen, P. A. Dahono, J. Sutanto, "A new type of DC-DC converter for rolling stock auxiliary power supply", *Proceedings of 1998 International Conference on Power Electronic Drives and Energy Systems for Industrial Growth*, vol. 1, pp. 436-440, December 1998.

[3] Xinbo Ruan, Bin Li, Qianhong Chen, "Three-level converters-a new approach for high voltage and high power DC-to-DC conversion", *2002 IEEE 33rd Annual Power Electronics Specialists Conference, PESC'02*, vol. 2, pp. 663-668, 2002.

[4] Byeong-Mun Song, R. McDowell, A. Bushnell, J. Ennis, "A three-level DC-DC converter with wide-input voltage operations for ship-electric-power-distribution systems", *IEEE Transactions on Plasma Science*, vol. 32, no. 5, pp. 1856-1863, October 2004.

[5] F. Canales, P. Barbosa, F. C. Lee, "A zero-voltage and zero-current switching three-level DC/DC converter", *IEEE Transactions on Power Electronics,* vol. 17, no. 6, pp. 898-904, November 2002.

[6] Z.L. Lou, Z.S. Wang, "An Improved Three-Level Soft-Switching DC/DC Converter", *5th International CES/IEEE Power Electronics and Motion Control Conference, IPEMC'2006*, vol. 1, pp. 1-5, 14-16, Aug. 2006.

[7] A. Coccia, F. Canales, P. Barbosa, S. Ponnaluri, "Wide input voltage range compensation in DC/DC resonant architectures for on-board traction power supplies", *European Conference on Power Electronics and Applications, EPE'2007*, pp. 1-10, 2-5 Sept. 2007.

[8] I. Roasto, D. Vinnikov, I. Galkin, "Comparison of control methods for high-voltage high-power three-level half-bridge DC/DC converters", *Compatibility and Power Electronics, CPE '09*, pp. 258-264, 20-22 May 2009.

[9] P. Alou, J. A. Oliver, O. Garcia, R. Prieto, J. A. Cobos, "Comparison of current doubler rectifier and center tapped rectifier for low voltage applications", *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, APEC '06*, pp. 7, March 2006.

[10] B.-R. Lin, K. Huang, D. Wang, "Analysis and implementation of full-bridge converter with current doubler rectifier", *IEEE Proceedings of Electric Power Applications*, vol. 152, no. 5, pp. 1193-1202, September 2005.

[11] B.-R. Lin, F.-Y. Hsieh, D. Wang, K. Huang, "Analysis, design and implementation of active clamp zero voltage switching converter with output ripple current cancellation", *IEE Proceedings of Electric Power Applications*, vol. 153, pp. 653-663, Sept. 2006.

BIOGRAPHY

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