DOUBLE CONVERSION UNINTERRUPTED ENERGY SYSTEM WITH RECTIFIER AND THE INVERTER INTEGRATION

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***Abstract* – This paper presents the design, implementation and experimental results of a double conversion uninterrupted power supply (UPS), with integration of the rectifier and the inverter stages. The system is composed by a rectifier and an inverter, which employs a single-pole strategy for the switching modulation. The main system characteristics are: the control assembled with commercial integrated circuits, and the unified circuit of the rectifier and the inverter. Theoretical analysis, operation principle, and topology details are presented and validated through experimental results.**

***Keywords* - Power electronics, double conversion UPS, inverter rectifier integration, reduction of components.**

I. INTRODUCTION

Hospitals, industries, telecommunications companies, and computer centers, concern, more and more, about uninterrupted energy sources, which are internationally known as UPS, or as no-break, in Brazil, according to [1-2]. Due to the need of these sectors not to suffer surges of voltage, interruptions on the electric distribution grid, or frequency transitory oscillations, power electronics has always search for the best solution to solve these drawbacks. Thus, the usage of no-breaks is an excellent solution to keep the quality of energy to feed critical and vital loads [1, 3].

A UPS must protect grid-connected loads from voltage disturbances on the electric distribution grid, since the concessionaires are not always capable to assure the continuity and the quality of the supplied energy [3]. The system is composed by a rectifier, an inverter, a bank of batteries, a bypass circuit, and a galvanic isolation between the transformer input and output [5, 6].

The basic objective of a DC-AC converter is to transform a direct voltage source in alternated symmetrical voltage source with pre-defined amplitude and frequency. These converters, known as "inverters", can be divided into four groups, in accordance to the needed output: dc-ac voltage converters, dc-ac current converters, dc-ac current regulated converters, and phase-controlled dc-ac converters. The most common is the dc-ac voltage converter, which is the initial source of this research.

Among the existing topologies, the full-bridge single-phase voltage inverter, the half-bridge single-phase voltage inverter, and the push-pull inverter are the most used, due to their characteristics. The first one, shown in Figure 1, is more suitable for high power, high voltage applications [2, 5-7, 13, 14]. The output voltage is AC and behaves as a sine waveform. The input can be batteries, solar panels or any other DC voltage source. In some cases their input are filtered rectifying circuits, before entering the inversion process, as presented in [5].

This paper presents two stages employed in a basic UPS topology: the rectifier and the inverter, operating in a unique set structure, as presented in Figure 2. The developed topology was first proposed by Divan [8], though applying a distinct modulation and low capacitance for the input DC bus.

The main advantages observed in this structure are: reduced costs, as it employs a small number of components, low voltage stress across the switches, and the qualities of a single-pole PWM modulation. On the other hand, such characteristics lead to a more complex control strategy.

For inverter applications, the output voltage control and regulation is necessary. The modulation method chosen in this work was a sinusoidal PWM with filter, used for harmonic attenuation. Also, the proposed configuration has the following parameters: input voltage 220 V, output voltage 110 V, and nominal power 1 kVA.

II. DESCRIPTION OF PROPOSED TOPOLOGY

In the proposed topology, switches S_5 and S_6 commutate in low frequency (60 Hz), which, along with diodes D_1 and D_2, present a similar operation of a full-wave rectifier. Switches S_3 and S_4 are complementary to each other and operate at 20 kHz during the two semi-cycles of the input voltage. The proposed switching strategy reduces the stresses across the semiconductors to a level lower than one presented in [5].

For the prototype assembling, switches IFGP50B60PD1 and the rectifier bridges GBPC3521A were used for the power stage.

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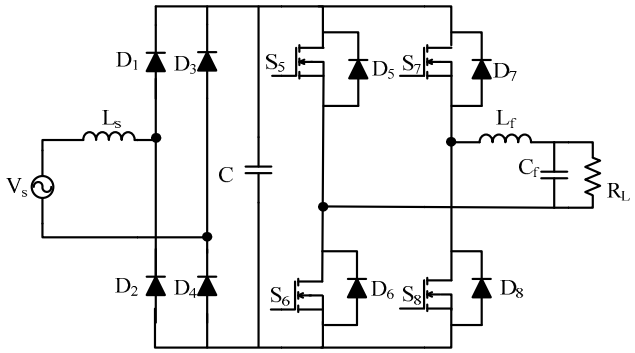

Fig. 1. Single-phase rectifier and inverter in full-bridge topology.

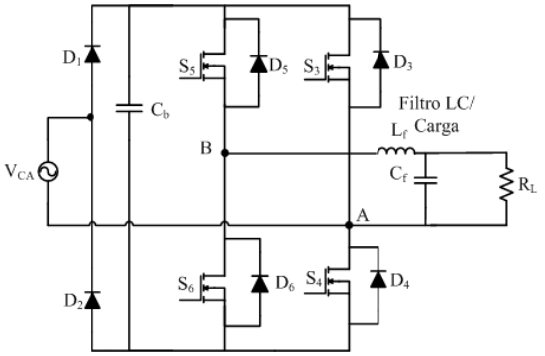

Fig. 2. Proposed topology.

A. Operation Principle

The operation stages will be described using the single-pole modulation. These stages have been divided into two semi-cycles, positive and negative, in accordance with the output voltage. For the theoretical analysis it will be considered that all elements, active and passive, are ideal, the output voltage is a pure sine wave, and the system operates in steady state.

1) Positive semi-cycle of the Output Voltage - It is divided in two intervals: on the first one, the DC bus voltage (V_{CC}) is greater than the input voltage (V_{CA}), and the second, when the input voltage is greater than the DC bus one.

$V_{CC} > |V_{CA}|$:

First stage [t_o - t_a] - This stage, presented on Figure 3, begins when S_3 is turned-on. The circuit is fed by the C_b capacitor that will be discharged by the filtering inductor L_f. The voltage V_{AB} is positive and the current through the inductor increases linearly in its negative semi-cycle. This stage ends when S_3 turns-off.

Second stage [t_a – t_b] – This stage is presented in Figure 4. As S_3 remains blocked, the DC bus is disconnected from the circuit, D_4 assumes the inductor current, and voltage V_{AB} goes to zero. The diode D_4 conducts, due to the direction of the current imposed by L_f, which remains unchanged, and continue to flow through S_6. The inductor L_f is discharged, making its current increases linearly until it is near to zero, in its negative semi-cycle. This stage finishes when the switch S_4 is turned-off.

$V_{CC} < |V_{CA}|$:

Third stage [t_b – t_c] - The third stage of the positive semi-cycle begins when the input voltage starts to be greater than the voltage on DC bus. At this moment, diode D_1 starts to conduct and the DC bus capacitor will start to be charged, as well as the L_f inductor. The voltage V_{AB} is positive, as shown in Figure 5. The current flows through D_6, due to the fact that the current flowing through D_1 is higher than the one through L_f, as the current in D_1 is the sum of the current that flows through S_3 and the one that circulates through the DC bus. This stage finishes when S_3 is turned-off.

Fourth stage [t_c – t_d] - This stage starts when S_3 is blocked, as presented in Figure 6. The direction of the current polarizes D_4, the voltage V_{AB} is zero, and the current through D_1 is greater than the current through the L_f inductor, as it is the sum of the currents through D_4 and D_6. When the input voltage starts to be lower than the DC bus one, the inverter comes back to operation stages 1 and 2 until the output voltage goes to zero again, beginning a new cycle.

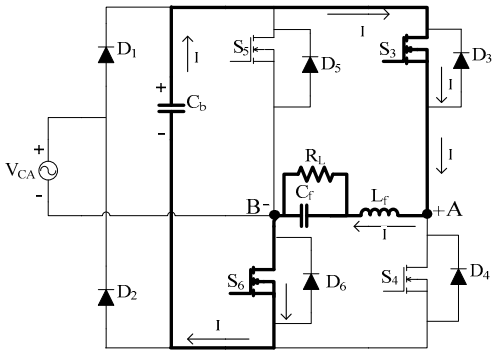

Fig. 3. First stage of the positive semi-cycle of the output voltage.

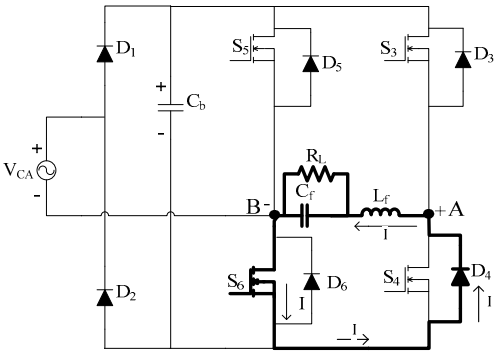

Fig. 4. Second stage of the positive semi-cycle of the output voltage.

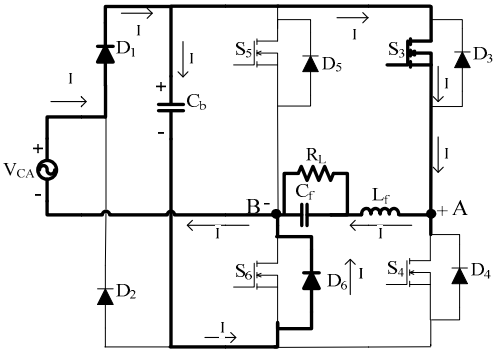

Fig. 5. Third stage of the positive semi-cycle of the output voltage.

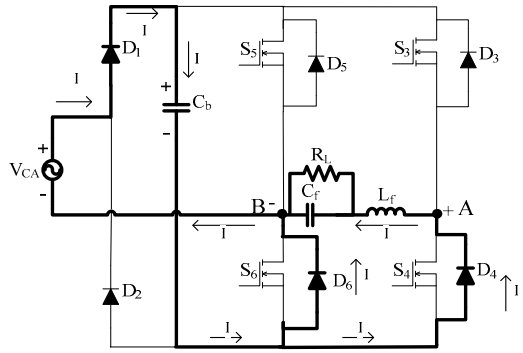

Fig. 6. Fourth stage of the positive semi-cycle of the output voltage.

2) Negative semi-cycle of the Output Voltage - It is divided in two intervals: while the slide DC bus voltage is greater than the input one, and when the input is greater than DC bus one.

$V_{CC} > |V_{CA}|$:

First stage [$t_d - t_e$] – At instant t_d, S_4 and S_5 are turned-on, connecting the load and the filter LC to the DC bus, which supplies it. The voltage V_{AB} is negative and the current through the inductor increase in its positive semi-cycle. This stage can be observed in Figure 7 and finishes when S_4 is turned-off.

Second stage [$t_e - t_f$] – During this stage, the current that flows through the L_f inductor remains on the same direction, because D_3 is conducting. The voltage V_{AB} is zero, the current through the Lf inductor decreases, and the energy previously stored on the inductor is now delivered to the load. The second stage of operation can be seen in Figure 8 and it finishes when S_3 turns-off.

$V_{CC} < |V_{CA}|$:

Third stage [$t_f - t_g$] - During this stage, D_2 and S_4 are conducting. The voltage V_{AB} becomes negative ($-V_{CC}$) and the current through L_f inductor increases. Figure 9 shows this operation stage, which ends when S_4 turns-off.

Fourth stage [$t_g - t_h$] – Figure 10 presents the fourth stage, which begins when S_4 turns-off, forcing D_3 to conduct. The voltage V_{AB} goes to zero and the current through the L_f inductor decreases, delivering the previously stored energy to the load. This stage ends when S4 turns-on.

When the input voltage is lower than the DC bus voltage the inverter will operate again on stages 1 and 2. The D_2 is blocked until the output voltage decrease to zero starting a new cycle.

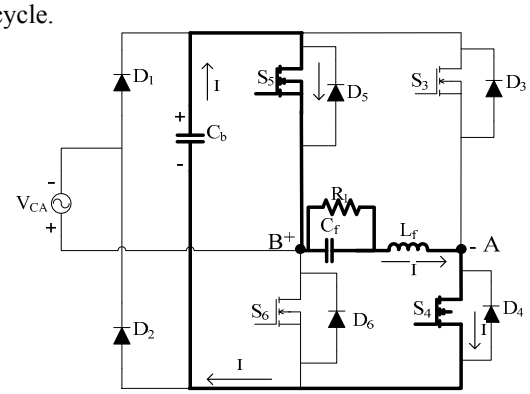

Fig. 7. First stage of the negative semi-cycle of the output voltage.

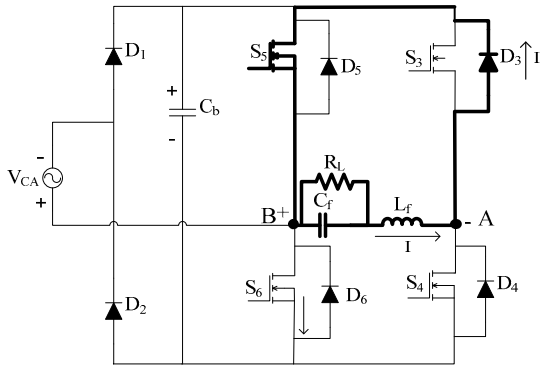

Fig. 8. Second stage of the negative semi-cycle of the output voltage.

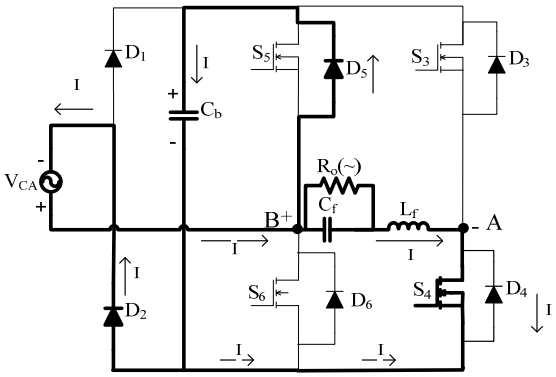

Fig. 9. Third stage of the negative semi-cycle of the output voltage.

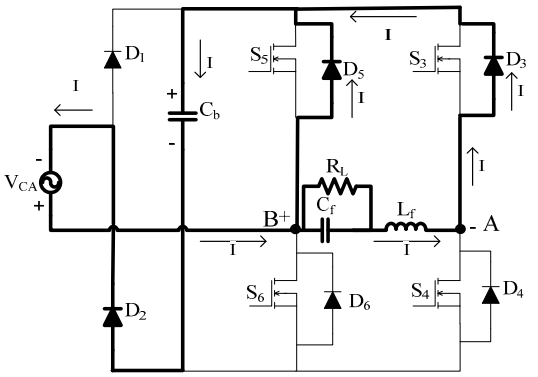

Fig. 10. Fourth stage of the negative semi-cycle of the output voltage.

B. Applied Modulation

The modulation strategy adopted to control the switches of the proposed topology, presented in Figure 2, was the three-level sinusoidal PWM with a rectified sine wave reference, in order to lower the ripple of the output voltage, in accordance with [4] and [7]. Appling the sinusoidal PWM with a rectified sine wave reference, and the modulation of just one leg of the inverter, it is possible to obtain three levels on the output voltage. S_5 and S_6 commutate on the frequency of the input voltage, and the other leg, formed by S_3 and S_4, is controlled by comparing a modulator sine wave signal with a triangular carrier.

During the positive semi-cycle of the input voltage, S_6 and D_1 are turned-on, while S_5 and D_2 are blocked, and vice-versa on the negative semi-cycle. When S_5 and S_6 are conducting, S_3 and S_4 are complementarily switched in high

frequency. In this type of modulation the output voltage presents three instantaneous values: +Vcc, zero or - Vcc.

The proposed modulation requires a low-pass LC output filter, in order to prevent distortions on the output voltage. It must be noticed that this filter was chosen due to its characteristics of reducing reactive components, lower the output voltage ripple, and low cost, weight and volume.

The filter inductance and capacitance can be expressed by equations (1) and (2), respectively, according to [1, 17, 18].

$$L_f = \frac{\sqrt{2}\cdot V_o \cdot (\sqrt{2}\cdot V_{in_{pk}} - \sqrt{2}\cdot V_o)}{2\cdot \Delta I_{Lf}\cdot f_s \cdot V_{in_{pk}}} \quad (1)$$

$$C_f = \frac{1}{L_f \cdot \left(\frac{2\cdot\pi\cdot f_s}{10}\right)^2} \quad (2)$$

Where:

V_{in_pk} - Peak input voltage.
V_o - Output voltage.
ΔI_{Lf} - Current ripple through the filter inductor.
f_s - Switching frequency.

C. Control strategy

The control technique developed is known as voltage loop control and is widely applied on inverters. It consists of monitoring the output voltage and comparing it with a sine reference voltage. To generate the synchronized reference voltage with the input one, a microcontroller is used.

The inverter transfer function was obtained through the CCM small-signal Buck converter analysis, according to [11], and implemented as shown in Figure 11 [12].

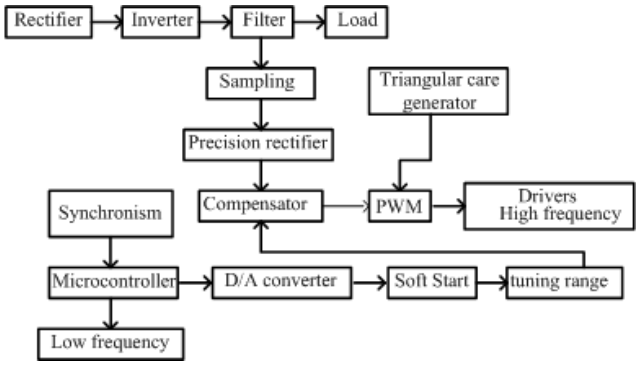

Fig. 11. Schematic diagram of the proposed control strategy.

In order to control the output voltage loop, it was chosen the PID compensator. The poles allocation criterions were adopted as follows: one pole was allocated on the origin, minimizing the static error during the permanent regime, while the other was allocated on the switching frequency in order to attenuate high frequency signals on the voltage loop. The zeros were allocated on the natural oscillation frequency and the open loop crossing frequency (FTLAv) is adopted as four times lower than the switching frequency [11].

Adopting these criterions, the zeros and poles frequencies can be calculated: $f_{z1} = f_{z2} = 1{,}659$ kHz, $f_{p1} = 0$ Hz e $f_{p2} = 16{,}593$ kHz.

Figure 11 presents the Bode diagram of the open loop transfer function, where can be observed the system before the compensation (dashed line), and the compensated system (solid line). The phase margin is 32 degrees.

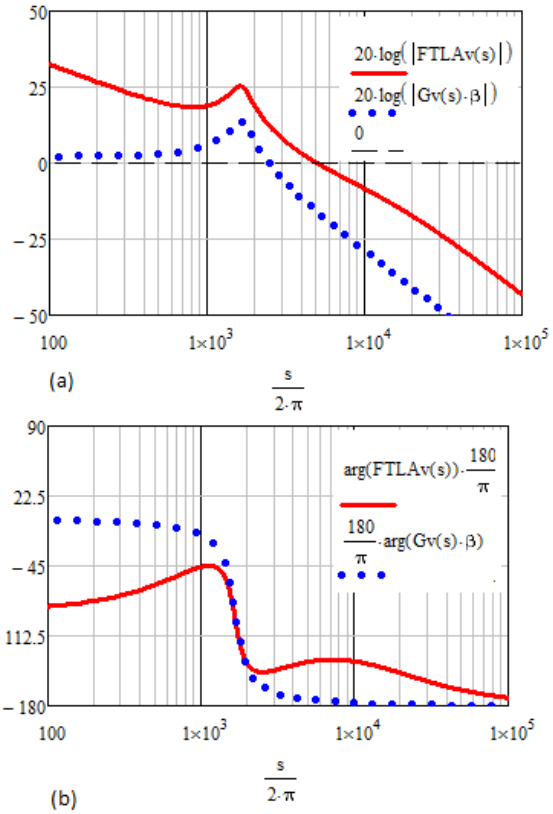

Fig. 12. Bode diagram of the open loop transfer function (a) gain, (b) phase.

III. SWITCHING STRESS ANALISYS

The current peak value through D_1 and D_2, can be expressed by equation (3) [19]:

$$I_{D1_{pk}} = \frac{C_b \cdot \left(V_{c_{pk}} - V_{c_{min}}\right)}{t_c} \quad (3)$$

The waveform of the instantaneous current through S_3 is shown in Figure 13. The average value of this current can be approached by (4) [15].

$$I_{S3_{AVG}} = \frac{1}{M_f}\sum_{i=0}^{\frac{M_f}{2}} \int_i^{i+M\cdot sen\left(\frac{2\cdot\pi}{M_f}\cdot i\right)} I_{o_{pk}}\, sen\left(\frac{2\pi}{M_f}t\right) dt \quad (4)$$

The frequency index of the inverter is the relation between the frequency of the carrier signal (f_p) and the frequency of the modulating signal (f_m). The value of the RMS current is given by (5) [15].

$$I_{S3_{RMS}} = \sqrt{\frac{1}{M_f}\sum_{i=0}^{\frac{M_f}{2}}\int_{i}^{i+M\cdot sen\left(\frac{2\cdot\pi}{M_f}\right)}\left[I_{o_{pk}}\,sen\left(\frac{2\pi}{M_f}t\right)\right]^2 dt} \quad (5)$$

Where:

M - Modulation index.
M_f - Frequency index.
I_o - Load current.
f_m - Modulating wave.
f_p - Carrier wave.
I_{o_pk} - Load current peak.

Diode D_3 conducts when S_4 is blocked and the current through it is behaves as the waveform presented on Figure 14. The average current through D_3 is equal to the average current through D_4, which can be calculated as (6), based on Figure 13 [15]. The current RMS value through D_3 and D_4 can be expressed as (7).

$$I_{D3_{AVG}} = \frac{1}{M_f}\cdot\sum_{i=0}^{\frac{M_f}{2}}\int_{i+M\cdot sen\left(\frac{2\cdot\pi}{M_f}\cdot i\right)}^{i+1} I_{o_{pk}}\,sen\left(\frac{2\pi}{M_f}t\right)dt \quad (6)$$

$$I_{D3_{RMS}} = \sqrt{\frac{1}{M_f}\sum_{i=0}^{\frac{M_f}{2}}\int_{i+M\cdot sen\left(\frac{2\cdot\pi}{M_f}\right)}^{i}\left[I_{o_{pk}}\,sen\left(\frac{2\pi}{M_f}t\right)\right]^2 dt} \quad (7)$$

In order to calculate of the average and RMS current through S_5 and S_6, it must be considered the instant when the switches are blocked on its operation stage. Thus, the average current can be expressed by (8) [15].

$$I_{S5_{AVG}} = \frac{1}{2\pi}\left(\int_0^{t_{c1}\pi} I_{o_{pk}}\,Msen(\omega t)\,d\omega t + \int_{t_{c2}\pi}^{\pi} I_{o_{pk}}\,Msen(\omega t)\,d\omega t\right) \quad (8)$$

The RMS current through these switches can be calculated by (9) [15].

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\left(\int_0^{t_{c1}\pi}\left(I_{o_{pk}}\,Msen(\omega t)\right)^2 d\omega t + \int_{t_{c2}\pi}^{\pi}\left(I_{o_{pk}}\,Msen(\omega t)\right)^2 d\omega t\right)} \quad (9)$$

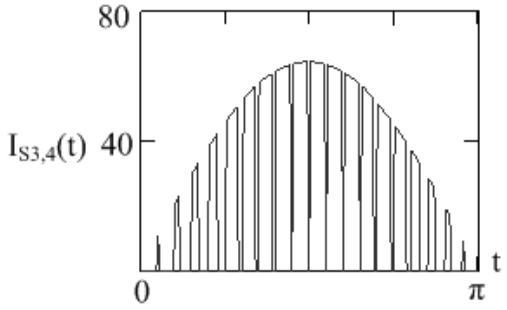

Fig. 13. Instantaneous current through switches S_3 and S_4.

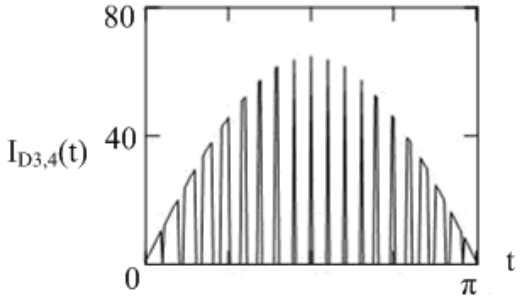

Fig. 14. Instantaneous current through diodes D_3 and D_4.

The current flowing through the DC bus capacitor can be obtained using (10).

$$I_{Cb_{RMS}} = \sqrt{I_{1_{RMS}}^2 + I_{2_{RMS}}^2} \quad (10)$$

Where:

$I_{1\_RMS}^2$ - RMS value of the AC component of the input current.

$I_{2\_RMS}^2$ - RMS value of the rectifier output current.

IV. EXPERIMENTAL RESULTS

This section presents the experimental waveforms of the proposed topology operating with nominal power and linear load of 1 kW.

Figure 15 and 16 present, respectively, the assembled power and control prototypes.

The input voltage and current waveforms during one cycle are illustrated in Figure 17. The measured input current RMS value was 8.25A.

The output voltage and current are presented on Figure 18, where can be observed a small distortion in both waveforms on zero-crossing region. This occurs due to the synchronism between the commutation on the low-frequency inverter leg and the input voltage, due to the presence of inductive output filter. If the load was purely resistive, this distortion would be not identifiable. The measured current RMS value was 9.06A.

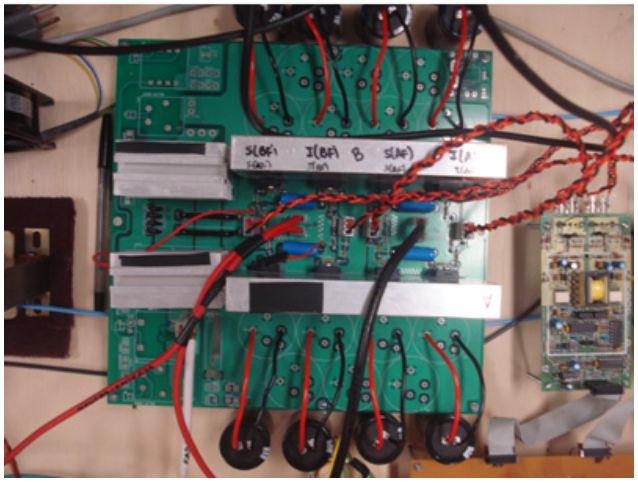

Fig. 15. Prototype power stage picture.

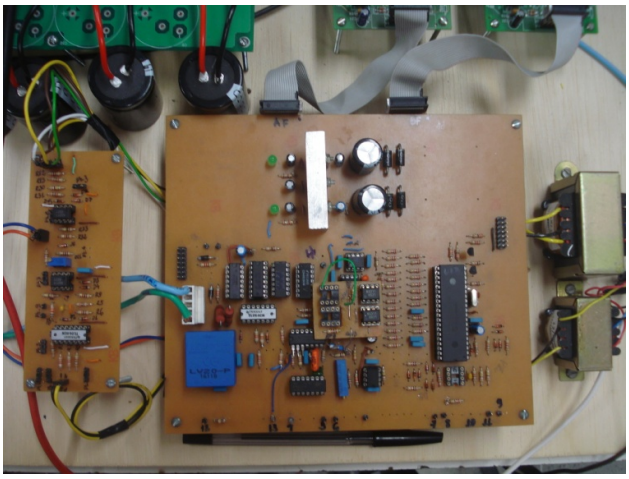

Fig. 16. Prototype control picture.

Figure 19 illustrates the current waveform through the inductor filter. The current distortion observed at the end of each semi-cycle occurs due to the reference voltage synchronism, used on the loop control of the input voltage, limiting the modulation.

Figure 20 presents the current across one of the DC bus capacitor, while Figure 21 shows the output voltage waveform before the filtering, where can be observed the three levels. Figure 22 shows the total harmonic distortion of the output voltage. Figure 23 illustrates the efficiency curve, where can be observed that the inverter efficiency, in nominal power (1kW), was 91%.

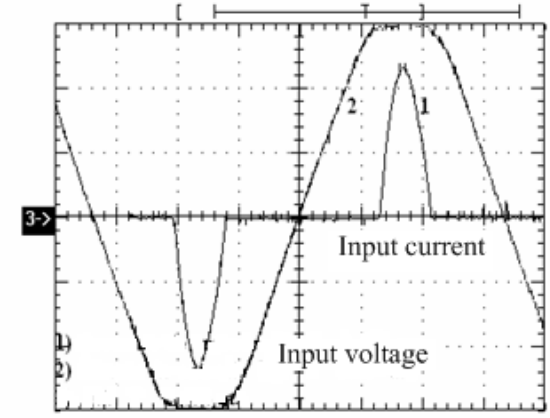

Fig. 17. Input voltage and current waveforms (100 V/div, 10 A/div, 2 ms/div).

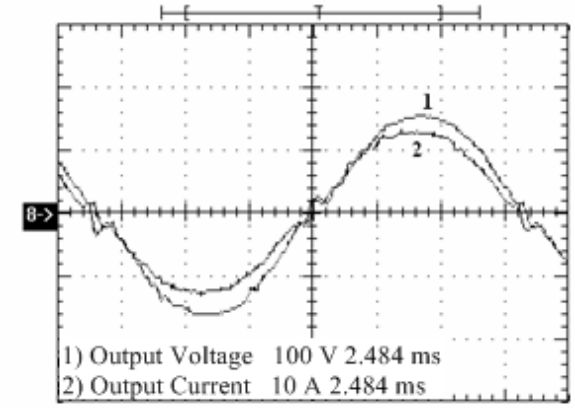

Fig. 18. Output voltage and current waveforms (100 V/div, 10 A/div, 2 ms/div).

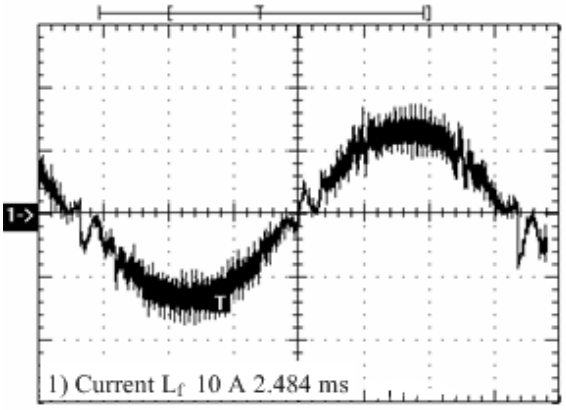

Fig. 19. Waveform of the current through the inductor filter (10 A/div, 2,484 ms/div).

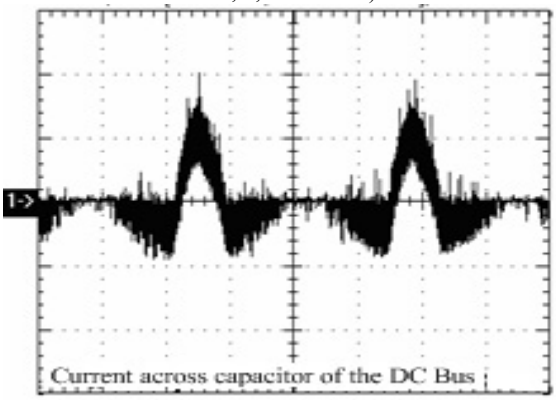

Fig. 20. DC bus current (2 A/div, 2.5 ms/div).

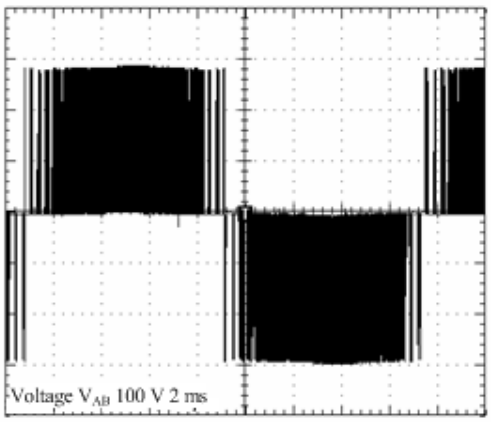

Fig. 21. Non-filtered output voltage (100 V/div, 2ms/div).

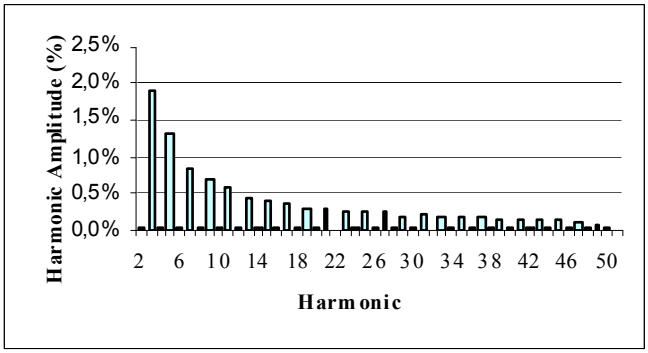

Fig. 22. Total Harmonic Distortion.

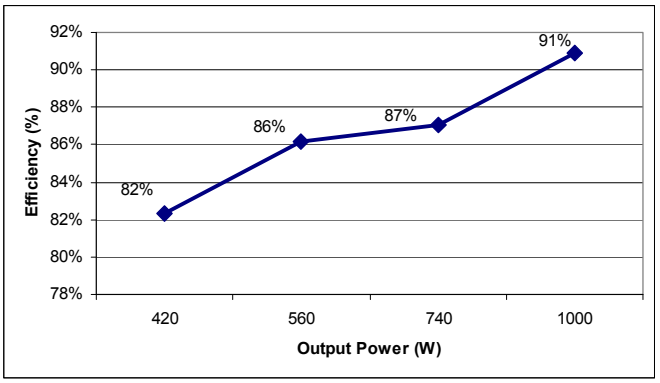

Fig. 23. Efficiency curve.

V. CONCLUSION

This paper presented an inverter topology which is far suitable for high power and great output voltage applications. The sinusoidal PWM modulation using the rectified sine waveform as reference was the most coherent with the necessities, as better characteristics from the waveforms were obtained.

The adopted circuit presents a fewer number of components if compared to conventional topologies, which guarantees good performance and efficiency. Also it possesses the qualities of single-pole modulation PWM three levels.

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