ANALYSIS OF ACTIVE POWER FILTERS OPERATING WITH UNBALANCED LOADS

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Abstract – **The aim of this paper is to perform an analysis of the shunt Active Power Filter (APF) operating with unbalanced loads. The impact of the load imbalance on the APF performance is mathematically demonstrated and validated with experimental results using a 25 kVA shunt APF prototype. The APF operation in such conditions is affected by the appearance of DC-link voltage ripple at twice the grid frequency. As consequence, the source currents become distorted and the APF performance deteriorates. Based on this fact, a new control scheme is proposed to avoid high voltage ripple in the DC link, without increasing the DC-link capacitance.**

Keywords **– Active Power Filter, Unbalanced Load, Voltage Loop Control.**

I. INTRODUCTION

The grid power quality issue has become a great concern due to the connection of non-linear loads, such as diode/thyristor front-end rectifiers that inject high harmonic currents into the grid. The shunt Active Power Filter (APF) is considered as a well-known solution to reduce the current harmonics to acceptable limits. The conventional APF topology consists of a three-phase Voltage Source Inverter (VSI) connected to the Point of Common Coupling (PCC) by means of an L filter, as shown in Figure 1. The APFs have also demonstrated to be very effective not only to mitigate the harmonics but also to perform additional power quality improvement tasks as reactive power and unbalanced load compensation [1],[2]. However, if the compensation of the reactive power and the fundamental negative current sequence is possible, it is often not justified due to the increase of the APF rated power [1],[2].

Coming to the unbalanced load issue [3]-[10], the presence of fundamental negative sequence component in the load currents can affect the APF system performance. This negative sequence, if not blocked by the APF current reference generator, will produce a fundamental negative sequence component in the APF currents due to the proportional gain of the current controller. That will produce a 2nd order ripple in the DC-link voltage, which will generate harmonic distortion in the source currents. Therefore, if the unbalanced load compensation is not required, the circulation of the fundamental negative sequence currents in the APF must be completely blocked to avoid distortion of the source currents.

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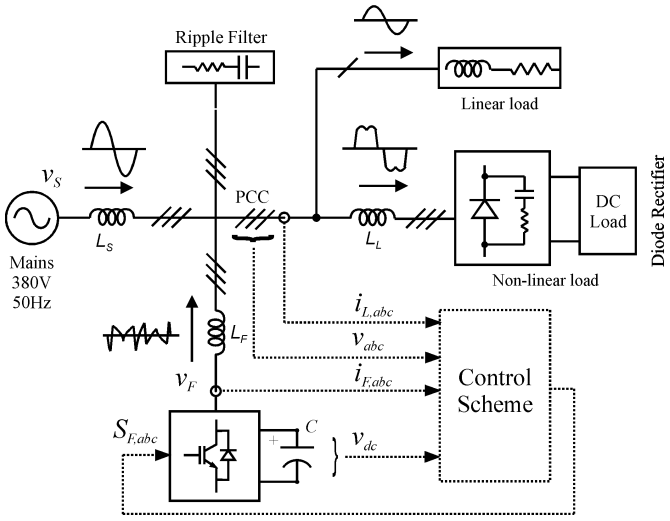

Fig. 1. Basic current harmonic compensation scheme of an unbalanced load using a shunt APF.

The aim of this paper is to perform an analytical study of the APF operating with unbalanced load. The effect of the negative sequence component on the APF performance will be mathematically demonstrated and validated with experimental results using a 25kVA shunt APF prototype. Based on this analysis, a new voltage loop scheme is proposed to avoid high DC-link voltage ripple without increasing the DC-link capacitance and thus the APF cost.

II. MATHEMATICAL MODEL

The continuous-time dynamic model of the shunt APF of Figure 1 can be represented by the following equations on the AC and DC side, respectively:

$$L_T \cdot d\bar{i}_F(t)/dt = \bar{v}_S(t) - \bar{v}_F(t) - R_T \cdot \bar{i}_F(t) \qquad (1)$$

$$C \cdot dv_{dc}(t)/dt = i_{dc}(t) \qquad (2)$$

where L_T=(L_F+L_S), R_T=(R_F+R_S); The vectors $\bar{v}_S(t), \bar{v}_F(t), \bar{i}_F(t)$ represent the grid voltage, the APF poles voltage and APF input current. A continuous switching vector $s(t)$ can be defined as

$$\bar{s}(t) = \frac{2}{3}\left(s_a(t) + \alpha \cdot s_b(t) + \alpha^2 \cdot s_c(t)\right) \qquad (3)$$

where s_a , s_b , s_c are the duty cycles of each converter leg and $\alpha = e^{j\frac{2\pi}{3}}$. The factor 2/3 found in (3) is selected to maintain the same length of the switching vector after the

transformation. In this case, the transformation is said to be amplitude invariant [11].

The active power $P_{poles}(t)$ at the inverter poles can be obtained as

$$P_{poles}(t)=\frac{3}{2}\mathrm{Re}\left\{S_{poles}(t)\right\}=\frac{3}{2}\mathrm{Re}\left\{\bar{v}_F(t)\cdot\bar{i}_F{}^*(t)\right\} \quad (4)$$

where the superscript "*" means complex conjugate. The coefficient 3/2 in (4) is a direct result of the application of the 2/3 factor for the voltage and current vectors [11].

The inverter poles voltage vector $\bar{v}_F$ is obtained replacing $s_j=0.5\cos(\omega t+\theta_j)+0.5$ (where $\theta_j=\{0,-2\pi/3,2\pi/3\}$) in the voltage vector $\bar{v}_F=2/3(v_{aN}+\alpha\cdot v_{bN}+\alpha^2\cdot v_{cN})$ where $v_{jn}=s_jV_{dc}$ and j=a,b,c.

$$\bar{v}_F(t)=\frac{1}{2}\bar{s}(t)v_{dc}(t) \quad (5)$$

Substituting (5) in (4) yields the active power $P_{poles}(t)$ as

$$P_{poles}(t)=\frac{3}{2}\mathrm{Re}\left\{\frac{1}{2}\bar{s}(t)\cdot v_{dc}(t)\cdot\bar{i}_F{}^*(t)\right\} \quad (6)$$

If the switching and conduction losses are neglected, the active power at the inverter output is equal to the active power at the inverter poles:

$$P_{out}=v_{dc}(t)\cdot i_{dc}(t)=P_{poles}(t)=\frac{3}{4}\cdot v_{dc}(t)\,\mathrm{Re}\left\{\bar{s}(t)\cdot\bar{i}_F{}^*(t)\right\} \quad (7)$$

So, the i_{dc} current is easily obtained from (7) as

$$i_{dc}(t)=\frac{3}{4}\mathrm{Re}\left\{\bar{s}(t)\cdot\bar{i}_F{}^*(t)\right\} \quad (8)$$

Referring (8) in stationary (α,β) frame yields

$$i_{dc}(t)=\frac{3}{4}\mathrm{Re}\left\{\bar{s}_{\alpha\beta}(t)\cdot\bar{i}_{F\alpha\beta}{}^*(t)\right\} \quad (9)$$

where

$$\bar{s}_{\alpha\beta}=\bar{s}_{\alpha\beta}^{1p}+\bar{s}_{\alpha\beta}^{1n}+\sum_{h=6k+1}^{\infty}\bar{s}_{\alpha\beta}^{hp}+\sum_{h=6k-1}^{\infty}\bar{s}_{\alpha\beta}^{hn}\quad k=1,2,3\ldots \quad (10)$$

$$\bar{i}_{F\alpha\beta}=\bar{i}_{F\alpha\beta}^{1p}+\bar{i}_{F\alpha\beta}^{1n}+\sum_{h=6k+1}^{\infty}\bar{i}_{F\alpha\beta}^{hp}+\sum_{h=6k-1}^{\infty}\bar{i}_{F\alpha\beta}^{hn}\quad k=1,2,3\ldots \quad (11)$$

Considering a generic variable $\bar{x}$, the space vector of a positive and a negative h-order harmonic frequency can be expressed in stationary frame as $\bar{x}_{\alpha\beta}^{hp}=e^{jh\omega_e t}\cdot\bar{x}_{dq}^{hp}$ (where $\omega_e=2\pi f_{grid}$ rad/s) and $\bar{x}_{\alpha\beta}^{hn}=e^{-jh\omega_e t}\cdot\bar{x}_{dq}^{hn}$. The vector $\bar{x}_{dq}^{hp}$ is the space vector of a positive h-order harmonic frequency represented in a synchronous frame rotating at positive $h\omega_e t$ and $\bar{x}_{dq}^{hn}$ is the space vector of a negative h-order harmonic frequency represented in a synchronous frame rotating at negative $h\omega_e t$. The expressions found in (10) and (11) can be simplified if it is considered that the APF compensates only the first harmonic pair (5th, 7th). Therefore, $\bar{s}_{\alpha\beta}$ and $\bar{i}_{F\alpha\beta}$ contain the positive and negative sequences of fundamental component and the 5th and 7th harmonics.

$$\begin{aligned}\bar{s}_{\alpha\beta}&=\bar{s}_{\alpha\beta}^{1p}+\bar{s}_{\alpha\beta}^{1n}+\bar{s}_{\alpha\beta}^{5n}+\bar{s}_{\alpha\beta}^{7p}\\&=e^{j\omega_e t}\cdot\bar{s}_{dq}^{1p}+e^{-j\omega_e t}\cdot\bar{s}_{dq}^{1n}+e^{-j5\omega_e t}\cdot\bar{s}_{dq}^{5n}+e^{j7\omega_e t}\cdot\bar{s}_{dq}^{7p}\end{aligned} \quad (12)$$

$$\begin{aligned}\bar{i}_{F\alpha\beta}&=\bar{i}_{F\alpha\beta}^{1p}+\bar{i}_{F\alpha\beta}^{1n}+\bar{i}_{F\alpha\beta}^{5n}+\bar{i}_{F\alpha\beta}^{7p}\\&=e^{j\omega_e t}\cdot\bar{i}_{dq}^{1p}+e^{-j\omega_e t}\cdot\bar{i}_{dq}^{1n}+e^{-j5\omega_e t}\cdot\bar{i}_{dq}^{5n}+e^{j7\omega_e t}\cdot\bar{i}_{dq}^{7p}\end{aligned} \quad (13)$$

Replacing (12) and (13) in (9) yields

$$\begin{aligned}i_{dc}=\frac{3}{4}\mathrm{Re}\{&(e^{j\omega_e t}\bar{s}_{dq}^{1p}+e^{-j\omega_e t}\bar{s}_{dq}^{1n}+e^{-j5\omega_e t}\bar{s}_{dq}^{5n}+e^{j7\omega_e t}\bar{s}_{dq}^{7p})\cdot\\&(e^{j\omega_e t}\bar{i}_{dq}^{1p}+e^{-j\omega_e t}\bar{i}_{dq}^{1n}+e^{-j5\omega_e t}\bar{i}_{dq}^{5n}+e^{j7\omega_e t}\bar{i}_{dq}^{7p})^*\}\end{aligned} \quad (14)$$

After expanding the terms and rearranging the real part of (14) the DC side current becomes

$$\begin{aligned}i_{dc}=\frac{3}{4}(&I_{dc}+I_{s2}\sin 2\omega_e t+I_{c2}\cos 2\omega_e t+I_{s4}\sin 4\omega_e t+\\&I_{c4}\cos 4\omega_e t+I_{s6}\sin 6\omega_e t+I_{c6}\cos 6\omega_e t+I_{s8}\sin 8\omega_e t+\\&I_{c8}\cos 8\omega_e t+I_{s12}\sin 12\omega_e t)\end{aligned} \quad (15)$$

where

$$I_{dc}=s_d^{1p}\cdot i_d^{1p}+s_q^{1p}\cdot i_q^{1p}+s_d^{1n}\cdot i_d^{1n}+s_q^{1n}\cdot i_q^{1n} \quad (16)$$

$$I_{s2}=s_d^{1p}\cdot i_q^{1n}-s_q^{1p}\cdot i_d^{1n}-s_d^{1n}\cdot i_q^{1p}+s_q^{1n}\cdot i_d^{1p} \quad (17)$$

$$I_{c2}=s_d^{1p}\cdot i_d^{1n}+s_q^{1p}\cdot i_q^{1n}+s_d^{1n}\cdot i_d^{1p}+s_q^{1n}\cdot i_q^{1p} \quad (18)$$

$$I_{s4}=s_d^{1n}\cdot i_q^{5n}+s_d^{5n}\cdot i_q^{1n} \quad (19)$$

$$I_{c4}=s_q^{1n}\cdot i_q^{5n}+s_d^{5n}\cdot i_d^{1n} \quad (20)$$

$$I_{s6}=s_d^{1p}\cdot i_q^{5n}-s_d^{1p}\cdot i_q^{7n}-s_d^{5n}\cdot i_q^{1p}+s_q^{7p}\cdot i_q^{1p} \quad (21)$$

$$I_{c6}=s_q^{1p}\cdot i_q^{5n}+s_q^{1p}\cdot i_q^{7p}+s_d^{5n}\cdot i_d^{1p}+s_d^{7p}\cdot i_q^{1p} \quad (22)$$

$$I_{s8}=s_d^{7p}\cdot i_q^{1n}-s_d^{1n}\cdot i_q^{7p} \quad (23)$$

$$I_{c8}=s_q^{1n}\cdot i_q^{7p}+s_d^{7p}\cdot i_d^{1n} \quad (24)$$

$$I_{s12}=s_d^{7p}\cdot i_q^{5n}-s_d^{5n}\cdot i_q^{7p} \quad (25)$$

Replacing (15) in (2) yields

$$\begin{aligned}\frac{dv_{dc}}{dt}=\frac{3}{4C}(&I_{dc}+I_{s2}\sin 2\omega_e t+I_{c2}\cos 2\omega_e t+I_{s4}\sin 4\omega_e t+\\&I_{c4}\cos 4\omega_e t+I_{s6}\sin 6\omega_e t+I_{c6}\cos 6\omega_e t+I_{s8}\sin 8\omega_e t+\\&I_{c8}\cos 8\omega_e t+I_{s12}\sin 12\omega_e t)\end{aligned} \quad (26)$$

Integrating both sides of (26) gets the DC-link voltage as

$$v_{dc} = \frac{3}{4C}\left(I_{dc} - \frac{I_{s2}}{2\omega_e}\cos 2\omega_e t + \frac{I_{c2}}{2\omega_e}\sin 2\omega_e t - \frac{I_{s4}}{2\omega_e}\cos 4\omega_e t + \right.$$
$$\frac{I_{c4}}{4\omega_e}\sin 4\omega_e t - \frac{I_{s6}}{6\omega_e}\cos 6\omega_e t + \frac{I_{c6}}{6\omega_e}\sin 6\omega_e t - \quad (27)$$
$$\left.\frac{I_{s8}}{8\omega_e}\cos 8\omega_e t + \frac{I_{c8}}{8\omega_e}\sin 8\omega_e t - \frac{I_{s12}}{12\omega_e}\cos 12\omega_e t\right)$$

Finally, (27) can be rewritten using some trigonometric identities:

$$v_{dc} = \frac{3}{4C}\left(I_{dc} + \frac{I_2}{2\omega_e}\sin(2\omega_e t - \alpha_2) + \right.$$
$$\frac{I_4}{4\omega_e}\sin(4\omega_e t - \alpha_4) + \frac{I_6}{6\omega_e}\sin(6\omega_e t - \alpha_6) + \quad (28)$$
$$\left.\frac{I_8}{8\omega_e}\sin(8\omega_e t - \alpha_8) + \frac{I_{12}}{12\omega_e}\cos(12\omega_e t - \alpha_{12})\right)$$

where

$$I_{2k} = \sqrt{I_{s2k}^2 + I_{c2k}^2}, \quad \alpha_{2k} = \arctan\left(-\frac{I_{s2k}}{I_{c2k}}\right) \quad (k = 1,2,3,4).$$

The expression (28) clearly shows a 2nd order harmonic component at the converter DC side due to the negative sequence component in the inverter input current $\bar{i}_F$ in (1). In addition, the interaction of the fundamental component of the switching vector $\bar{s}$ with the 2nd order harmonic of the DC voltage creates a 3rd order harmonic in the converter poles voltage, which allows a 3rd order (not zero sequence) harmonic current flowing into the grid. So, the 3rd order harmonic in the grid current will produce a 4th order harmonic in the DC current and in the DC voltage, and so on. Therefore, the appearance of odd harmonics of order $h=2k+1$ (k = 1, 2…) on the AC side is a consequence of the presence of even harmonics of order $h=2k$ (k = 1, 2…) on the DC-link voltage and vice-versa.

III. VOLTAGE LOOP CONTROL SCHEME

The shunt APF control scheme is commonly implemented using two control loops (Figure 2): the DC voltage loop and the current loop. The DC voltage control loop is an outer loop usually implemented with a PI regulator and its output is the active current reference needed to maintain the DC-link charged at the required value. The current control loop regulates the APF currents $i_{F,\alpha\beta}$ using the current references $i^*_{F,\alpha\beta}$ computed from the load currents $i_{L,abc}$ and from the output of the DC-link regulator.

As demonstrated in the previous section, the presence of an unbalanced load will lead to even harmonics in the DC-link voltage and odd harmonics at the inverter AC side. The fundamental negative sequence current generated by the unbalanced load is introduced in the APF system by means of the reference generator shown in Figure 2.

There are basically two solutions to eliminate the effects of the undesirable harmonics at the inverter AC side: (1) the fundamental negative sequence component is blocked by the current reference generator [12] and (2) using the DC-link

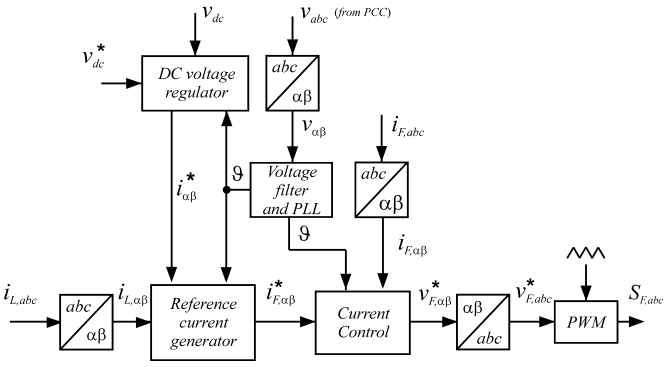

Fig. 2. Block diagram of the APF control.

voltage loop. Note that both strategies are used when the compensation of unbalanced load is not required. This paper is focused on the second approach.

The use of the conventional PI control in the voltage loop (shown in Figure 3) allows the generation of the 2nd order harmonic voltage ripple at DC side. Following the scheme of Figure 3, the voltages v^*_{dc} and v_{dc} are the DC-link voltage reference and DC-link actual voltage, respectively. To start this analysis, we can consider that the DC-link actual voltage is given by (28). To individuate the effects produced by the 2nd order DC-link voltage ripple on the AC side APF current, the other harmonic frequencies are neglected and (28) becomes

$$v_{dc} = \frac{3}{4C}\left[I_{dc} + \frac{I_2}{2\omega_e}\sin(2\omega_e t - \alpha_2)\right] \quad (29)$$

where $I_2 = \sqrt{I_{s2}^2 + I_{c2}^2}, \alpha_2 = \arctan\left(-\frac{I_{s2}}{I_{c2}}\right)$ (30)

The terms I_{s2} and I_{c2} are defined in (17) and (18), respectively. Assuming the reference voltage v^*_{dc} being equal to V_{dc}, the error ε in the PI controller of Figure 3 is

$$\varepsilon = v^*_{dc} - v_{dc} = V_{dc} - \frac{3}{4C}I_{dc} - \frac{3}{4C}\frac{I_2}{2\omega_e}\sin(2\omega_e t - \alpha_2) \quad (31)$$

The DC-link voltage V_{DC} is exactly equal to $\frac{3}{4C}I_{dc}$ if the controller provides no error in steady-state operation for DC components. Doing this assumption, the output of the PI controller becomes

$$i^*_d = (A_2\varepsilon_2 \cdot \sin(2\omega_e t - \alpha_2 + \phi_2)) \quad (32)$$

where $\varepsilon_2 = -\frac{3}{4C}\frac{I_2}{2\omega_e}$, A_2 and ϕ_2 are the magnitude and phase imposed by the PI control for the 2nd order harmonic frequency and superscript "*" means reference value.
Using complex exponentials, the output of the PI DC-link voltage regulator is

$$i^*_d = \frac{A_2\varepsilon_2}{2j}\cdot\left(e^{j(2\omega_e t - \alpha_2 + \phi_2)} - e^{-j(2\omega_e t - \alpha_2 + \phi_2)}\right) \quad (33)$$

It can be seen that the current i_d^* still contains a 2nd order harmonic frequency with both positive and negative sequences. As consequence, the reference currents will contain a 3rd order harmonic component when modulated from (*d*,*q*) to (α,β) reference frame

$$\bar{i}_{\alpha\beta}^* = \frac{A_2\varepsilon_2}{2j}\cdot\left(e^{j(3\omega_e t-\alpha_2+\phi_2)} + e^{-j(\omega_e t-\alpha_2+\phi_2)}\right) \quad (34)$$

As explained before, this 3rd harmonic will generate a 4th harmonic in the DC-link voltage, and so on. To avoid this 3rd harmonic at the APF AC side, the negative 2nd order frequency presented in i_d^* (33) must be cancelled.

A possible solution to solve this problem is the use of a Sinusoidal Signal Integrator (SSI) (resonant regulator) shown in Figure 4. The SSI is tuned on the resonant frequency $\omega_r = 2\omega_e$ ($\omega_e = 2\pi f_{grid}$ rad/s).

As shown in [13], the SSI is able to deal with both positive and negative sequences from the input signal. However, we need to integrate only the negative sequence of the input signal to mitigate with the 3rd harmonic order contained in the reference current i_d^*.

For this reason, the proposed DC voltage regulator uses a single SSI controller, tuned on $\omega_r = 2\omega_e$, as shown in Figure 5. This solution is simpler than the one presented in [14], where two resonant controllers have been used.

The SSI closed loop transfer functions of the outputs y_1 and y_2 respect to the input are given by:

$$\frac{Y_1}{U}(s) = \frac{2k_{i2}s}{s^2 + 2k_{i2}s + \omega_r^2} \quad (35)$$

$$\frac{Y_2}{U}(s) = \frac{-2k_{i2}\omega_r}{s^2 + 2k_{i2}s + \omega_r^2} \quad (36)$$

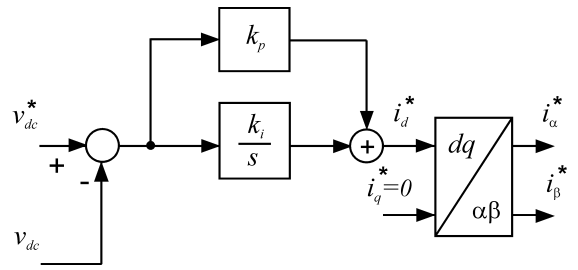

Fig. 3. Conventional DC voltage regulator.

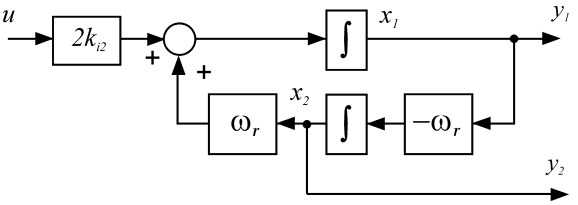

Fig. 4. Sinusoidal Signal Integrator (SSI) block diagram.

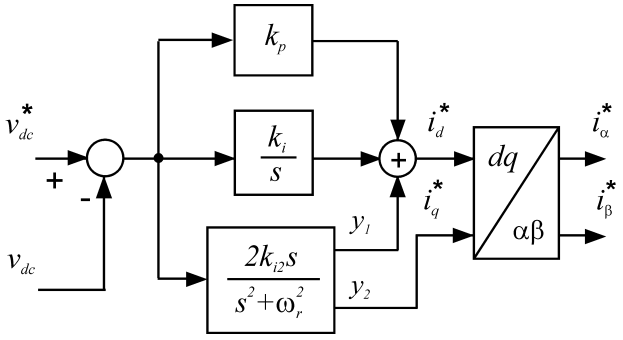

Fig. 5. Proposed DC voltage regulator.

The magnitudes and phases of $\frac{Y_1}{U}(s)$ and $\frac{Y_2}{U}(s)$ are:

$$\left|\frac{Y_1}{U}(s)\right| = \frac{2k_{i2}\omega_r}{\sqrt{(\omega_r^2-\omega^2)^2 + (2k_{i2}\omega)^2}} \quad (37)$$

$$\angle\frac{Y_1}{U}(s) = \tan^{-1}\frac{(\omega_r^2-\omega^2)}{2k_{i2}\omega} \quad (38)$$

$$\left|\frac{Y_2}{U}(s)\right| = \frac{\omega_r}{\omega}\left|\frac{Y_1}{U}(s)\right| \quad (39)$$

$$\angle\frac{Y_2}{U}(s) = \angle\frac{Y_1}{U}(s) - \frac{\pi}{2} \quad (40)$$

According to (40), the regulator outputs y_1 and y_2 are always sinusoidal with the same amplitude and being always phase-shifted by 90 electrical degrees at steady-state.

Since both SSI's internal states x_1 and x_2 are used in the scheme of Figure 4, only the negative 2nd order harmonic will be integrated. Based on these characteristics, the controller output of Figure 4 is

$$\bar{i}_{dq}^*(s) = \left[\frac{Y_1}{U}(s) + j\frac{Y_2}{U}(s)\right]\cdot\varepsilon(s) \quad (41)$$

Neglecting the DC terms, the SSI's output in the time domain is

$$\begin{aligned}\bar{i}_{dq}^* = &\left(A_{y1}\varepsilon_2\sin(2\omega_e t-\alpha_2+\phi_{y1})\right)- \\ &j\cdot\left(A_{y2}\varepsilon_2\sin(2\omega_e t-\alpha_2+\phi_{y2})\right)\end{aligned} \quad (42)$$

By taking into account that A_{y1}=A_{y2} and $\phi_{y2} = \phi_{y1} - \frac{\pi}{2}$, (42) becomes:

$$\begin{aligned}\bar{i}_{dq}^* = &\left(A_{y1}\varepsilon_2\sin(2\omega_e t-\alpha_2+\phi_{y1})\right)- \\ &j\left(A_{y1}\varepsilon_2\sin(2\omega_e t-\alpha_2+\phi_{y1}-\frac{\pi}{2})\right)\end{aligned} \quad (43)$$

Therefore

$$\bar{i}_{dq}^* = \left(A_{y1}\varepsilon_2/j\right)\cdot e^{-j(2\omega_e t-\alpha_2)} \quad (44)$$

This 2nd order harmonic with negative sequence (-2) becomes fundamental frequency also with negative frequency (-1) after the modulation from (*d*,*q*) to (α,β) reference frame as follows:

$$\bar{i}^{*}_{\alpha\beta} = \left(A_{y1}\varepsilon_2 / j\right)\cdot e^{-j(\omega_e t-\alpha_2)} \quad (45)$$

This negative sequence of fundamental frequency will cancel the negative sequence introduced by the APF current reference generator (see Figure 2). Therefore, the 2nd order DC-link voltage ripple will be cancelled, attenuating the 3rd order harmonic distortion in the inverter AC side and implicitly in the source currents.

IV. EXPERIMENTAL RESULTS

The APF control of Figure 2 has been implemented on a 25 kVA APF prototype using a switching frequency of 10 kHz equal to the sampling frequency. The inverter interface inductance, L_F, and the input load inductance, L_L, are 250 μH. The DC-link reference voltage of the IGBT inverter has been set at 730 V. The DC link capacitance is 1.3 mF. The whole APF control scheme has been implemented on the dSPACE DS1103 development board. The quantities measured from the system are: the load currents, the APF currents, the PCC line-to-line voltages and the APF DC link voltage.

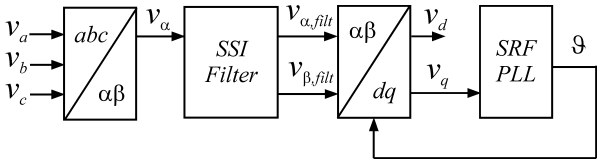

Fig. 6. Phase-Locked-Loop scheme.

The Phase Locked Loop (PLL) scheme is shown in Figure 6. A filter based on the closed loop implementation of the SSI shown in Figure 4 (hereinafter SSI filter) accurately calculates the fundamental frequency of the supply voltages in stationary (α,β) frame [15-16]. It can be seen from Figure 4 that is possible to generate $v_{\beta,filt}$ from $v_{\alpha,filt}$ noting that the state variables y_1 and y_2 are shifted by 90 degrees (see expression (40)). This approach possibilities to deliver a set of balanced and non distorted voltages to the SRF-PLL [16-17] improving its performance.

The detection of reference harmonic currents is done using High-Pass Filters in *dq* rotating frame synchronous with the voltage vector [18].

The current control block has been implemented with a scheme based on a selective harmonic compensation approach [19]. It receives as inputs the APF reference and measured currents in stationary (α,β) reference frame, as well as the position ϑ of the PCC voltage vector computed by means of a PLL scheme (Figure 6). All the tests have been performed with a single-phase linear load connected in parallel with a three-phase diode front-end rectifier as shown in Figure 1.

The APF operation under three different cases will be presented as follows.

A. APF with the conventional PI DC-link voltage controller

The imbalanced load currents can be seen in Figure 7. When the DC-link control is implemented with the conventional PI control of Figure 3, the source currents become highly distorted by a 3rd order harmonic, as it can be seen in Figure 8. A 2nd order harmonic ripple can also be seen in the DC-link voltage, as shown in Figure 9.

B. APF with the proposed DC-link controller

When the proposed control strategy (Figure 5) is implemented, the distortion caused by the 3rd order harmonic on the source current and by the 2nd order ripple on the DC-link voltage is almost cancelled (Figure 10-11). The differences between these two control schemes can also be evaluated by the Fourier analysis of the source currents considering both cases (Figures 12-17).

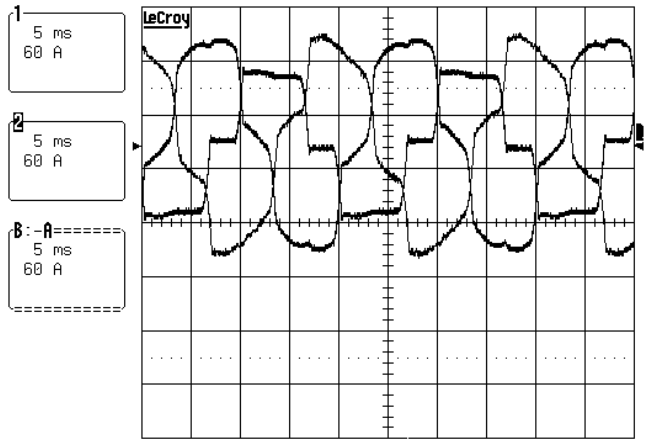

Fig. 7. APF operating with unbalanced loads. Traces 1; 2; B: load currents i_{Labc}.

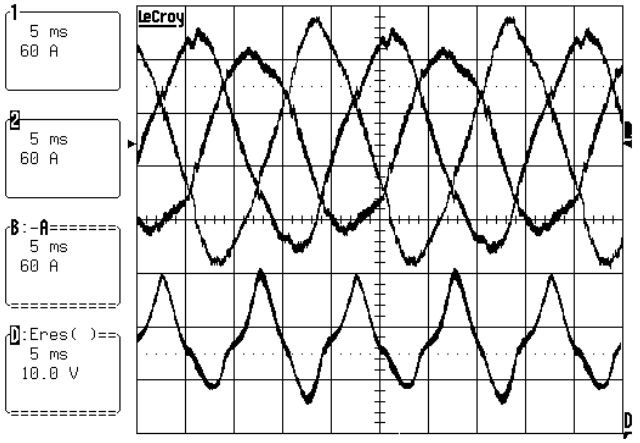

Fig. 8. APF with the conventional PI DC-link voltage controller. Traces 1; 2; B: source currents i_{Sabc}.Trace D: DC-link voltage ripple.

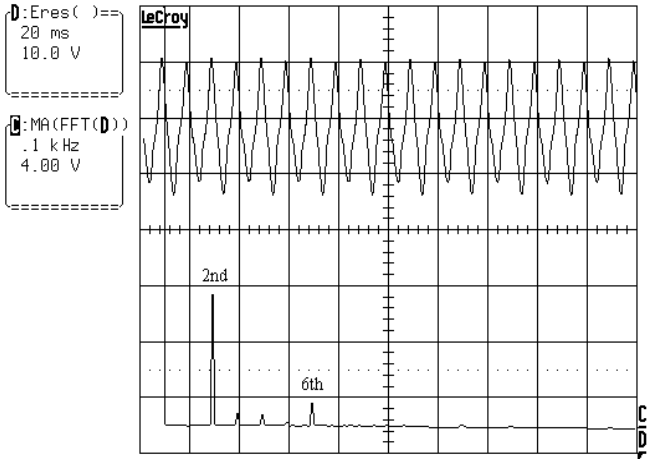

Fig. 9. Fourier analysis of the DC-link voltage using the APF with the conventional PI DC-link voltage controller.

It can be noted that the 3rd order harmonic in the mains current is highly attenuated for the proposed DC link voltage controller.

The non-zero 5th order source current harmonic is due to some non-ideal operating condition of the APF current control loop and does not depend on the DC link voltage loop.

The Fourier analysis of the filter currents for the proposed DC-link controller is shown in Figs. 18-20.

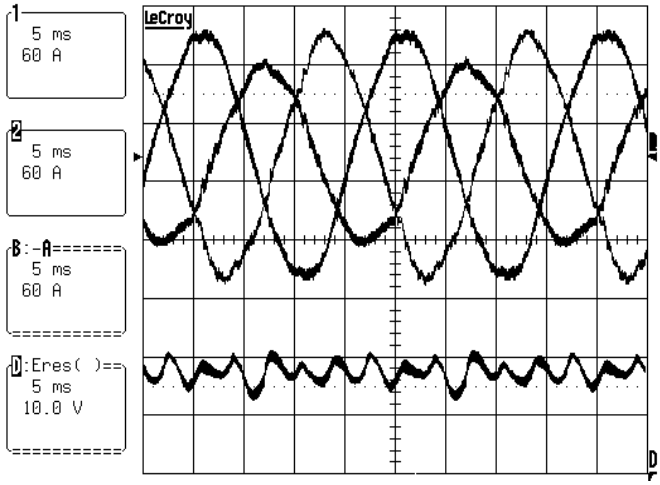

Fig. 10. APF with the proposed DC-link voltage controller. Traces 1; 2;B: source currents i_{Sabc}.Trace D: DC-link voltage ripple.

Note that the amplitude of the third harmonic components of the filter currents (Figures 18-20) is the same of the source currents (Figures 15-17). In addition, the THD of load and source currents are shown in Table I.

C. APF compensating the fundamental negative sequence

If the APF needs to compensate also the fundamental negative sequence of the load currents, then it can be used a control scheme similar with the one presented in Figure 2. The main difference is that a fundamental negative sequence controller must be implemented in the current control loop and

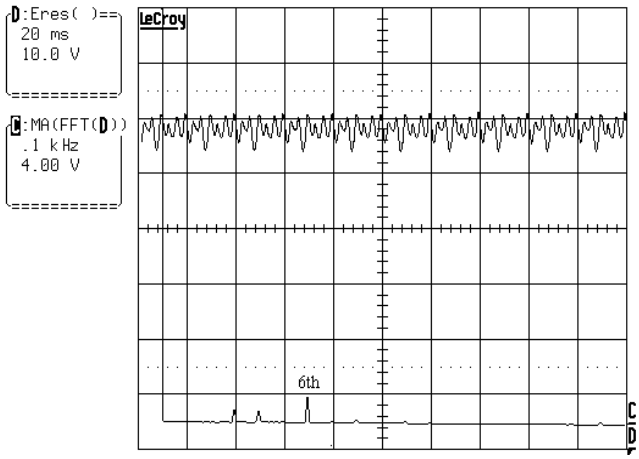

Fig. 11. Fourier analysis of the DC-link voltage using the APF with the proposed DC-link voltage controller.

the DC-link voltage loop must employ the conventional PI controller. In this case, the 2nd order harmonic ripple in the DC-link voltage is increased due to the circulation of all amount of fundamental negative sequence current in the APF. The source currents and the DC-link voltage are shown in Figure 17. It can be seen that the source currents are not pure sinusoidal. This is partially due to the ripple in the DC-link voltage. In this case, the only solution to achieve good APF performance is to increase the DC-link capacitance. The APF designer should take into account the operation with unbalanced loads and oversize the DC-link capacitance accordingly.

TABLE I
THD for source current and load current

	Load current	Source current
Phase A	18%	4.1%
Phase B	26%	5.0%
Phase C	19%	4.5%

V. CONCLUSIONS

The paper performed a theoretical analysis of the shunt Active Power Filter (APF) operating with unbalanced loads. It has been clearly demonstrated that a DC-link voltage ripple at twice the grid frequency appears when the APF attempts compensating the negative sequence of the load currents. As consequence, the source currents become distorted by a 3rd order harmonic. A simple DC link voltage controller has been proposed to block the fundamental negative sequence current component. As a result, the DC link voltage ripple has been almost cancelled, without increasing the DC link capacitance.

If the APF needs compensating also the fundamental negative sequence of the source currents to balance the source currents, then the DC link capacitance must be increased to reduce the DC link voltage ripple. Otherwise, the APF performance deteriorates. Experimental results with a 25 kVA shunt APF prototype are provided to validate the effectiveness of the proposed DC link voltage controller.

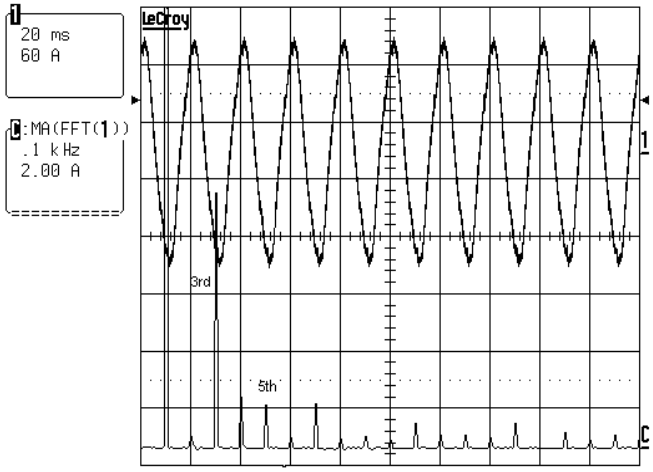

Fig. 12. Fourier analysis of the source current i_{Sa} using the APF with the conventional PI DC-link voltage controller.

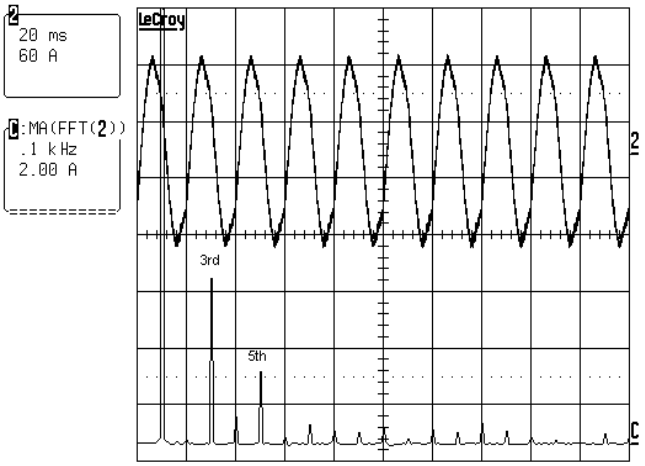

Fig. 13. Fourier analysis of the source current i_{Sb} using the APF with the conventional PI DC-link voltage controller.

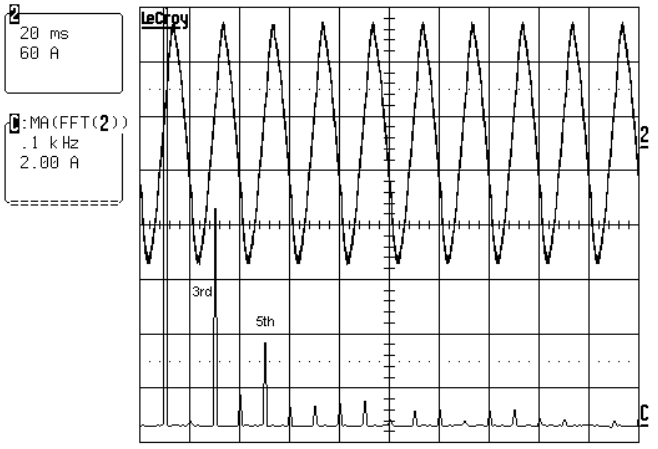

Fig. 14. Fourier analysis of the source current i_{Sc} using the APF with the conventional PI DC-link voltage controller.

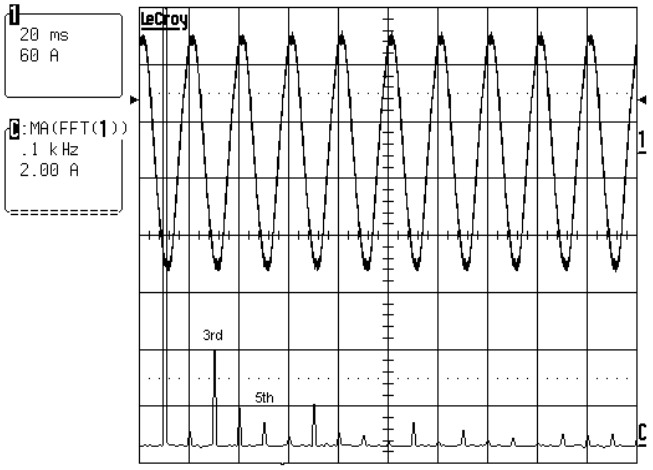

Fig. 15. Fourier analysis of the source current i_{Sa} using the APF with the proposed DC-link voltage controller.

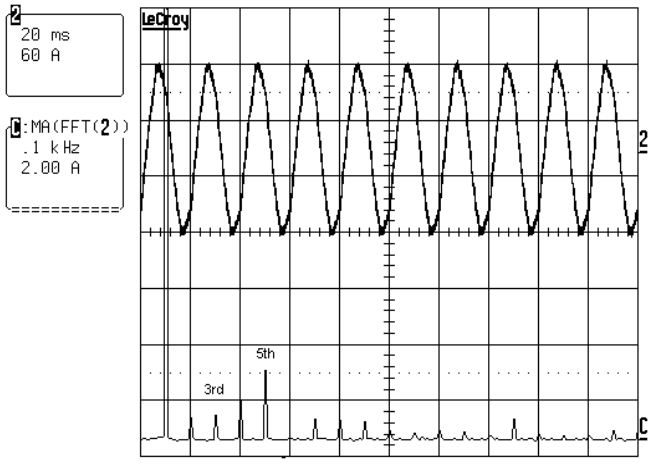

Fig. 16. Fourier analysis of the source current i_{Sb} using the APF with the proposed DC-link voltage controller.

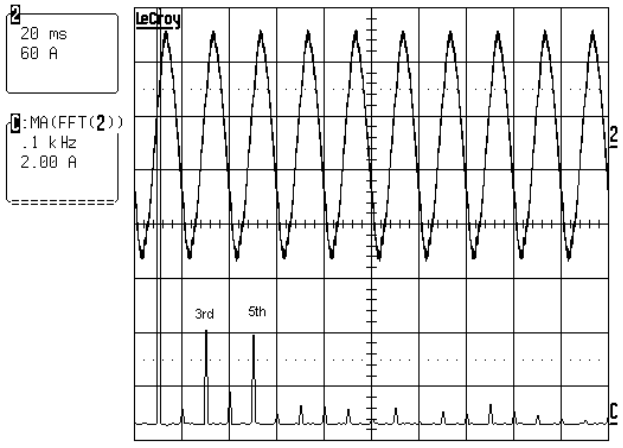

Fig. 17. Fourier analysis of the source current i_{Sc} using the APF with the proposed DC-link voltage controller.

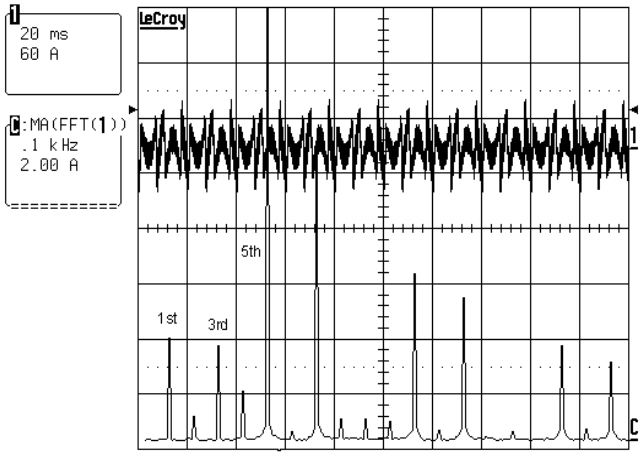

Fig. 18. Fourier analysis of the filter current i_{Fa} using the proposed DC-link voltage controller.

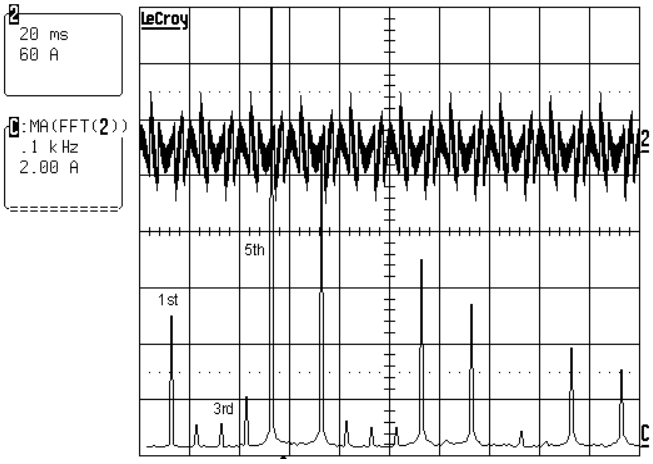

Fig. 19. Fourier analysis of the filter current i_{Fb} using the proposed DC-link voltage controller**.**

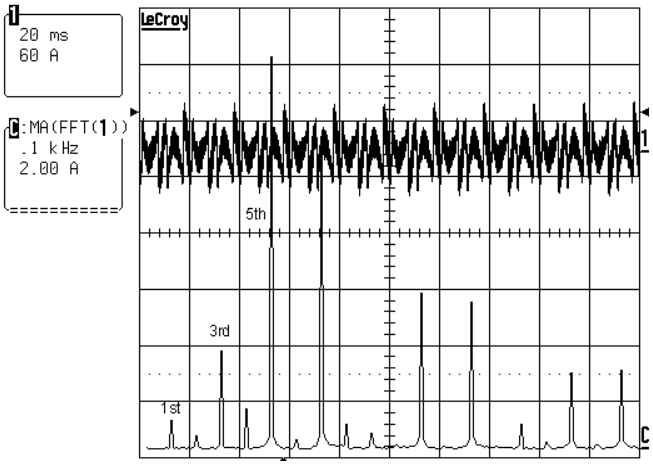

Fig. 20. Fourier analysis of the Filter current i_{Fc} using the proposed DC-link voltage controller.

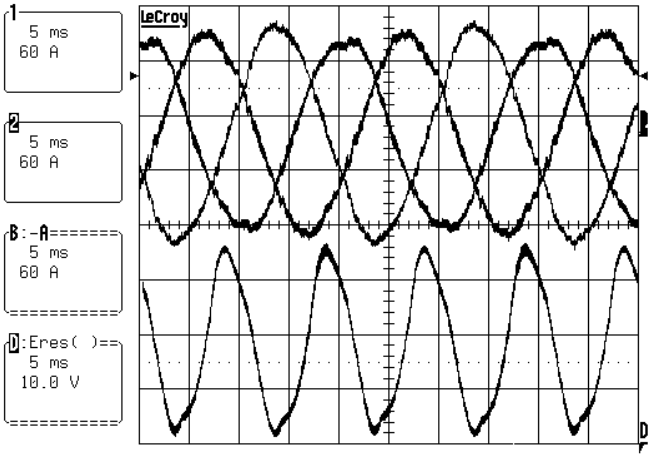

Fig. 21. APF compensating unbalanced load. Traces: 1,2,B: source currents i_{Sabc}. Trace D: DC-link voltage ripple.

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BIOGRAPHIES

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Alberto Tenconi received the M.Sc. and the Ph.D. degrees in electrical engineering from the Politecnico di Torino, Turin, Italy, in 1986 and 1990, respectively. From 1988 to 1993, he was with the Electronic System Division of the FIAT Research Center, where he was engaged in the development of electrical vehicle drive systems. He then joined the Department of Electrical Engineering, Politecnico di Torino, where he is currently a Full Professor. He is the author of more than 120 papers published in international journals and conference proceedings. He is a reviewer of international journals and Associate Editor of IEEE Transactions on Industrial Electronics. His fields of interest are high-performance drive design, new power electronic device applications, and nonconventional electric machines development. He has participated both as a designer and as a scientist in many national and European research programs.