DESIGN CRITERION FOR ZCZVT SINGLE-PHASE INVERTERS WITH MAGNETICALLY-COUPLED AUXILIARY POLE

Mário L. S. Martins[1], Carlos M. O. Stein[1], José R. Pinheiro[2] e Hélio L. Hey[2]
[1]PROCEN - GEPEP, Universidade Tecnológica Federal do Paraná - UTFPR
Pato Branco, PR, BRASIL
mlucio@utfpr.edu.br, cmstein@utfpr.edu.br
[2]GEPOC, Universidade Federal de Santa Maria - UFSM
Santa Maria, RS, BRASIL
hey@ctlab.ufsm.br, renes@ctlab.ufsm.br

***Abstract* – This paper presents in detail a design methodology for Zero-Current Zero-Voltage Transition inverters with magnetically-coupled auxiliary circuit. These ZCZVT inverters accomplish favorable soft-switching conditions with a magnetically coupled auxiliary voltage which is derived directly from the inverter filter inductor. It ensures no resonant auxiliary circuit, reducing circulating reactive energy. The design methodology takes into account the semiconductor requirements to ensure low switching losses on the assisted IGBT modules, which is very important to ensure the best characteristics of the ZCZVT technique. The theoretical analysis is verified experimentally by means of a 1kW, 40 kHz laboratory prototype. The results prove the high efficiency of the prototype implemented according to the proposed design.**

***Keywords* - Coupled filter inductor, Inverter, Soft-switching, Zero-current transition, Zero-voltage transition.**

I. INTRODUCTION

Since it was commercially introduced in 1983 [1] continual improvements of the IGBT make it the most used power switch for many low and medium power applications [2]. More recently, enhancements in IGBT current capability and blocking voltage allowed a growing perspective to it in high power applications [3], [4]. Besides the aforementioned features, high-input impedance MOS-gate control, low forward voltage drop and fast switching have making the IGBT the predominant semiconductor in several industrial applications, especially in the field of motion control [5], where it provides the use of efficient power conversion systems [6]. Lately the IGBT is almost latch up free and its development has been mostly focused on the reduction of conduction and switching loss by optimizing the cell structure and lifetime control [7]. Indeed there is a trade-off between the IGBT turn-off time and the on state voltage drop [8] that promotes the manufactures investigations on materials, structures and fabrication processes.

In spite of a large variety of blocking voltages, most of IGBTs are available today with a 600 V blocking capability [9]. Depending on the manufacture the 600 V IGBT can be of Punch-Through (PT, or asymmetrical) or Non Punch-Through (NPT, or symmetrical) type. The PT-IGBTs use lifetime killers to enhance the trade-off between turn-off time and on state voltage drop [10]. At high temperatures, they exhibit a large current tail due to the increased carrier lifetime. On the other hand, the NPT-IGBTs technology is based on high carrier lifetime in the drift region and lower emitter efficiency. These devices do not use lifetime killers, consequently are less sensitive to temperature variations. Additionally, NPT-IGBTs [11] provide improved ruggedness, switching loss and paralleling than the PT-IGBTs even though their higher on state voltage drop.

Aiming to alleviate the tail current losses and further improving power density, dynamics and EMI performance of IGBT based power converters; soft-switching techniques such as Zero-Current Transition (ZCT) [12], [13] and Zero-Current Zero-Voltage Transition (ZCZVT) [14], [15], [16], [17] have been used. These Resonant Transitions techniques incorporate soft-switching function into PWM converters with minimum voltage/current stresses and circulating energy. They maintain the semiconductor device ratings and converter control design as close as possible to their PWM hard-switched counterparts. This feature is a consequence of the location of the auxiliary components which are in parallel with main power path.

Once switching turn-off losses associate to turn-off time are minimized, the IGBTs trade-off can be loosen. Nevertheless, the effectiveness of the Resonant Transition techniques relay on the fact that auxiliary circuit losses do not off-set the switching losses saved from main semiconductors. The auxiliary circuit losses are quite dependent on the reactive energy produced by resonant elements that comprises the auxiliary circuit [18]. Hence, an adequate design for the auxiliary circuit is critical to ensure a superior performance. Furthermore, the auxiliary circuit design must take into account the characteristics of the semiconductors technology as well as its constraints in order to in fact reduce their switching losses.

This paper presents a design methodology for the ZCZVT inverter with magnetically-coupled auxiliary circuit [19]. This inverter presents naturally low reactive energy due to the absence of resonant elements in the auxiliary circuit. It is a consequence of the auxiliary circuit energy required for the main switches turn-off to be directly processed by the filter inductor which is magnetically-coupled with auxiliary circuit itself (Figure 1). To also ensure low auxiliary semiconductor losses it is required to consider their technology in the design of the auxiliary circuit. Therefore, the proposed design methodology also takes it into account.

Manuscript received on 27/10/2009. Revised on 15/02/2010. Accepted for publication in 25/03/2010 by recommendation of the Editor Fernando L. M. Antunes.

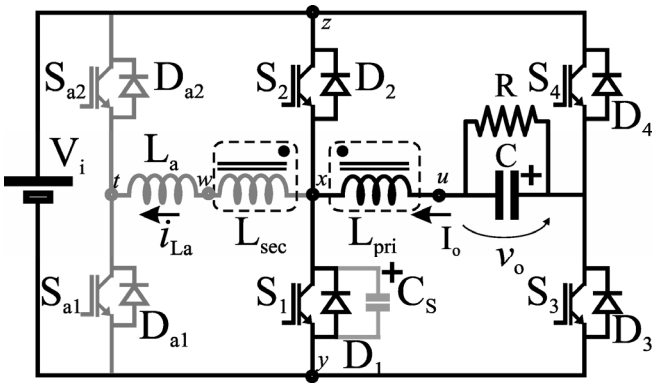


Fig. 1. ZCZVT single-phase inverter with magnetically-coupled auxiliary circuit.

II. IGBT SWITCHING UNDER ZVS AND ZCS

With very few exceptions, semiconductor characteristics in soft-switching mode are typically not specified by the device manufacturers. Nevertheless, various studies have already addressed the behavior of IGBT under soft-switching conditions and have revealed dissimilarities between hard- and soft-switching IGBT counterparts. In soft-switching, the device shows a turn-on voltage over-shoot (in Zero-voltage mode) and a turn-off current bump (in Zero-current mode) that increase the switching power losses (vide Figure 2).

The turn-on voltage overshoot or forward recovery voltage spike, is a consequence of the finite time taken for the modulation of drift region conductivity [2] and are quite dependent on di/dt applied through the device during its turn-on. The voltage spike is proportional to the temperature for PT- and NPT-IGBTs while dynamic saturation voltage, $V_{CE\ (SAT)}$ is proportional to temperature only for NPT-IGBTs Figure 2(a).

The turn-off current spike is a consequence of the sudden evacuation of the stored charge in the internal bipolar base of IGBT when forward voltage is re-applied across the device. The total recovery charge, or forward recovery charge, is the integral of current bump over time and it is a function of applied di/dt at current zero crossing, diode conduction time (t_d), temperature and gate voltage duration (t_b). It is evident that higher carrier density in the drift region leads to more prominent turn-off current tail. Hence, as the carrier transport is heavily dependent on carrier lifetime in PT devices, the increase in recovery charge with temperature is significantly in these semiconductors. In NPT the higher carrier lifetime even at room temperature produces an al-most independent behavior. On the other hand, to reduce the recovery charge in NPT-IGBTs during diode conduction time (t_d) it is required to maintain the gate voltage applied until forward voltage to be re-applied Figure 2(b).

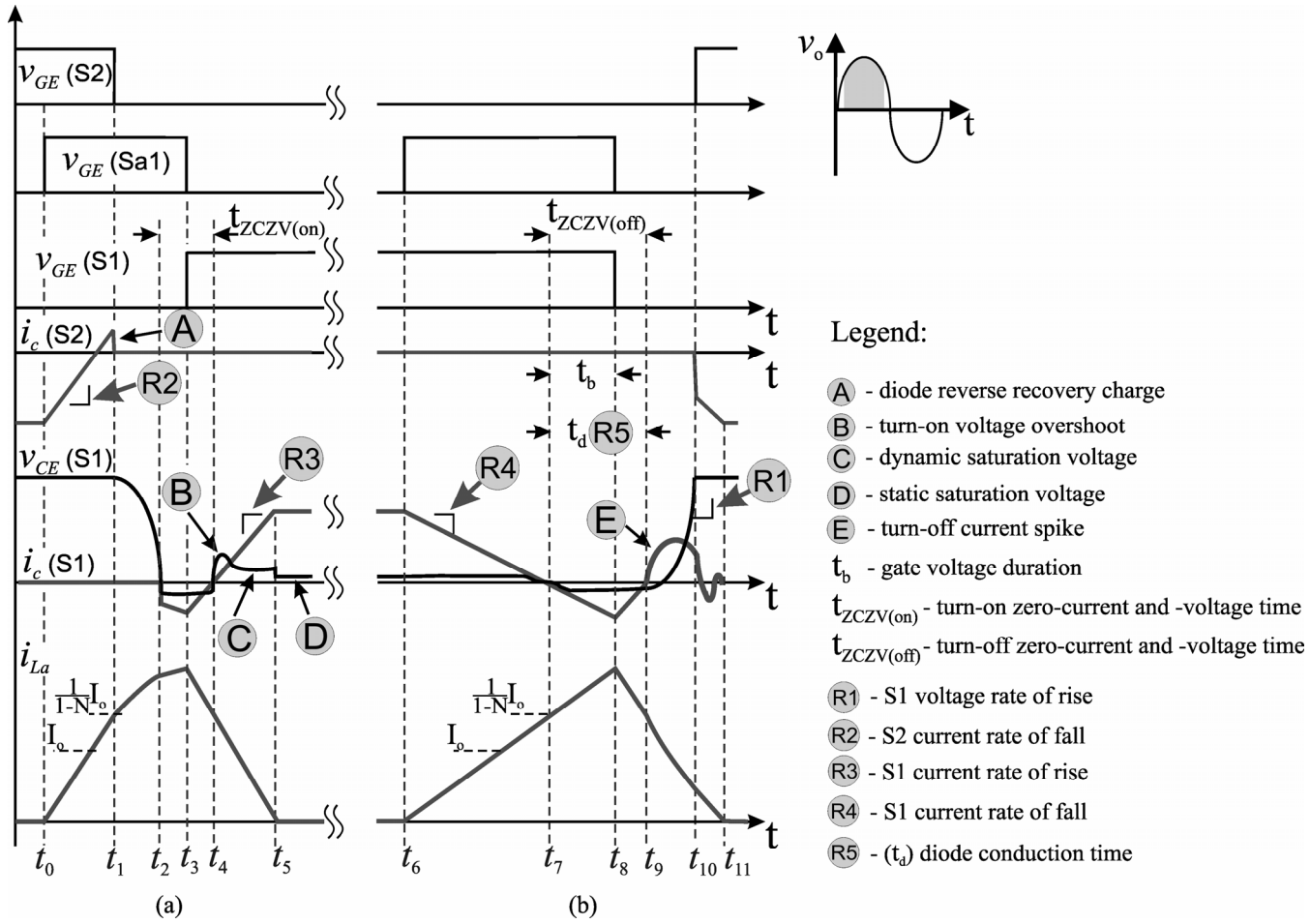


Fig. 2. Theoretical waveforms for the one ZCZVT inverter leg with magnetically-coupled auxiliary pole and detailed IGBT switching waveforms. (a) ZCZVT turn-on operation; (b) ZCZVT turn-off operation.

The co-pack diodes that comprise the PWM pole also contributes to the switching losses since during the diode turn-off transition, its stored minority charge is removed via recombination inside the device, taking a finite time and spent a finite energy to be accomplished. The initial amount of minority charge is a function of the diode forward current and its rate of change.

The Zero-voltage and Zero-current switching condition for inverters are obtained for a PWM pole switch arrangement, as proposed in [20], by forcing the voltage of incoming switch to zero before its turn-on (likewise ZVT) and forcing the outgoing switch current to zero prior its turn-off (likewise ZCT). Controlling the current rate of change for this process, the losses through the PWM pole semiconductors can be reduced.

A. Practical Switching Constrains

As described in previous section and depicted in Figure 2, there are two phenomena that contributes to the switching losses under soft-switching conditions. They are a result of the finite time needed to establish or remove amounts of charge in the wide, light doped drift region of IGBT and diode. These physical constrains must be taken into account by the auxiliary circuit designer in order to not exacerbate their effect on switching losses. Hence, a set of design restrictions are derived from Figure 2 and specified below.

1) Restriction R1 - is the maximum rate of rise of re-applied forward voltage across switch S1. It is associated with turn-off current spike and EMI performance of inverter.

2) Restriction R2 - is the maximum rate of fall of negative current through switch S2. It is associated with co-packed anti-parallel diode recovery losses.

3) Restriction R3 - is the maximum rate of rise of forward current through switch S1. It is related to forward recovery voltage spike.

4) Restriction R4 - is the maximum rate of fall of forward current through switch S1. It is also related to turn-off current spike.

5) Restriction R5 - is the minimum time of conduction for the anti-parallel of S1 that ensures that stored charge can be removed. It is also associated with turn-off current spike.

As carrier lifetime determines the time required to achieve an effective charge level, current rates through the semiconductor must comply with the following expression [21],

$$\frac{di}{dt} < \frac{I_{rated}}{k_n \tau} \tag{1}$$

where:

τ -is the average carrier lifetime.

k_n -is a constant whose value determines the level of losses demanded.

I_{rated} -is the rated conduction current of the semiconductor.

di/dt -instantaneous rate of change of current through the semiconductor.

Hence, restrictions R2, R3 and R4 must observe expression (1).

In terms of current rise (fall) time, expression (1) may be alternatively written as follows,

$$t_{ri}\left(t_{fall}\right) > k_n \tau \frac{I_o(t)}{I_{rated}} \tag{2}$$

where:

t_{ri} -is the semiconductor rise time.

t_{fall} -is the semiconductor fall time.

$I_o(t)$ - is the semiconductor switched current level.

Restriction R5 is associated to the decay of stored charge, which can be given by considering the t_{fall} in expression (2).

III. ZCZVT INVERTER CIRCUIT ANALYSIS

In order to simplify the analysis, the filter coupled inductor is replaced by its cantilever model with its N-port representation [22]; Load current (I_o) is assumed to be positive with direction defined in as shown in Figure 3.

A. ZCZVT inverter with magnetically-coupled auxiliary pole principles of operation

Assuming that load current is flowing in a positive direction, the ZCZVT inverter with a magnetically-coupled auxiliary pole assumes twelve different circuit modes in one switching period, which will be briefly described as follows.

Turn-on Process:

At instant t_0 the auxiliary switch S_{a1} is turned on and the current starts to ramp up through auxiliary inductor L_a. When diode D_2 is off (t_1), capacitor C_s starts to discharge in a resonant fashion. At t_2 voltage v_{Cs} reaches zero and the difference of the secondary and primary windings current flows through diode D_1, establishing the ZCZV condition. At t_3, S_{a1} is turned off meanwhile S_1 is turned on. From t_3 to t_5 auxiliary diode D_{a2} conducts the auxiliary current, demagnetizing L_a. At t_5 current i_{La} reaches zero and the turn-on process is finished.

Turn-off Process:

At instant t_6 the auxiliary switch S_{a1} is turned on and current starts to rise up through auxiliary inductor L_a in a linear fashion. The voltage applied to L_a is directly reflected from the coupled inductor. At t_7 diode D_1 is turned on conducting the difference between the coupled inductor secondary and primary windings currents, establishing once again the ZCZV condition. At t_8 both switches (S_1 and S_{a1})

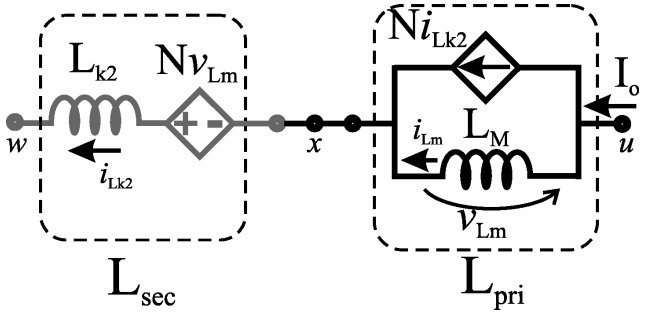


Fig. 3. Coupled inductor model for ZCZVT inverter.

are turned off. From this instant, diode D_{a2} conducts the auxiliary circuit current, demagnetizing L_a. From t_9 to t_{10} capacitor C_s is charged in a resonant way. At t_{10} C_s is fully charged and i_{La} continues to ramp down until it reaches zero at t_{11}, when the turn-off process is finished.

B. Derivation of Restriction R2

To evaluate the current rate of fall through the co-pack diode ($i_D(t)$) of S2, it is required to derive it from the equivalent circuit shown in Figure 4(a). Applying the KVL to the equivalent circuit the following expression can be obtained,

$$i_{D2}(t) = -i_{S2}(t) = i_{Lm}(t) + (N-1)\,i_{La}(t). \quad (3)$$

where:

N - is the turns ratio of coupled inductor coils (N_2/N_1).
N_1 - is the number of turns of primary winding.
N_2 - is the number of turns of secondary winding.
$i_{Lm}(t)$ - is the coupled inductor magnetizing current.
$i_{La}(t)$ - is the current through the auxiliary inductor.

Replacing the circuit relations from the equivalent circuit of the inverter shown in Figure 4(a) and considering that $L_m >> L_a$, one can obtain,

$$L_a \geq \frac{(N-1)\left(NV_o\{\theta\} - (1-N)V_i\right)}{\frac{d}{dt} i_{D2(MAX)}}. \quad (4)$$

where:

V_i - is the inverter bus voltage.
V_o - is the inverter load voltage, which is a function of the output sinusoidal angle $\{\theta\}$.
$di_{D2(MAX)}/dt$ - is the maximum rate of fall of the current through the anti-parallel diode D2.
L_a - is the auxiliary circuit inductance.

Assuming that $\theta = \omega t$, it can be seen by (3) that $i_{Lm}(t)$ will be sinusoidal as the inverter load current I_o is a function of angular position θ. Hence, expression (4) becomes,

$$L_a\{\theta\} \geq \frac{(N-1)\left(NV_o\{\theta\} - (1-N)V_i\right)}{\frac{d}{dt} i_{D2(MAX)}}. \quad (5)$$

C. Derivation of Restriction R3

The current rate of rise through switch S1 is derived from the equivalent circuit shown in Figure 4(b). Applying the KVL to the equivalent circuit the following expression can be obtained,

$$i_{S1}(t) = i_{Lm}(t) + (N-1)\,i_{La}(t). \quad (6)$$

Applying the first derivative to expression (6) and solving it to L_a, it can be found that,

$$L_a\{\theta\} \geq \frac{(N-1)\left(NV_o\{\theta\} - V_i\right)}{\frac{d}{dt} i_{S1(MAX)}}. \quad (7)$$

where:

$di_{S1(MAX)}/dt$ - is the maximum rate of rise of the current through switch S1.

D. Derivation of Restriction R4

The current rate of fall through switch S1 is derived from the equivalent circuit shown in Figure 4(c). Applying the KVL to the equivalent circuit the following expression can be obtained,

$$i_{S1}(t) = i_{Lm}(t) + (N-1)\,i_{La}(t). \quad (8)$$

Applying the first derivative to expression (8) and solving it to L_a, it can be found that,

$$L_a\{\theta\} \geq \frac{N(N-1)V_o\{\theta\}}{\frac{d}{dt} i_{S1(MAX)}}. \quad (9)$$

E. Derivation of Restriction R5

The co-pack diode (D_1) conduction time is the time required to the recombination of minority carrier through the IGBT *pn* junction. A rule of thumb consider that,

$$t_d = 2 \sim 4\, t_{fall}. \quad (10)$$

Depending on the semiconductor device, the diode conduction time can range from 50 to 400ns, as can be seen in Table I, which shown this parameter as a function of fall time for three 2-pack IGBT modules with 600V/40A ratings.

F. Effective Duty Cycle (R6)

The voltage and current transition times impose limitations to the maximum and minimum duty cycle of the PWM pole switches, i.e., the current transference from main

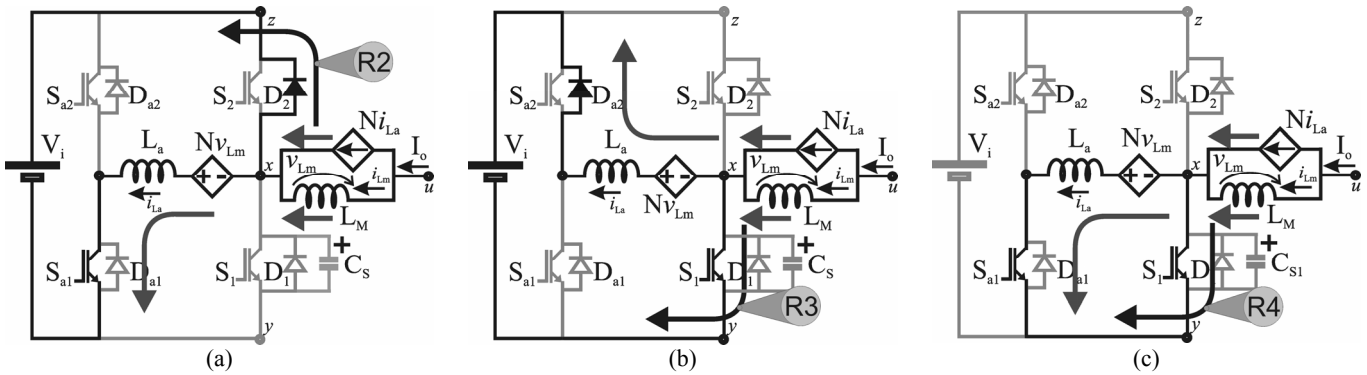


Fig. 4. Equivalent circuit for the restrictions derived from maximum current rate of change. (a) For restriction R2; (b) For restriction R3; (c) For restriction R4.

to the auxiliary circuit limit the inverter output voltage range. The maximum output voltage is obtained from the following equation,

$$V_{o(MAX)} = \left(T - \left(\Delta t_{Loss1}\right)\right)V_{in}. \quad (11)$$

where Δt_{Loss1} is the interval required to transfer the current from one co-pack diode to the auxiliary circuit and vice-versa. This interval is given by,

$$\Delta t_{Loss1} = \left(\Delta t_{E1} + \Delta t_{E2}\right) + \left(\Delta t_{E10} + \Delta t_{E11}\right). \quad (12)$$

where the intervals Δt_{E1}, Δt_{E2}, Δt_{E10} and Δt_{E11} correspond to the inverter operating stage 1, stage 2, stage 10 and stage 11, respectively [19].

Regardless of the very small resonant stages Δt_{E2} and Δt_{E10} the interval Δt_{Loss1} can be approximate by the sum of the linear stages Δt_{E1} and Δt_{E11}.

Thus, the maximum possible duty cycle is expressed as,

$$\Delta t_{Loss1} = \Delta t_{E1} + \Delta t_{E11}. \quad (13)$$

Substituting the time interval Δt_{E1} and Δt_{E11} from the circuit equations and also considering that $i_{Lm}(t_0) = I_o$, and $i_{La}(t_{10}) = 2I_o$ it can be found that,

$$L_a\{\theta\} \le \frac{\Delta t_{Loss1}}{\left(\dfrac{1}{(1-N)\left(NV_o + (1-N)V_i\right)} + \dfrac{2}{N\left(V_i - V_o\right)}\right) I_0\{\theta,\phi\}}. \quad (14)$$

Similarly, the minimum output voltage is obtained from the following equation,

TABLE I
2-pack IGBT modules characteristics

Module	Nominal Ratings [A]	t_d (2 x t_{fall}) [ns]	t_{rr} [ns]
VII 50-06P1 #	42.5 (25°) / 29 (70°)	80	50
SK45GB063 +	45 (25°) / 30 (70°)	50	20
2MBI 50N-060 *	50 (25°) / -----	400	35

#IXYS, + Semikron, *Fuji

$$V_{o(MIN)} = \Delta t_{Loss2} V_{in}. \quad (15)$$

where Δt_{Loss2} is the interval required to transfer the current from the auxiliary circuit to one IGBT. This interval is given by,

$$\Delta t_{Loss2} = \left(\Delta t_{E4} + \Delta t_{E5}\right) + \left(\Delta t_{E7} + \Delta t_{E8}\right). \quad (16)$$

where the intervals Δt_{E4}, Δt_{E5}, Δt_{E7} and Δt_{E8} correspond to the inverter operating stage 4, stage 5, stage 7 and stage 8, respectively [19].

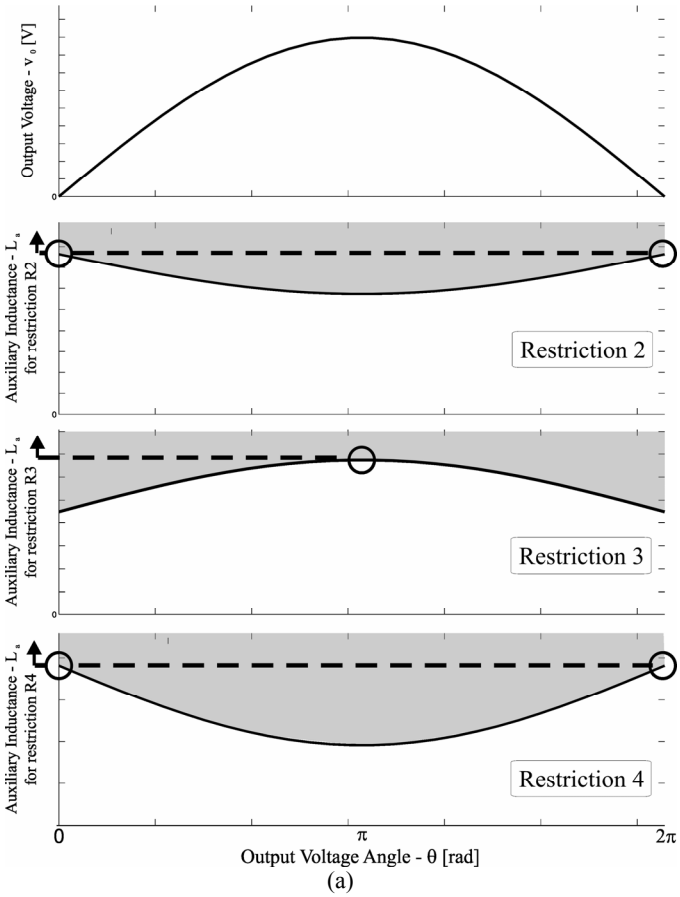
Regardless of the very small stages Δt_{E4} and Δt_{E7} the interval Δt_{Loss2} can be approximate by the sum of the linear stages Δt_{E5} and Δt_{E7}.

Thus, the minimum possible duty cycle is expressed as,

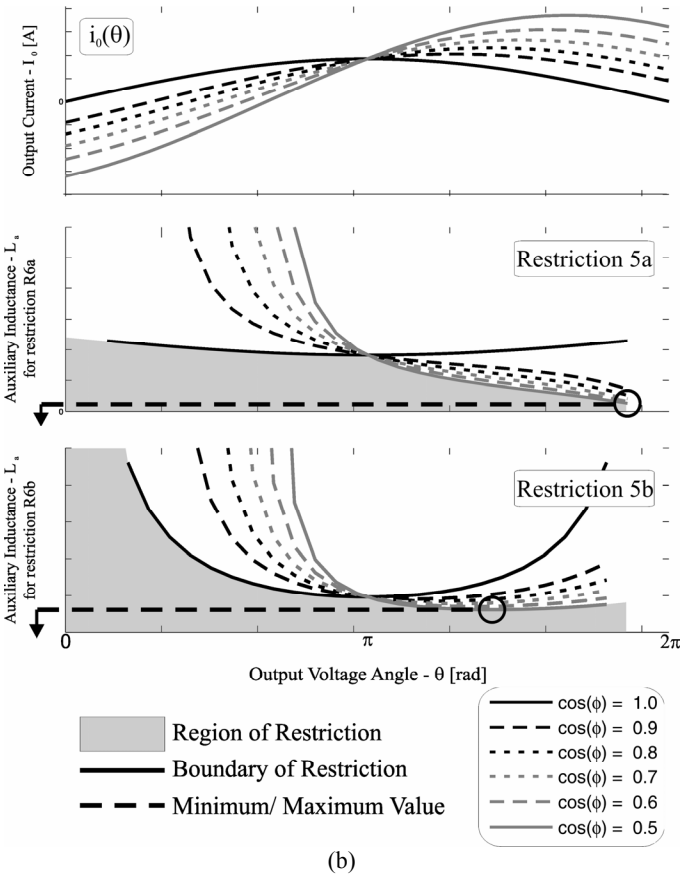
$$\Delta t_{Loss2} = \Delta t_{E5} + \Delta t_{E7}. \quad (17)$$

Substituting the time interval Δt_{E5} and Δt_{E7} from the circuit equations and also considering that $i_{Lm}(t_6) = I_o$, and $i_{La}(t_3) = 2.5I_o$ it can be found that,

$$L_a\{\theta\} \le \frac{\Delta t_{Loss2}}{\left(\dfrac{1}{(1-N)NV_o} + \dfrac{2.5}{V_i - NV_o}\right) I_0\{\theta,\phi\}}. \quad (18)$$



(a)



(b)

Fig. 5. Restrictions for $V_o\{\theta\}$ and load displacement factor $\{\phi\}$.

It can be seen that restrictions R2, R3 and R4 concern the minimum value of auxiliary inductor ($L_{a(MIN)}$) which is dependent of output voltage $V_o\{\theta\}$. Since the output voltage is a function of the angular frequency, the dependence of R2, R3 and R4 of θ is depicted in Figure 5(a). In spite of it, there is a minimum value that satisfies all restrictions, which, in turn, is a function of circuit parameters such as V_i, V_o, N, $di_{D(MAX)}/dt$ and $di_{S(MAX)}/dt$.

On the other hand, restriction R6 concerns the maximum value of auxiliary inductor ($L_{a(MAX)}$) which is dependent of both, output voltage $V_o\{\theta\}$ and load displacement factor $\{\phi\}$. Since the output voltage is a function of the angular frequency, the dependence of R6 of θ and ϕ is depicted in Figure 5(b). Similarly, there is a maximum value of L_a that satisfies all conditions of restriction R6, which is also a function of circuit parameters such as V_i, V_o, N, $di_{D(MAX)}/dt$ and $di_{S(MAX)}/dt$.

IV. AUXILIARY CIRCUIT DESIGN CONSIDERATIONS

To design the auxiliary circuit parameters and components, according to the restrictions defined in Section III, it is required to determine the maximum current rate of change for the IGBT and co-pack diodes that form the PWM pole switches. With these parameters defined, it is also necessary to take into account the inverter specifications that concern the load requirements and other system constrains like the switching frequency and DC bus voltage.

A. Maximum Current Rate of Change of Semiconductors

In order to establish a graphical relation of the auxiliary inductor value (L_a) as a function of the coupled inductor turns ratio (N), it is required to define the maximum current rate of change through the semiconductors using the following expressions.

The maximum allowable current rate of fall (restriction R2) through the co-pack diode can be obtained from the following expression,

$$\frac{d}{dt} i_{\mathrm{D2}(MAX)} \{R2\} = \frac{I_{o(MAX)}}{t_{rr}^{\,2}} \left(2.8\times10^{-6} V_i\right)^2 \quad (19)$$

where t_{rr} is the reverse recovery time, given by,

$$t_{rr} = \frac{2Q_{rr}}{I_{rr}} \quad (20)$$

And Q_{rr} is the reverse recovery charge and I_{rr} is the maximum reverse current.

Hence,

$$\frac{d}{dt} i_{\mathrm{D2}(MAX)} \{R2\} = 282 \, A/\mu s \quad (21)$$

The maximum allowable current rate of rise (restriction R3) through the IGBT can be obtained from the following expression,

$$\frac{d}{dt} i_{\mathrm{S1}(MAX)} \{R3\} = \frac{I_{\mathrm{Nominal}}}{k_n \tau} \quad (22)$$

where k_n is set to one; and τ is set to a general value defined as 1μs [23].

Thus,

$$\frac{d}{dt} i_{\mathrm{S1}(MAX)} \{R3\} = 30 \, A/\mu s \quad (23)$$

The maximum allowable current rate of fall (restriction 4) through the IGBT can be estimated to be the same as for the co-pack diode, and thus,

$$\frac{d}{dt} i_{\mathrm{S1}(MAX)} \{R4\} \approx \frac{I_{o(MAX)}}{t_f} \quad (24)$$

where t_f is set to the sum of t_{fall} and t_{doff} of the IGBT module.

This way,

$$\frac{d}{dt} i_{\mathrm{S1}(MAX)} \{R4\} = 40.5 \, A/\mu s \quad (25)$$

B. Duty-Cycle loss and its restrictions

To establish a graphical relation of the auxiliary inductor value (L_a) as a function of the coupled inductor turns ratio (N), it is required to also define the maximum and minimum possible duty cycles, which are given by (26) and (27) , respectively.

$$\Delta t_{Loss1} = D_{MAX} = k_M M_a T_S \approx 12.5\mu s \, . \quad (26)$$

where:

k_M - is a constant of allowed duty-cycle loss, it varies from 0 to 1.

M_a - is the modulation index $\left(M_a = V_{o(Max)}/V_i\right)$.

T_s - is the switching period $\left(T_s = 1/f_s\right)$.

For this analysis, T_s = 25μs, M_a = 0.49 and k_M is set to 1. and

$$\Delta t_{Loss2} = D_{Min} = k_D T_S = 7.5\mu s \, . \quad (27)$$

where:

k_D - is a constant of allowed minimum duty-cycle, it varies from 0 to 1.

For this analysis k_D is set to 0.3.

C. Inverter Design Constrains

The design parameters for the ZCZVT inverter are defined in Table II. It is considered that the inverter feeds a resistive load and the output filter is a second order (LC) low pass filter. The output voltage frequency is 60 Hz and the switching frequency is 40 kHz.

D. Auxiliary Circuit Parameters

Using the semiconductor parameters described in Table I and the ZCZVT inverter parameters described in Table II, for a load with a displacement factor of 0.8, the graphs of Figure 6 are obtained. The curves traced in Figure 6 shown the maximum and minimum values for inductance L_a in function of turns ratio N. it can be seen that curves for minimum values are slightly influenced by the semiconductor parameters.

By Figure 6 it can be seen that any value below the boundary of min./max. duty-cycle complies with restrictions (14) and (18). Values above this boundary will produce a bed operation of the auxiliary circuit and may damage the circuit. It should be highlighted that the auxiliary circuit does not operate at low output voltages. The minimum voltage permitted for its operation is also defined by D_{Min}.

TABLE II
ZCZVT inverter parameters

Parameter	Value
Load Power	1 kW
Bus Voltage (V_i)	360 V
Output Voltage (V_o)	127 V_{rms}
Switching Frequency (f_s)	40 kHz
Output filter THD	5%
Filter inductor (L)	1.0 mH
Filter capacitor (C)	20 µF

On the other hand, any value above the boundary of maximum di/dt (for the respective semiconductor) complies with restrictions (5), (7) and (9). Values below this boundary will produce excessive switching losses in the IGBT module, even at ZCZVT conditions, which is detailed in Section II.

Hence the choice of the auxiliary circuit parameters between these boundaries permits a better performance of the ZCZVT inverter.

In order to reduce the copper losses in the coupled inductor, which are proportional to the secondary winding copper length, the turns ratio N is chosen as small as possible, hence, N = 0.3. Similarly, inductor L_a is defined as the smallest one, i. e., L_a = 7.14 µH, i.e., it is set on the boundary of max. di/dt for the SK45GB063 module.

V. EXPERIMENTAL RESULTS

To evaluate the effectiveness of the design methodology presented in Section IV, a 1 kW, 40 kHz laboratory prototype has been built its and experimental results are given in Fig. 7. The prototype diagram is the same as shown in Figure 1. The H-bridge ZCZVT inverter with magnetically-coupled auxiliary circuit operate with discontinuous PWM modulation in such a way that only one inverter leg commutates at high frequency (40 kHz) [19]. In the breadboard prototype, both inverter legs are implemented with a 2-pack IGBT module SK45GB063 from Semikron. Since the auxiliary circuit handles a fraction of the inverter power, the auxiliary switches have been implemented with MOSFETs (IRFP460) semiconductors that are suited to fast switching (80 kHz) with very low switching losses. To avoid the conduction of the intrinsic slow switching body diode, an arrangement of two Hyperfast diodes (RHR870) is used. A

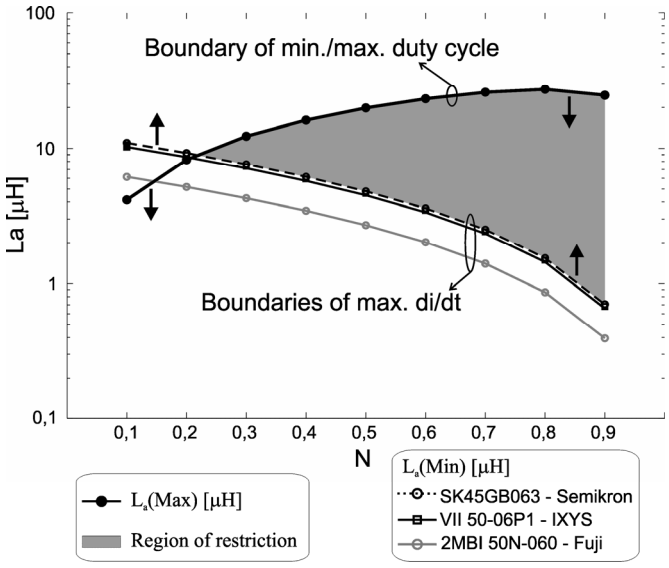
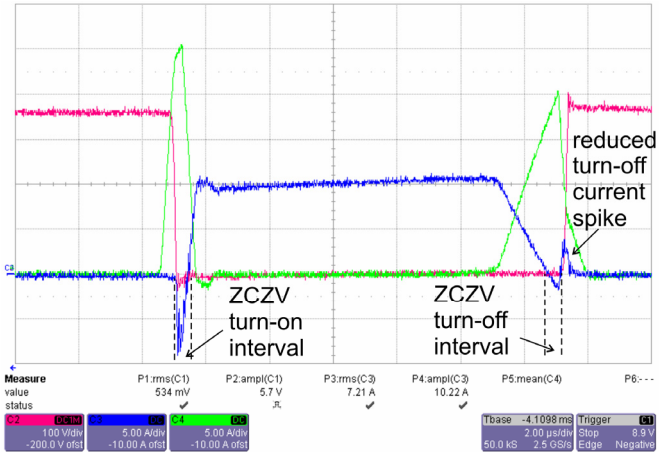
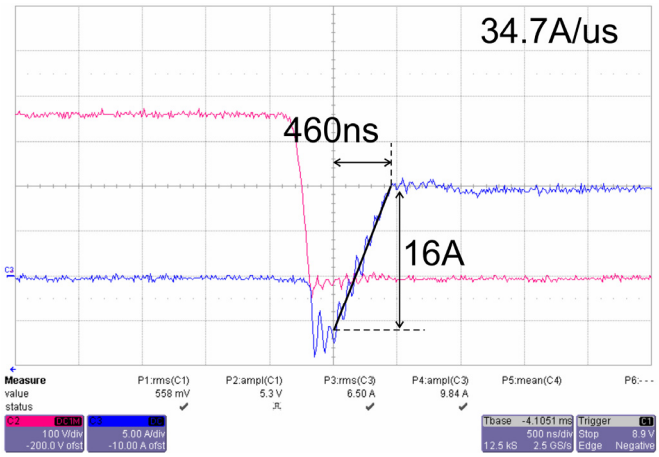


Fig. 6. Auxiliary circuit parameters L_a in function of N for different IGBT modules.



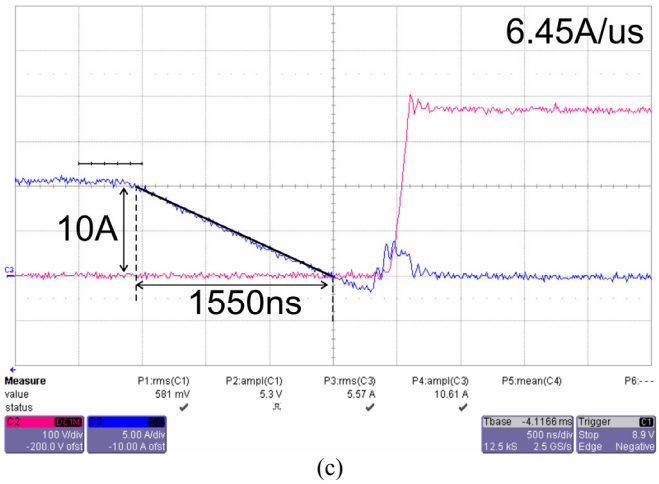
(a)

Scales: v_{CE} 100V/div; i_C 5A/div; i_{La} 5A/div



(b)

Scales: v_{CE} 100V/div; i_C 5A/div



(c)

Scales: v_{CE} 100V/div; i_C 5A/div

Fig. 7. Experimental results for ZCZVT inverter prototype. (a) Main switch waveforms for a switching period. (b) Detail of main switch turn-off process. (c) Detail of main switch turn-on.

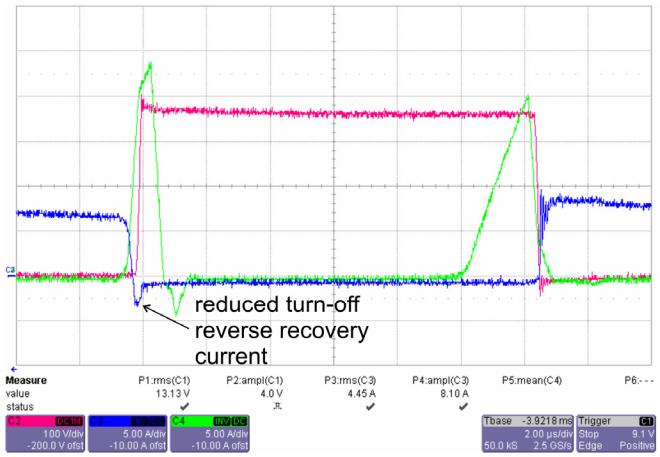


Fig. 8. Co-pack diode waveforms for a switching period.

Scales: v_{CE} 100V/div; i_F 5A/div; i_{La} 5A/div

series diode block the reverse current through the MOSFET and other diode bypass the series connection to provide bidirectional current capability. The coupled inductor is accomplished with an EE-69/33/52 shape E Ferrite Core wrapped with two 30/9 copper coils. A saturable Toshiba SA 14x8x4.5 core is connected in series with the coupled inductor secondary winding to prevent ringing in the auxiliary semiconductor switches.

Figure 7(a) shows a PWM pole main switch waveforms and the auxiliary inductor current. From the waveforms it can be seen that the auxiliary circuit produces very low reactive energy, as the inductor current deviates the PWM pole current in a linear fashion. The Zero-Current and Zero-Voltage conditions intervals for both turn-on and turn-off transitions are highlighted with vertical dotted lines in the figure. It is also pointed out the existence of a current spike right after the switch turns off. It can be minimized enlarging the ZCZV turn-off time, enabling a better reduction of the stored charge in the internal bipolar base of IGBT. Figure 7(b) shows a detail of the switching turn-on process. It can be seen that the current rate of change is about 34.7 A/µs, which is very close to the theoretical value defined by expression (23). On the other hand, Figure 7(c) shows that the current rate of change for the turn-off process is about 6.45 A/µs. The theoretical value for the turn-off current rate of change is approximately six times higher. The current through the module co-pack diode is viewed in Figure 8. It can be seen that the diode turns off with a reduced di/dt. Nevertheless, there is a small reverse recovery current (about 3A) which can be minimized reducing the restriction defined by expression (21).

Hence, from the experimental results, it can be concluded that the restrictions that was took into account during the auxiliary circuit design have been achieved. It should be considered that the design methodology make use of ideal components, such as the coupled inductor, which coupling factor is assumed to be equal to its turns ratio, disregarding the primary and secondary leakage inductances.

The efficiency curve obtained from the ZCZVT inverter laboratory prototype is depicted in Figure 9, along with a dissipative snubber inverter prototype (Undeland snubber)

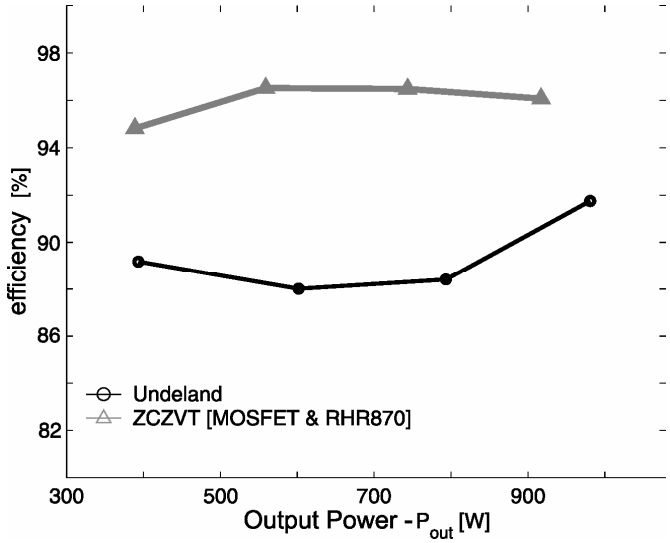


Fig. 9. Efficiency curves.

with same specifications. It can be seen that the ZCZVT inverter presents higher efficiency for the entire load range, achieving 96% at full load. It also can be seen from Figure 9 that, the variable timing control of the auxiliary switches and the low reactive energy results in high efficiency values, even in light load conditions, as the efficiency curve of the ZCZVT inverter is kept above 96% from half to full-load.

VI. CONCLUSIONS

The ZCZVT technology potentially can improve the efficiency of power electronics converters, reducing significantly the switching losses. Nevertheless it only is effective if the semiconductors physical limitations are observed. This way, this paper presented a detailed design methodology for the ZCZVT inverters with magnetically-coupled auxiliary circuit. It takes into account the semiconductor current rates of change to ensure low switching losses to the assisted devices, and inverter operating limits. Complete calculus and analysis of the auxiliary circuit parameters are presented and discussed counting different IGBT module technologies.

The theoretical analysis is verified experimentally by means of a 1kW, 40 kHz laboratory prototype. The results are compared to a dissipative snubber inverter prototype with similar specifications and prove the high efficiency of the prototype implemented according to the proposed design.

The ZCZVT inverter prototype presented higher efficiency for the entire load range, achieving 96% at full load. It also can have been demonstrated that the variable timing control of the auxiliary switches and the low reactive energy results in high efficiency values, even in light load conditions, as the efficiency curve of the ZCZVT inverter is kept above 96% from half to full-load.

ACKNOWLEDGEMENT

The authors would like to express their gratitude to CAPES, CNPq (nº 481195/2007-6, 478154/2009-7 and 554103/2010-9), FAPERGS and “Secretaria de Estado da Ciência, Tecnologia e Ensino Superior - SETI” for their financial

support. They also would like to thank Toshiba do Brasil, Thornton Inpec Eletrônica Ltda, Icotron (an EPCOS company) and XILINX for material support.

REFERENCES

[1] B.J. Baliga, *et al*, "The Insulated Gate Transistor (IGT): A New Power Switching Device", *in Proc. of IEEE Industry Application Society Annual Meeting – IAS83*, pp. 794-803.

[2] S. Pendharkar, K. Shenai, "Zero Voltage Switching Behavior of Punchthrough and Nonpunchthrough Insulated Gate Bipolar Transistors (IGBTs)", *IEEE Transactions on Electron Devices*, vol. 45, no. 8, pp. 1826-1835, August 1998.

[3] N.A. Moguilnaia, *et al*, "Innovation in Power Semiconductor Industry: Past and Future", *IEEE Transactions on Engineering Management,* vol. 52, no 4, pp. 429-439, 2005.

[4] D. Vinnikov, "Some Design Considerations for the 6.5 kV IGBT-Based Half-bridge DC/DC Converter", *Eletrônica de Potência*, vol. 13, no. 2, pp. 55-60, May 2008.

[5] V.K. Khana, *The Insulated Gate Bipolar Transistor IGBT: Theory and Design*, IEEE Press, Piscataway, NJ, 2003.

[6] W.R. Araújo, L.C. Leite, S.G. Moreira, V.M. Pereira, A.R. da Silva Jr., "Aplicação de Técnicas de Inteligência Artificial visando Eficiência Energética e Estimação de Parâmetros em Sistemas Motrizes Industriais", *Eletrônica de Potência*, vol. 13, no. 4, pp. 209-216, November 2008.

[7] L. Lorenz, A. Mauder, J.G. Bauer, "Rated Overload Characteristics of IGBTs for low voltage and high voltage devices", *in Proc. of the 36th IEEE Industry Applications Society Annual Meeting,* IAS 2001, pp. 1066-1073.

[8] B.J. Baliga, "Trends in Power Semiconductor Devices", *IEEE Transactions on Electron Devices*, vol. 43, no. 10, pp. 1717-1731, October 1996.

[9] B.J. Baliga, "The future of power semiconductor device technology", *in Proc. of IEEE*, vol. 89, no. 6, pp. 822-832, 2001.

[10] S. Lefebvre, F. Forest, "Turn-off Analysis of The IGBT used in ZCS Mode", *in Proc. of the 6th International Symposium on Power Semiconductor Devices & ICs.*, pp. 99-104, 1994.

[11] G. Miller, J. Sack, "A new concept for a non punch through IGBT with MOSFET like switching characteristics", *in Proc. of the IEEE 20th Annual Power Electronics Specialists Conference,* PESC '89, pp. 21-25, 1989.

[12] G. Hua, *et al*, "Novel zero-current-transition PWM converters", *IEEE Transactions on Power Electronics*, vol. 9, no. 6, pp. 601-606, 1994.

[13] G. Hua, C.S. Leu, F. C. Lee, "Soft-Switching Techniques in PWM Converters", *IEEE Transaction on Industrial Electronics*, vol. 42, no. 6, pp. 595-603, 1995.

[14] C.M.O. Stein, H.L. Hey, "Conversor Boost ZCZVT PWM", *Eletrônica de Potência*, vol. 3, no. 1, pp. 35-41, November 1998.

[15] C.M.O. Stein, H.L. Hey, "A True ZCZVT Commutation Cell for PWM Converters", *IEEE Transactions on Power Electronics*, vol. 15, no. 1, pp. 185-193, 2000.

[16] M.L. da S. Martins, J.L. Russi, J.R. Pinheiro, H.L. Hey, "Zero-Current Zero-Voltage Transition PWM Converters with Magnetically Coupled Auxiliary Circuit", *Eletrônica de Potência*, vol. 13, no. 4, pp. 204-208, November 2008.

[17] C.A. Gallo, F.L. Tofoli, E.A.A. Coelho, L.C. de Freitas, V.J. Farias and J.B. Vieira Jr., "A ZCZVT PWM three-level full-bridge McMurray inverter", *in Proc. of 35th Annual Power Electronics Specialists Conference*, 2004. PESC 04. 2004, pp. 4803-4807, Vol.6.

[18] X. Jing, D. Boroyevich, "Comparison between a novel zero-switching-loss topology and two existing zero-current-transition topologies", *in Proc. of IEEE Applied Power Electronics Conference* APEC '00, Vol. 2, pp. 1044-1048, 2000.

[19] M.L. Martins, *et al*, "Novel Resonant Transition PWM Inverters: Synthesis and Analysis", *in Proc. of the 37th IEEE Power Electronics Specialists Conference*, PESC '06, 2700-2706, 2006.

[20] C.M.O. Stein, *et al*, "Zero-Current and Zero-Voltage Soft-Transition Commutation Cell for PWM Inverters", *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 396-403, 2004.

[21] C.M. Johnson and V. Pickert, "Three-phase soft-switching voltage source converter for motor drives. Part 2: Fundamental limitations and critical assesment", *in IEE proc. of Electric Power Applications*, 1999, vol. 146, no2, pp. 155-162.

[22] D. Maksimovic, R. Erickson, "Modeling of cross-regulation in multiple-output flyback converters" *in Proc. of 14th IEEE Annual Applied Power Electronics Conference and Exposition,* APEC '99, vol. 2, pp. 1066-1072.

[23] J.G. Kassakian, M.F. Schlecht, G.C. Verghese, *Principals of Power Electronics*, Addison-Wesley Publishing Company, Massachusetts, 1991.

BIOGRAPHIES

Mário Lúcio da Silva Martins was born in Palmeira das Missões, RS, Brazil, in 1976. He received the B.S., M.S. and Ph.D. degrees in electrical engineering from the Federal University of Santa Maria, Santa Maria, Brazil in 1999, 2002 and 2008, respectively.

In 2006, he joined the Department of Electronics of the Federal University of Technological – Parana, Pato Branco, Brazil, where he is currently a Professor, lecturing Power Electronics and Electrical Circuit Analysis for the under and pos-graduating courses of Electrical Engineering. His research interests include high-frequency power converter topologies for DC and AC power sources, VSD drives and renewable sources.

Dr. Martins is a member of the Brazilian Power Electronics Society (SOBRAEP) and IEEE Industry Applications, Power Electronics and Industrial Electronics Societies. Dr. Martins was the recipient of the Second Prize Paper Award from the Industrial Power Converter

Committee of the IEEE Industry Applications Society (IAS) at the 2005 IAS Annual Meeting.

Carlos Marcelo de O. Stein was born in Santiago, RS, Brazil, in 1970. He received the B.S., M.S. and Ph.D. degrees in electrical engineering from the Federal University of Santa Maria, Santa Maria, Brazil in 1996, 1997 and 2003, respectively.

Since 2003, he has been with the UTFPR, Pato Branco, Parana, Brazil, where he is currently a Professor. His research interests include high-frequency power converter topologies, power-factor-correction techniques, power supplies, and soft-switching techniques.

Dr. Stein is a member of the Brazilian Power Electronics Society (SOBRAEP).

José Renes Pinheiro was born in Santa Maria, Brazil, in 1958. He received the B.S. (1981) degree from the Federal University of Santa Maria, Santa Maria, Brazil, and the M.S. (1984) and Ph.D. (1994) degrees from the Federal University of Santa Catarina, Florianópolis, Brazil, all in electrical engineering.

Since 1985, he has been a Professor at the Federal University of Santa Maria, where, in 1987, he founded the Power Electronics and Control Research Group (GEPOC). From 2001 to 2002, he was with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, as a Postdoctoral Research Scholar.

Dr. Pinheiro is a member of the Brazilian Power Electronics Society, Brazilian Automatic Control Society, and several IEEE societies.

Hélio Leães Hey was born in Santa Maria, Brazil, in 1961. He received the B.S. (1985) degree from the Catholic University of Pelotas, Pelotas, Brazil, and the M.S. (1987) and Ph.D. (1991) degrees from the Federal University of Santa Catarina, Florianopolis, Brazil.

From 1989 to 1993, he was with the Federal University of Uberlândia, Uberlândia, Brazil. Since 1994, he has been with the Power Electronics and Control Research Group (GEPOC), Federal University of Santa Maria, where he is currently a Professor. From 1995 to 1999, he was Editor of the Brazilian Power Electronics Journal.

Dr. Hey is a member of the Brazilian Power Electronics Society, Brazilian Automatic Control Society, and several IEEE societies.