# ADAPTIVE HYSTERESIS CURRENT CONTROL OF A PWM INVERTER AT CONSTANT MODULATION FREQUENCY APPLIED TO SHUNT ACTIVE POWER FILTERS

R.R. Pereira C.H. da Silva L.E. Borges da Silva G. Lambert-Torres
Federal University of Itajubá - UNIFEI
Itajubá, Brazil
e-mail: rondi@unifei.edu.br; carloschedas@unifei.edu.br; leborges@unifei.edu.br; germano@unifei.edu.br

B. K. Bose
University of Tennessee
Knoxville, USA
e-mail: bbose@utk.edu

*Abstract*— **This paper proposes a novel adaptive hysteresis current control strategy of a voltage-fed PWM inverter, where the switching frequency always remains constant and the harmonic ripple is minimum, irrespective of dc link voltage fluctuation and load parameter variation. The developed algorithm works well for single-phase as well as multi-phase inverters, although single-phase inverter operation, particularly in active harmonic filter mode, is emphasized in this paper. The algorithm uses fuzzy logic-based current error compensation, and it is simple to implement and does not involve any hysteresis-band calculation. The control strategy has been implemented digitally with a high-speed digital signal processor (TI-TMS320F2812). The proposed scheme has been thoroughly evaluated in laboratory by simulation as well as in experimental studies on a single-phase inverter, and its performance was found to be excellent.**

*Keywords* - **Adaptive hysteresis, current control, PWM, constant modulation frequency, fuzzy control, active harmonic filter, digital signal processor (DSP).**

## I. INTRODUCTION

The hysteresis-band current control PWM technique has been widely used for voltage-fed inverters primarily because of its simplicity of implementation. In addition, it is characterized by the advantages of fast response, inherent peak current limiting capability, and practical insensitivity to dc link voltage and load parameter variation. However, the main drawback of this method is the variation of modulation frequency that causes excessive harmonic ripple in the current wave. A number of hysteresis current control techniques are described in the literature [1]-[15]. Some of them are simple hysteresis current controls, while others are sophisticated adaptive strategies [1][2] to optimize the ripple by maintaining the modulation frequency constant. In the adaptive hysteresis-band current control strategy described by Bose [1] for machine [1]drive system, the band calculation is based on reference current derivative, dc link voltage, and load parameters, which are quite complex to implement in real time, particularly at high switching frequency. The scheme is again difficult to implement for applications such as active power filter and static VAR compensator, where the ac load parameters cannot be easily determined. Malesani's [2] adaptive hysteresis-band technique is more powerful, but it needs information of load current derivatives, dc link voltage, and load parameters to predict the band width for minimization of current error, while maintaining the modulation frequency constant. The technique is more difficult to implement because load current is generally polluted with noise. Both schemes are normally implemented digitally with a high-speed digital signal processor (DSP).

The approach described in this paper uses the adaptive idea proposed by Malesani, but does not use any hysteresis band directly. The main idea here is to look into the current errors between the reference current and the actual current peak in two consecutive half cycles and control the errors to be as symmetrical as possible about the reference current [16]. Indirectly, it tends to control the upper hysteresis-band to be equal to that of the lower band. The strategy is much simpler to implement digitally because it avoids the calculation of current derivatives and the tracking of the load and source parameters. The technique guarantees fast response and clock-synchronized constant switching frequency.

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## II. DESCRIPTION OF ALGORITHM

The adaptive hysteresis current control algorithm proposed in the paper will be developed and validated first for a single-phase H-bridge inverter with *R-L* load, as shown in Figure 1. However, the algorithm is also valid for a three-phase inverter with connected or isolated neutral load of arbitrary load parameters (including counter-electromotive force (counter EMF)). The inverter operates in the usual bipolar mode, i.e., when the device pair 1-3 is switched on, the load current increases with positive slope, whereas the current decreases with negative slope as the pair 2-4 is turned on. It is assumed that the load is highly inductive so that the load current variation is nearly linear with constant dc voltage $V_d$.

Figure 2 explains the algorithm with the help of waveforms. The "clock" wave on the top with time period $T$ and symmetrical half period $T/2$ determines the switching frequency of the inverter. In this project, the switching frequency is maintained constant at 20 kHz, i.e., $T$ = 50 μs. The three vertical dashed lines in every half-cycle, as indicated in the figure, are at 5 μs intervals. The time $t_k = t_0$, $t_1$, $t_2$, etc., as shown at the bottom at half-cycle interval, but lagging by 20 μs from the clock edge, is the reference time

for synchronizing the switching action of the inverter devices. At the middle of the figure, the inverter reference current ($i_{ref}$) is shown as the horizontal line, and the zigzag triangular wave is the actual inverter current ($i_{actual}$) wave, the mean value of which is trying to follow the $i_{ref}$ wave. The current error parameters $\varepsilon(t_0)$, $\varepsilon(t_1)$, $\varepsilon(t_2)$, etc., as shown, are the differences between the peak of actual current wave and the $i_{ref}$ wave at the corresponding reference times shown in the figure, i.e.,

$$\varepsilon(t_k) = i_{ref}(t_k) - i_{actual}(t_k) \quad (1)$$

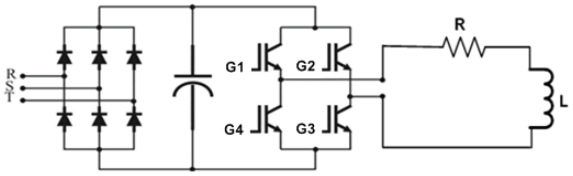



Fig. 1. Block diagram of converter system.

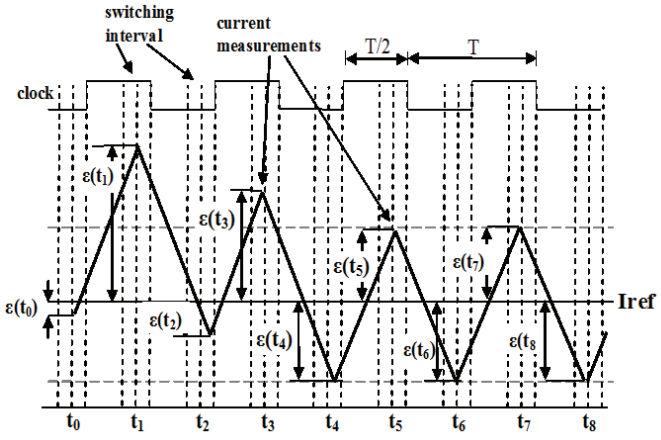



Fig. 2. Waveforms explaining the adaptive hysteresis current control strategy.

The initial part of the actual current wave is shown as unsymmetrical about the reference current wave (i.e., $|\varepsilon(t_1)| > |\varepsilon(t_2)|$ ), indicating that it is in transient condition, whereas in the latter part it is symmetrical (i.e., $|\varepsilon(t_6)| = |\varepsilon(t_7)| = |\varepsilon(t_8)|$), indicating the steady state condition. The algorithm tends to identify the asymmetry of the current error and controls the switching action of the devices, delaying or advancing with respect to the reference time $t_k$ so that it tends to be symmetrical in the steady state. Of course, in the switching control strategy, the variation of $i_{ref}$, if any, should also be taken into consideration.

Assume that initially at $t_k = t_0$, the current error $\varepsilon(t_0)$ is negative as shown. Switching of the inverter devices 1-3 at $t_0$ will increase the current linearly. Then, when the devices 2-4 are switched at $t_1$, the current will start to fall and the peak positive current error is $\varepsilon(t_1)$, as indicated in the Figure 2. There may be three possible scenarios:

Case 1: $|\varepsilon(t_1)| = |\varepsilon(t_0)|$
Case 2: $|\varepsilon(t_1)| > |\varepsilon(t_0)|$
Case 3: $|\varepsilon(t_1)| < |\varepsilon(t_0)|$

Case 1 indicates the steady state condition with symmetrical current errors, and therefore, the next switching action has to occur at the instant $t_2$, where $t_2 = t_1 + T/2$. This means that the duty cycle is 50%, as shown in the latter part of the current wave. Note that 50% duty cycle means that the average output voltage is zero. This is true for the ideal inductive load. However, with counter EMF and/or resistive parameter loads, the duty cycle will deviate from 50% and the slope of the rising current and falling current will be unsymmetrical. For Case 2, which is the actual case in Figure 2, the switching of the device pair 1-3 has to be delayed beyond the instant $t_2$ by $\Delta t_2$ for compensation of the current error asymmetry. For Case 3, on the other hand, the switching action has to be advanced by $\Delta t_2$ for compensation. The total compensation time at $t_k$, is given by the expression

$$\Delta t_k = \Delta t_{k-1} + \alpha \quad (2)$$

where $\Delta t_{k-1}$ = value of cumulative compensation time at time $t_{k-1}$ and $\alpha$ = estimated compensation time at the reference time $t_k$. The value of $\alpha$ depends on the difference between the past two values of current errors $\delta(k)$, where

$$\delta(k) = |\varepsilon(k-1)| - |\varepsilon(k-2)| \quad (3)$$

The compensation proceeds in sequence at every half cycle until the steady state condition is reached. If there is any variation in the reference current, i.e.,

$$\Delta i_{ref}(k) = i_{ref}(k) - i_{ref}(k-1) \quad (4)$$

It should also be taken into consideration for compensation. Therefore, $\alpha$ can be expressed as

$$\alpha = f(\delta, \Delta i_{ref}) \quad (5)$$

where the term $k$ has been dropped for simplicity.

### A. *Fuzzy Control of Compensation Time α*

The optimum value of $\alpha$ is given by the nonlinear relation with $\delta$ and $\Delta i_{ref}$ in (5), and can be estimated by using fuzzy logic. Fuzzy computation in real time is not a problem in high-frequency inverters considering the high speed of the DSP used in the controller. The fuzzy input variables ($\delta$ and $\Delta i_{ref}$) and the output variable $\alpha$ are bipolar, and can be described by triangular membership functions (MF) within a universe of discourse for a practical inverter. Figure 3 shows the membership functions of $\alpha$, where each of the seven fuzzy sets, i.e., negative large (*nl*), negative medium (*nm*), negative small (*ns*), zero (*zr*), positive small (*ps*), positive medium (*pm*), and positive large (*pl*), are described by an asymmetrical triangle. The universe of discourse of $\alpha$ is limited to ±10 μs, as shown in the Figure 3. The variables $\delta$ and $\Delta i_{ref}$ are described by five triangular membership functions (not shown) with overlap of 50%, and the MFs are identical for both the variables. The rule matrix for the estimation relating the fuzzy variables is given in Figure 4. A typical rule for estimation using Mamdani type implication can be read from Figure 4 as

IF δ is NS AND $\Delta i_{ref}$ is ZR THEN $\alpha$ is NS.

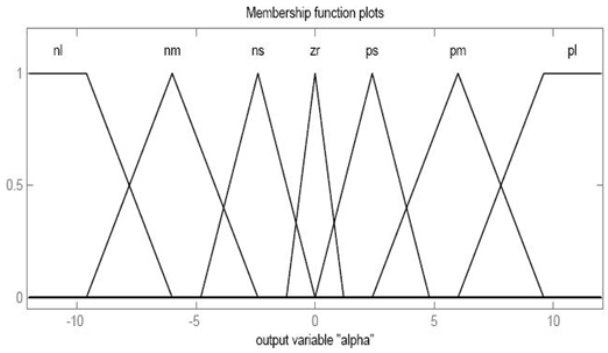



Fig. 3. Membership functions of fuzzy variable $\alpha$.

| $\Delta i_{ref}$ \ Delta ($\delta$) | NL | NS | ZR | PS | PL |
|---|---|---|---|---|---|
| NL | | | PM | PM | PL |
| NS | | | PS | PM | PL |
| ZR | NM | NS | ZR | PS | PM |
| PS | NL | NM | NS | | |
| PL | NL | NM | NM | | |

Fig. 4. Rule table for fuzzy variable $\alpha$ relating with $i_{ref}$ and $\delta$.

All the variables are normalized for convenience of implementation. Figure 4 indicates that a $+\delta$ of higher magnitude will force higher $+\alpha$, and vice versa for $-\delta$ value. On the other hand, $+\Delta i_{ref}$ of higher magnitude will make higher $-\alpha$, and vice versa for $-\Delta i_{ref}$ value. The input variables are fuzzified, the control rules are evaluated, and the corresponding outputs are aggregated to compose the fuzzy output of $\alpha$. Then, $\alpha$ is defuzzified using the simplified version of the Centroid (Center of Gravity) [17] method. The MATLAB-based Fuzzy Logic Toolbox [18] was used to develop the fuzzy control algorithm. All the membership functions and the rule table are iterated several times so that the performance of the fuzzy controller is the best reached.

## III. DSP IMPLEMENTATION METHODOLOGY

The proposed PWM algorithm was fully implemented digitally with a high speed Texas Instruments DSP type TMS320F2812, the features of which are summarized in Table 1.

The 32-bit fixed-point DSP has a computation speed of 150 MIPS (6.7 ns instruction cycle time), and the embedded A/D converter has 16 channels with 12-bit resolution and 80 ns conversion time. Besides, there are three 32-bit dedicated timers and one 32-bit X 32-bit hardware multiplier to enhance the computation speed.

Figure 5 shows the flowchart for implementation of the proposed PWM algorithm. The flowchart, including the fuzzy controller, is executed every half cycle ($0.5T$) of inverter operation, as explained in the task timing diagram of Figure 6. The half cycle interrupt (INT) is generated by a hardware timer in the DSP. At the point named INT the system loads the timer with the calculated value of the IGBT´s switching time $t_d$. After that, the computations for the inverter are first done during the time interval A and it takes typically 10 μs to complete. The inverter IGBT´s switching occurs at the instant F. This time lies within the permitted compensation zone B. The instant of IGBT´s commutations is defined by $\pm\Delta t_k$ which is synchronized about the reference time $t_k$, as shown in the figure as the center of the compensation interval B. The actual advance time ($-\Delta t_k$) or delay ($+\Delta t_k$) is calculated during the interval C in the previous half cycle and implemented with a downcounter with delay time $t_d$. The flowchart with the fuzzy control (shown in Figure 5) is executed in time C (3 μs) just after the switching command is placed to the IGBT´s.

**TABLE I**
**Salient Features of TI- TMS320F2812 DSP**

| |
|---|
| 32-Bit Fixed-Point |
| 150 MHz Frequency |
| Static Cmos With Harvard Architecture |
| Computation Rate: 150 MIPS (6.67 ns Cycle Time) |
| 18k Words Ram And 128k Words Flash Memory |
| 12-Bit, 16-Channel A/D Converter – 80 ns Conversion Time |
| 16 PWM Channels With Two Event Managers |
| Three 32-Bit Timers |
| 32x32-Bit Multiplier |
| Four Power-Down Modes |
| C And Assembly Language Support |

When the downcounter clears, the interrupt signal first measures the current with A/D converter at point E (80 ns) before switching the inverter devices at F (indicating an advanced compensation time $-\Delta t_k$ about the point $t_k$ in the figure). The measurement of current before switching the devices is important because of the noise introduced by the switching.

After the measurement of the current, $\varepsilon(k) = i_{ref}(k) - i_{actual}(k)$ is estimated based on the measured value of $i_{actual}(k)$. The device pair 1-3 is switched on for the positive value of $\varepsilon(k)$, or else, the 2-4 pair is switched on for the negative value of $\varepsilon(k)$, as indicated in the figure. If these criteria are not satisfied, the switching action of device pair is maintained (for transient situation of $i_{ref}$).

At the flowchart in Figure 5, the adaptive scale factor $\varepsilon_s(k)$ is calculated for the variable $\delta$ and then used to compute $\delta(k)$ pu by the expression

$$\delta(k)pu = \frac{\delta(k)}{\varepsilon_s(k)} = \frac{[\,|\,\varepsilon(k-1)\,| - |\,\varepsilon(k-2)\,|\,]}{\varepsilon_s(k)} \qquad (6)$$

where $\varepsilon_s(k) = |\varepsilon(k-1)| + |\varepsilon(k-2)|$ is given by the sum of the previous consecutive positive and negative current errors. The adaptive scale factor essentially gives slope-sensitive correction of $\delta(k)$ pu, which means the $\delta(k)$ pu parameter decreases with higher current slope, and vice versa. Both $\delta(k)$ pu and $\Delta i_{ref}$ are the variables of the fuzzy controller that estimates the value of $\alpha$ as shown. The variables $\Delta i_{ref}$ and $\alpha$ are also normalized with fixed scale factor, but are not indicated in Figure 5 for simplicity. Next, the compensation time $\alpha$ is subtracted or added, respectively, from $\Delta t(k-1)$ to calculate the delay time $\Delta t(k)$, as shown in the figure.

The resulting time delay $\Delta t(k)$ is used for computation of downcounting time $t_d$ for the next half cycle.

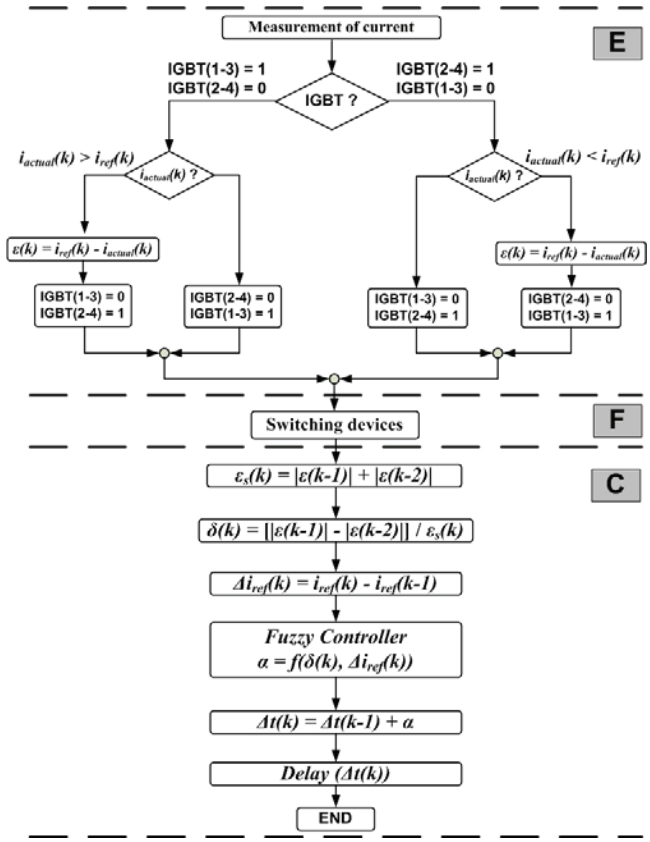
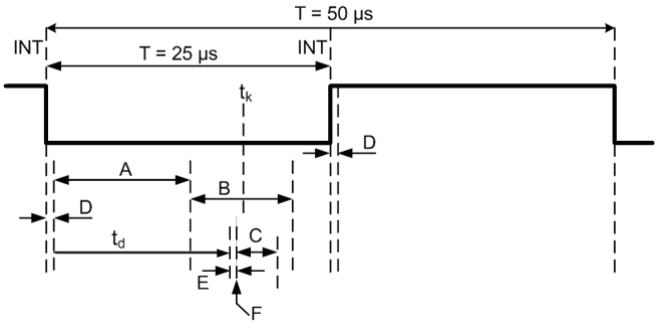



Fig. 5. Flowchart implementation for PWM algorithm.




**A -Time used for other calculations**
**B - Zone for variation of $\Delta t_k$ (10 µs)**
**C - Fuzzy Computation + Downcounter value calculation (around 3 µs)**
**D - Time to load the Downcounter and start it with time $t_d$ (calculated during previous C time)**
**E - Measurement of current + Switching strategy (1 µs)**
**F - Switching of devices**

Fig. 6. Timing diagram of the tasks.

## IV. SIMULATION STUDY

Once the compensation algorithm and the fuzzy controller were developed in detail, a simulation study of the converter system was conducted to validate the proposed control strategy. The MATLAB/Simulink program was used for the simulation study. The fuzzy control program developed by the MATLAB/Fuzzy Logic Toolbox was embedded in the Simulink program. The converter circuit, shown in Figure 1, was simulated with 120 V, 60 Hz single-phase ac supply and large filter capacitor so that dc voltage $V_d$ was reasonably smooth. The inverter frequency was fixed at 20 kHz with nominal passive load of $L$ = 5.0 mH and $R$ = 1.0 Ω. Figure 7 shows the response for a trapezoidal reference current wave varying within ±15 A. The device switching command wave is also included in the figure. Note that the command current slopes are gentle enough so that the PWM actual current wave can follow it. The response with load inductance variation from 5.0 mH to 2.5 mH is shown in the negative half cycle.

Evidently, the current error is larger when the inductance is lower. The constant switching frequency and equal current error are evident during the entire cycle. Figure 8 gives the expanded view of Figure 7 near zero crossing of the current wave highlighting the inductance variation effect. The algorithm tries to control the positive and negative current errors to be equal before and after the inductance variation. The duty cycle of the inverter remains nearly 50% because average load voltage is small. Figure 9 shows the transient response when the reference current changes abruptly from +10 A to –10 A. At initial and final steady states, the slopes of the rising and falling currents are equal and the duty cycle is 50% as shown. At transition of the reference current, the slope is too high for the actual current to follow, and therefore, the device pair 2-4 remains on until the natural falling current reaches the reference value.

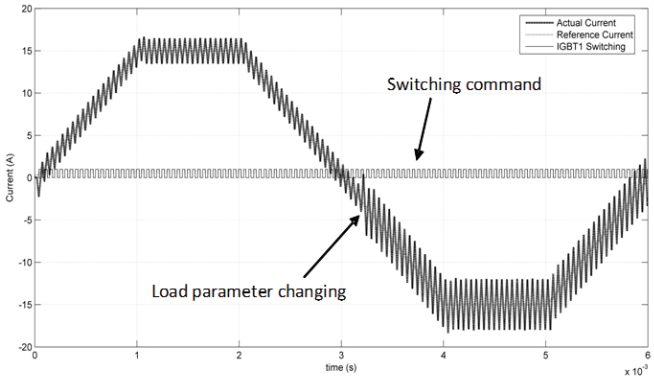



Fig. 7. Trapezoidal current wave synthesis showing load inductance variation (L=5mH to 2.5mH) effect.

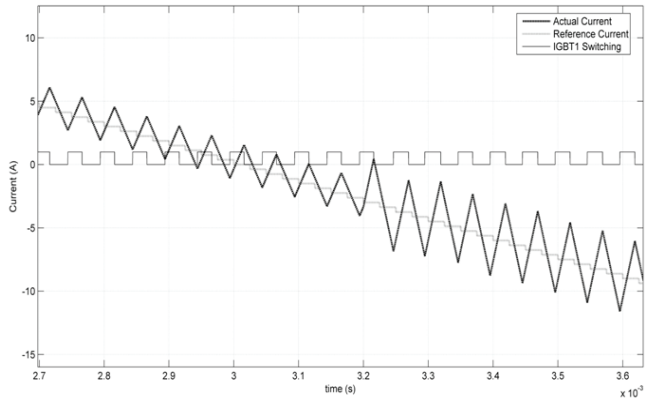



Fig. 8. Load inductance variation effect on current wave in Figure 7 (shown in detail).

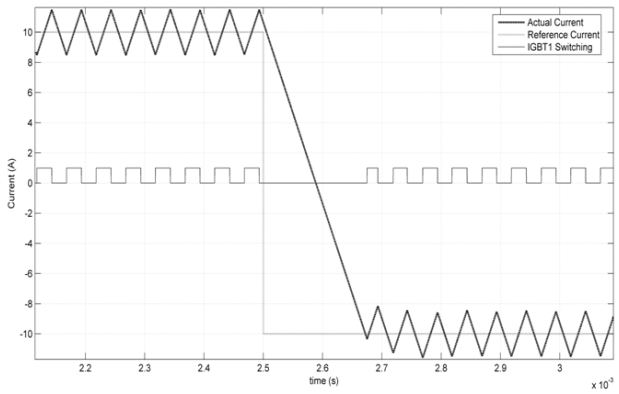



Fig. 9. Transient response of current wave (for +10A to -10A).

## V. EXPERIMENTAL STUDY

Once the validation of the algorithm was completed by simulation study, a set-up was organized in the laboratory for experimental study. A single-phase H-bridge converter system with variable *L* and *R* load, as shown in Figure 1, was available for the study. A Spectral Digital Board based on the DSP type TMS320F2812 was available for the control system. The timing diagram in Figure 6 discusses all the tasks computed and their execution times by the DSP. All the control programs were written in C language, but a few time-critical code segments were used in assembly language that were translated from the C code through Code Composer. All the tasks were repeated every 25 μs, as shown in Figure 6, while maintaining the inverter frequency constant at 20 kHz. The fuzzy controller for real-time implementation in the DSP was somewhat simplified from the corresponding simulation program to economize execution time.

Figure 10 shows the typical inverter current and the device switching waves in steady state for constant reference current. The small difference between the upper and lower error, and the corresponding asymmetry in the switching wave were caused by the error in the current measurement due to large noise. The large current spike at the instant of switching of every half cycle was due to recovery current through the feedback diode of the snubberless inverter. Figure 11 shows the transient response for abrupt change of reference current from +8 A to –8 A, and the corresponding switching wave. It well corresponds with the simulation wave in Figure 9. During the free fall of the current wave, as usual, the devices 2 and 4 remain on. Figure 12 shows the steady state waves with constant reference current, but with load inductance varying from 6.3 mH to 2.5 mH (resistance is the same). The resulting alteration of current slope and error amplitude is evident. After experimental validation of the inverter with *R-L* load, it was decided to test the inverter operation as an active harmonic filter, where the passive *R-L* load was removed and the output was tied to a single-phase 60 Hz ac line. In this mode, the inverter command current wave was composed of a 5$^{th}$ harmonic (300 Hz) current wave at 8 A superimposed with 7$^{th}$ harmonic (420 Hz) current at 5.7 A. The inverter was then tested for harmonic follow-up operation. Figure 13 shows the excellent performance in the harmonic follow-up operation.

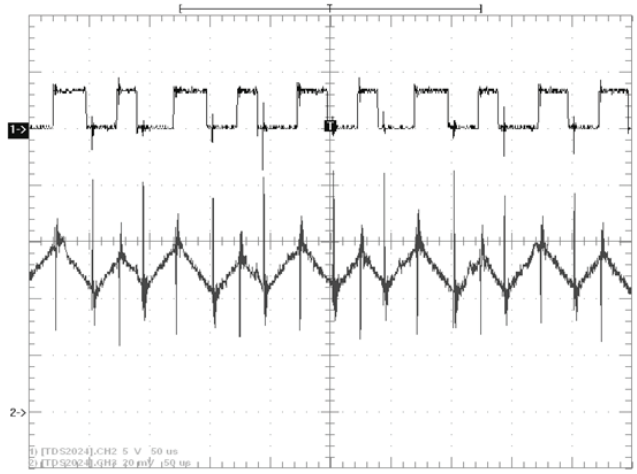


Fig. 10. Experimental steady state switching (top) and current waves (bottom).

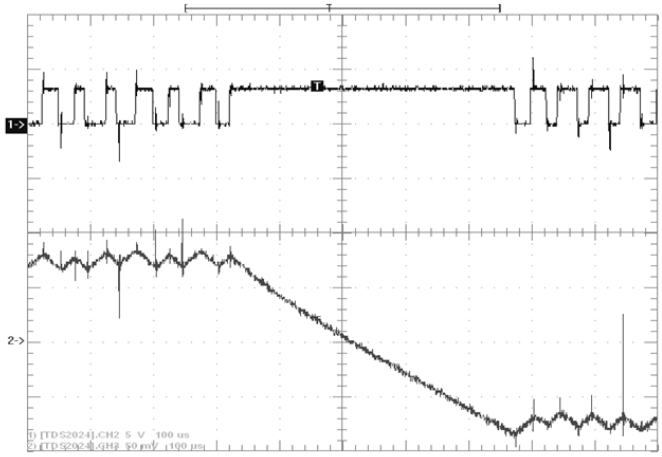


Fig. 11. Experimental transient response for current (from +8 A to -8 A) -L=6.3mH .

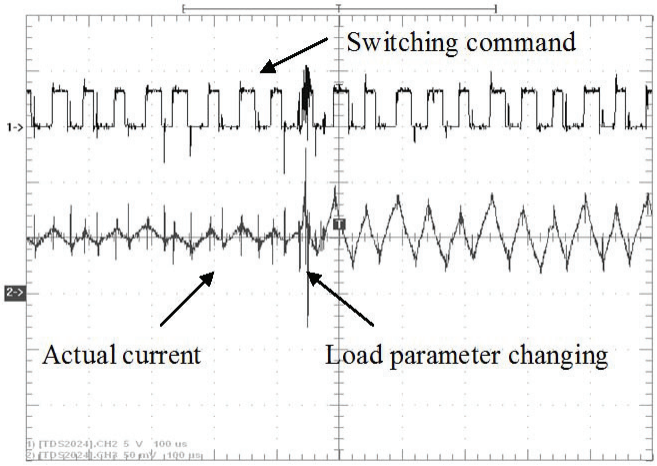



Fig. 12. Experimental switching and current waves for load inductance variation (L=6.3mH to 2.5mH).

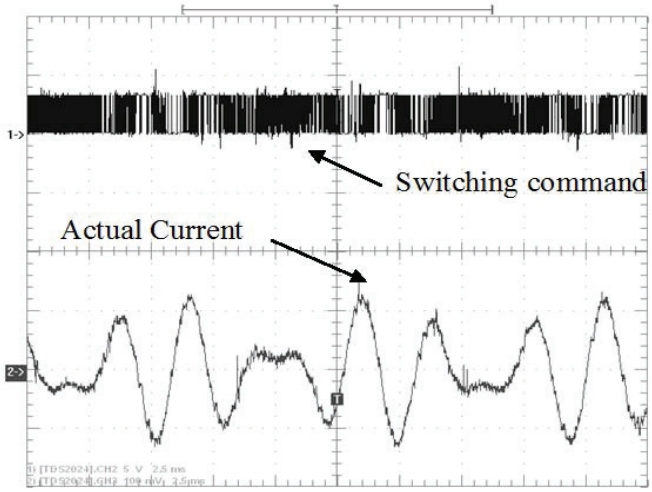



Fig. 13. Experimental current harmonic (5th and 7th) follow-up for active filter operation.

## VI. CONCLUSION

The project successfully demonstrates a new hysteresis current control PWM strategy of a voltage-fed inverter that is fast and adaptive in nature. The harmonic ripple is minimum because the positive current error is controlled to be equal with the negative current error, while operating the inverter at constant frequency. The algorithm is simple to implement and does not need any information about the load and source parameters.

The algorithm has been demonstrated on a single-phase inverter for normal operation with passive *R-L* load as well as active harmonic filter mode of operation. However, it is also valid for a three-phase inverter with arbitrary load and active filter operation. The algorithm uses fuzzy logic for current error compensation. The whole algorithm has been implemented digitally with the high speed DSP type TMS320F2812. The complete inverter with the algorithm was studied extensively by simulation and laboratory experimentation, and performance was found to be excellent.

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**Rondineli Rodrigues Pereira** graduated in computation engineering in 2007 and received M.Sc. degree in electrical engineering in 2009, from Itajubá Federal University, Brazil, where he is currently working toward the D.Sc degree. His research interests include digital signal

processing, adaptive filters, control algorithms for active power filters, harmonics and power quality.

**Carlos Henrique da Silva** received the B.Sc in electrical engineering from the Federal University of Sao Joao Del Rei in 2003, the M.Sc. and D.Sc degree in electrical engineering from the Federal University of Itajubá in 2005 and 2009 respectevely. Currently he is a Professor of the Electrical Engineering Department at Itajuba Federal University (UNIFEI), Brazil. His research interests include active power filters, digital signal processing and control systems.

**Luiz Eduardo Borges da Silva** (M'88) received his B.S. and a M.Sc. degrees in Electrical Engineering from Itajuba Federal University, in 1977 and 1982, respectively, and his Ph.D. degree from École Polytechnique de Montréal, Canada, in 1988. Currently, he is a Professor of the Electronic Engineering Department at Itajuba Federal University (UNIFEI), Brazil. He was a Visiting Professor at University of Tennessee at Knoxville, in 1998. His research focuses on power electronics, electronic power systems, power converters and applications of adaptive and intelligent control in industrial problems.

**Germano Lambert-Torres** (M'90) received the Ph.D. degree in Electrical Engineering from École Polytechnique de Montréal, Canada, in 1990. He received a B.S. and a M.Sc. degrees in Electrical Engineering from Itajuba Federal University, B.S. in Economics from Faculty of Economic Sciences at South of Minas, and a B.S. in Mathematics from Itajuba Faculty of Sciences and Letters.

He is currently a Professor and Dean of the Electrical Engineering Department at Itajuba Federal University (UNIFEI), Brazil. From 1995 to 1996 he was a Visiting Professor at University of Waterloo, Canada. From 2000 to 2004, he was served as Pro-Rector of Research and Graduate Studies at UNIFEI. He serves on a number of committees related to intelligent systems, in IEEE and CIGRE.

**Bimal K. Bose** (S'59-M'60-SM'78-F'89-LF'96) has held the Condra Chair of Excellence (endowed chair) in power electronics at the University of Tennessee, Knoxville, since 1987, where he was responsible for the teaching and research program in power electronics and motor drives. Concurrently, he served as the distinguished scientist (1989–2000) and chief scientist (1987–1989) of EPRI – Power Electronics Applications Center, Knoxville, Tennessee. Prior to this, he was an associate professor of electrical engineering, Rensselaer Polytechnic Institute, Troy, New York (1971–1976).

He is a Life Fellow of the IEEE. He is a specialist in power electronics and motor drives, including power converters, PWM techniques, micro-computer/DSP control, electric/hybrid vehicle drives, renewable energy systems, and AI applications in power electronics and motor drives.