GRID INTERACTION OF A SINGLE-PHASE FEEDER TO A THREE-PHASE CONVERTER

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***Abstract* – This paper describes the digital control strategy of a line-interactive single-phase to three-phase converter. A typical application may be in rural areas supplied by a single-wire with earth return power system. Due to the evolution of the agricultural and industry, some of the local loads (as electronic power converters, computers, communication equipments, etc.) require, nowadays, high power quality that is intended as sinusoidal, symmetrical and balanced three-phase voltage. In addition to that, to maximize the power absorbed from the feeder, the proposed converter, i.e. a three-phase pulse width modulated voltage source inverter, provides a unity line-side power factor. Differently from the conventional solutions, that uses a single-phase rectifier plus a three-phase inverter, the proposed power converter does not process totally the load power, but only the fraction needed to equalize the system. As it also does not manage active power, it does not necessarily require a DC source at the DC link. The digital control strategy, some design criteria and experimental results are presented.**

***Keywords* – Power quality, rural areas, single-phase to three-phase converter, uninterruptible power supply.**

I. INTRODUCTION

In spite of the distribution of electric power is typically three-phase, in some situations the costumers can have access only a single-phase feeder. This happens in residential, light commercial and, mainly, in rural areas. Sometimes a specific local appliance needs three-phase power, which requires some kind of power conversion [1].

Furthermore, new appliances, including information technology and power electronics converters, are sensitive to the power quality, and the local source must be able to satisfy such restrictions. To solve it some kind of single-phase to three-phase (1ϕ-3ϕ) conversion must be provided.

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The 1ϕ-3ϕ conversion can be done using some kind of pulse width modulation (PWM) converter [2]-[8]. In the conventional conversion system, the power is processed twice: by a single-phase rectifier and by a cascaded three-phase inverter. All the topologies presented in the above references have this conventional structure, but they incorporate some kind of upgrade to obtain a better performance, e.g., minimization of the number of power switches, cost reduction, line-side power factor improvement, better load voltage quality, etc.

As the single-phase feeder could directly feed loads like power electronics converters, computers, etc, and considering the typical maximum power limitation of the feeder. It is interesting to maximize the active power availability, which can be obtained with unity power factor. This improvement could be achieved using some kind of power factor corrector or active power filter.

This paper presents a digital control strategy conceived to supervise the operation of a single-phase to three-phase conversion system that improves the local power quality for linear and non-linear loads, and guarantees unity power factor towards the single-phase feeder. The system is shown in Figure 1. The single-phase feeder is connected to the local three-phase bus through a small series reactance (X_{L_S}). A three-phase Static Power Converter (SPC) also is connected to the bus through a second order low-pass filter ($L_{conv}.C_{conv}$).

The SPC controls the local power quality, producing three-phase balanced, symmetrical and sinusoidal voltages. It also controls the single-phase power flow adjusting the local voltage amplitude and phase angle (β). Due to the low impedance imposed by the SPC control, harmonic currents of the load flow locally (between the SPC and the load), except for the harmonic components already present in the single-phase voltage that flows between the SPC and the feeder. In this sense, the SPC also works as an uninterruptible power supply (UPS) for the current harmonics and as a reactive compensator [9]. Additionally, part of the load power is not processed by the SPC, and flows directly from the feeder, which improves the overall efficiency. As the SPC does not deliver active power to the load, it is not necessary to have a

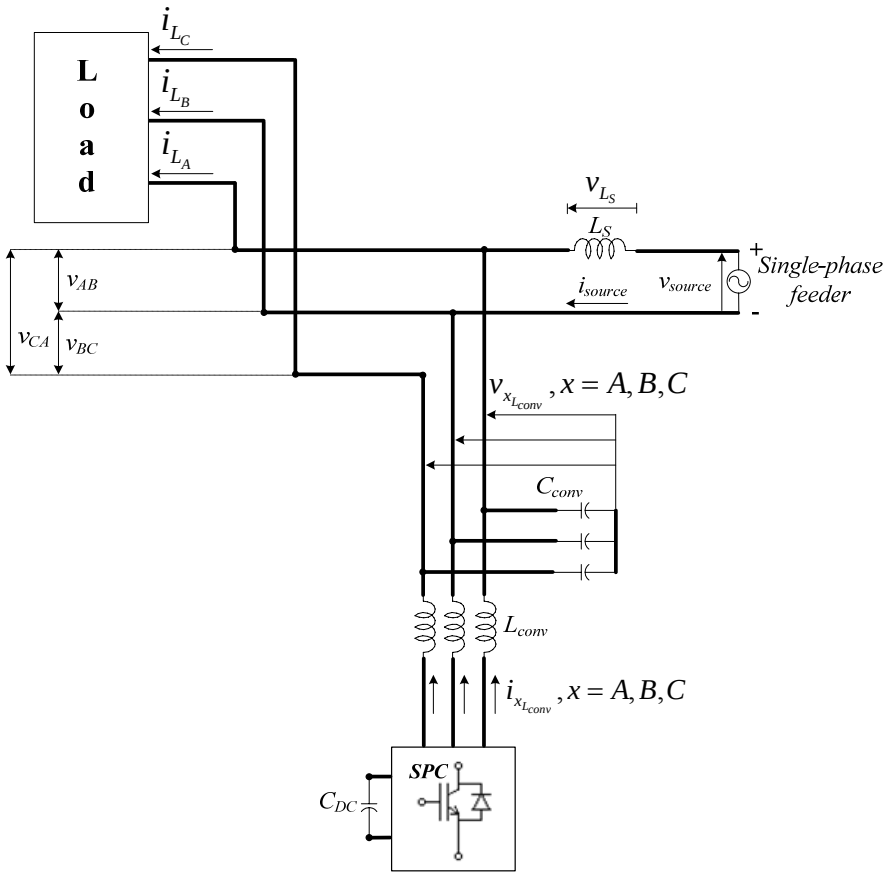


Fig. 1. Single-phase to three-phase conversion system.

DC power source, but if a DC source is available, the system could operate as a line interactive UPS as well, since the islanding situation can be adequately managed [10].

The organization of the paper is the following. In Section II, the basic operation of the converter is described. Since the focus of the paper is on the supervising digital controller, the supervising system control function, namely synchronization and DC link voltage control are only briefly discussed in Section III. Section IV an extensive set of experimental results is provided to demonstrate the proper operation of the SPC in the different typical conditions. Finally, a conclusion of the paper is presented.

II. LOW LEVEL CONTROL FUNCTIONS

According to the previous explanation, one of the control strategy goals is to produce a feeder current that provides unity power factor through the single-phase feeder. As the voltage of this source can vary, it is necessary to adjust both amplitude and β angle of the AC phase to phase voltage produced by the inverter ($\mathbf{V}_{AB}$), as shown in Figure 2.

The inductance that connects the feeder with the SPC is calculated using the power source capacity [11]. The operation point is calculated considering the load active power (P_L) and the amplitude of the actual source voltage (V_{source}), as indicated by (1) and (2). Additional information, to obtain these equations, is presented in Appendix.

As series inductance (L_S) was designed based on the maximum power transfer between the single-phase feeder and the local load on the rated voltage and frequency of the single-phase feeder [11]. It is possible to observe in Figure 3 that, thanks to this inductive coupling, when the system experiences 100% of load variation, i.e., passing from no-load to rated load operation, only 4% of over voltage (Figure 3.a and 3.d) and 4% of power factor reduction are observed at the Point of Common Coupling (PCC) (Figure 3.b and 3.c). Therefore, the specific method adopted to design the L_S inductance helps to limit the correction required to the closed loop controllers presented in this paper. For instance, to compensate variations from no-load to rated load, the β angle needs to be adjusted only by 16° (Figure 3.a and 3.b).

$$\beta = \arctan\left(\frac{2.P_L.X_{L_S}}{\mathrm{V}_{source}^2}\right) \quad (1)$$

$$\mathrm{V}_{AB} = \frac{\mathrm{V}_{source}}{\cos\beta} \quad (2)$$

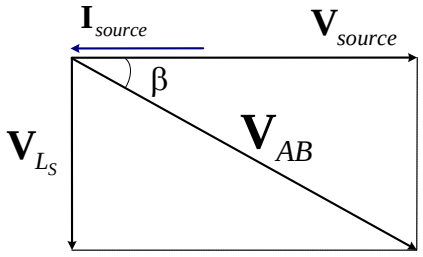


Fig. 2. Phasorial diagram.

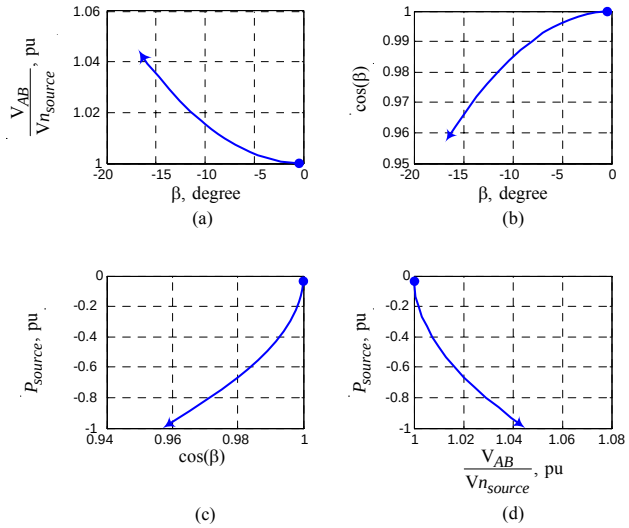


Fig. 3. Static behavior of the system.

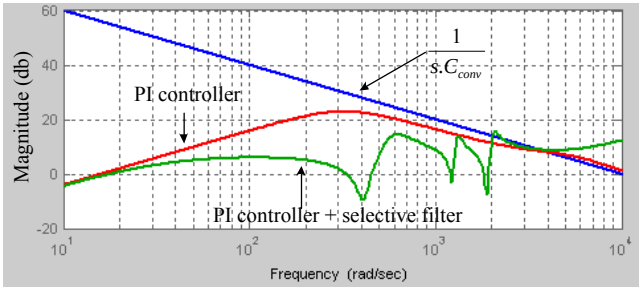


Fig. 4. Equivalent impedance of the inverter.

To guarantee high voltage quality of the SPC, closed loop control of the output current and voltage has been implemented. The proportional-integral controller (PI) was chosen as the control technique. The voltage PI regulator has been associated with a feedforward of the capacitive current and with a multiple selective filter (fundamental, 3rd and 5th harmonics) to minimize the impedance, and to reduce the distortion of the waveform that must be synthesized by the SPC, Figure 4. For the current control loop, an additional feedforward is used to increase the speed of response. The adopted design procedures were explained in detail in [11, 12], and a control block diagram are shown in Figure 5.

III. SUPERVISING SYSTEM CONTROL FUNCTIONS

The supervising controller drives the SPC to achieve the above mentioned goals, related to the load power quality. It was analyzed here the fundamental supervising controller functions, namely voltage loop synchronization with the source voltage and DC link voltage regulation. The k_{lem} and k_{volt} gains represent output to input scale factors while the feedforward gains G1 and G2 are always lower than 1. The SVM block is the space-vector routine. The SPC references ($v^*_{A_{Lconv}}, v^*_{B_{Lconv}}, v^*_{C_{Lconv}}$) are generated inside of the digital signal processor (DSP) whereas, $v_{A_{Lconv}}, v_{B_{Lconv}}, v_{C_{Lconv}}$ are measured according to Figure 5. To obtain them in the αβ reference frame, it is necessary to apply (3) in both signals. The same consideration can be done when currents are used.

$$\begin{bmatrix} v_{\alpha_{conv}} \\ v_{\beta_{conv}} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} v_{A_{conv}} \\ v_{B_{conv}} \\ v_{C_{conv}} \end{bmatrix} \quad (3)$$

A. Synchronization

To guarantee the proper power flow control operation, it is necessary to guarantee that the phase displacement between the single-phase AC bus voltage (v_{source}) and the reference voltage (v^*_{AB}) (internally generated by the control algorithm) is kept as close to zero as possible. Since the reference voltage is generated and updated at the switching (and sampling) frequency, this frequency must be an integer multiple of the source frequency (in this implementation the scale factor is N=200). A digital Phase-locked loop (PLL) controller was implemented to get this result. To explain the controller operation, it is necessary to refer to Figure 6. Suppose there is a small difference between the desired sampling period (T^*_{sw}) and the actual switching period (T_{sw}). Whereas $e(k)$ is call the phase error at the instant $k.T_{source}$. T_{source} is the source voltage period. According to (4), at $k.T_{source}$, the sampling period is increased, so as to get $e(k+1)=0$, at the end of next line period. In order to do that, the increment of T_{sw}, (5), is equal to the error divided by N, summed to the "memory" of all previous errors, that is stored in variable T_I (integral of the error). This guarantees that after instant $(k+1).T_{source}$ the synchronization error will be equal to zero and, in the absence of other perturbations, will remain equal to zero. In any case, the controller guarantees a dynamic response equal to a voltage source period, which is the faster possible. Particular care must be taken in the implementation to limit the controller action and avoid integral part saturation, in the presence of large perturbations. This is obtained with an anti wind-up algorithm. In (6), Y_{max} represents the maximum allowed variation in the switching period. The dynamic saturation limit (L) is calculated once per sampling cycle, so as to keep the control output within the limit Y_{max}.

$$\Delta T_{sw}(k) = \frac{e(k)}{N} + T_I(k), \qquad T_I(k) = T_I(k-1) + \frac{e(k)}{N} \quad (4)$$

$$T_{sw}(k) = T^*_{sw} + \Delta T_{sw}(k) \quad (5)$$

$$|L| = Y_{max} - \left| \frac{1}{200}.e(k) \right| \quad (6)$$

B. DC Link Voltage Control

When an AC power disturbance is detected, due to a load variation or to a feeder voltage fluctuation, the control system reacts adjusting the V_{AB} (voltage amplitude) in order to alter the power flow at the single-phase feeder.

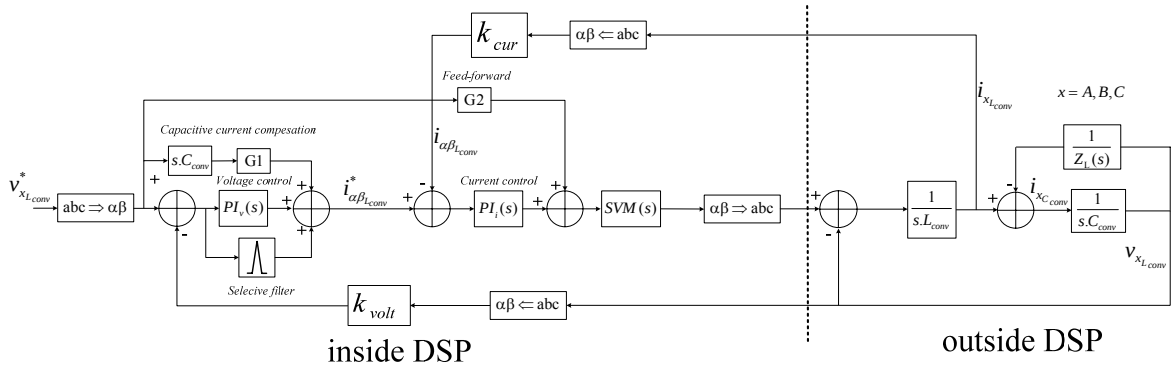


Fig. 5. Inverter output voltage control system in αβ reference frame.

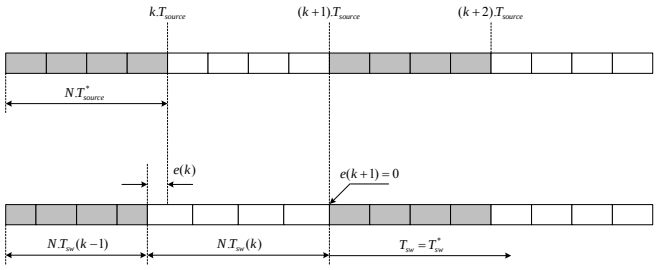


Fig. 6. Timing diagram of dead-beat synchronization.

During such transient, the power unbalance flows through the inverter, changing the DC link voltage. After the transient, whose power demand is supplied by the inverter, the load power is supposed to be constant.

The strategy adopted to regulate the DC link voltage is to exchange the necessary power with the single-phase feeder. In order to maintain the AC bus voltage amplitude constant, this control circuit adjusts only the β angle, based on the DC link voltage error, as illustrated in Figure 7. Considering the power balance condition (7), from the phasor diagram of Figure 2, it is possible to obtain the power flow at the single-phase feeder, when unity power factor is assumed. This is given by (8).

$$P_L + P_{DC} - P_{source} = 0 \tag{7}$$

$$P_{source} = \frac{\mathrm{V}_{AB}.\mathrm{V}_{source}}{2.X_{L_S}}.\sin\beta \tag{8}$$

According to (9), the DC link power flow is:

$$P_{DC} = \mathrm{I}_{DC}.\mathrm{V}_{DC}\,. \tag{9}$$

As the DC link voltage should be almost constant, a relatively large DC link capacitor was used, in this case 4700 μF. It is possible to assume that variations only take place in the DC link current, according to (10).

$$\Delta P_{DC} = \mathrm{V}_{DC}.\Delta\mathrm{I}_{DC} \tag{10}$$

The variation of P_{source} can then be expressed as in (11). Assuming small β values ($\sin\beta \cong \beta$) (11) can be linearized as in (12).

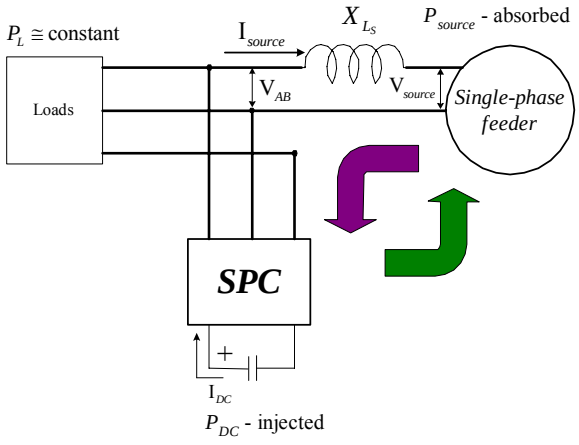


Fig. 7. DC voltage correction.

$$\frac{\partial P_{source}}{\partial\beta} = \frac{\mathrm{V}_{AB}.\mathrm{V}_{source}}{2.X_{L_S}}.\frac{\partial\sin\beta}{\partial\beta}\,, \tag{11}$$

$$\Delta P_{source} = \frac{\mathrm{V}_{AB}.\mathrm{V}_{source}}{2.X_{L_S}}.\Delta\beta\,. \tag{12}$$

Neglecting load power variations (considered as a disturbance input), (7) results in the following control law:

$$\Delta P_{source} = \Delta P_{DC}\,. \tag{13}$$

Substituting (10) and (12) into (13), the relation between a small β angle variation and the DC link current variation can be found (14).

$$\Delta\mathrm{I}_{DC} = \frac{\mathrm{V}_{AB}.\mathrm{V}_{source}}{2.\mathrm{V}_{DC}.X_{L_S}}.\Delta\beta \tag{14}$$

Based on this analysis, it is possible to derive the block diagram of Figure 8, which represents a linear approximation of the system, and allows the design of the DC link PI controller. Similarly to the current and voltage control, the parameters for the PI DC link controller are defined from the open loop gain (G_{OLDC}) (15), 62.83 rad/s of closed loop cut-off angular frequency (ω_{FCLDC}) and 60° of phase margin (mf_{DC}) were used to define the proportional (16) and integral (17) constants k_{propDC} and k_{intDC}.

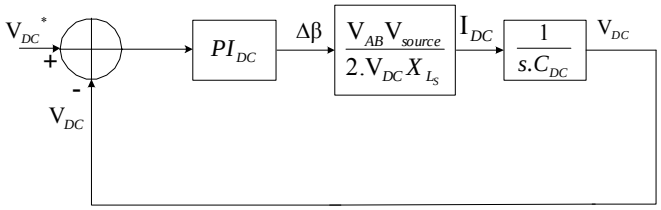


Fig. 8. DC link control.

$$G_{OLDC} = \frac{V_{AB}.V_{source}}{2.X_{L_S}} . \frac{1}{V_{DC}.C_{DC}} \quad (15)$$

$$k_{propDC} . \frac{G_{OLDC}}{\omega_{FCLDC}} = 1 \quad (16)$$

$$k_{intDC} = k_{propDC} . \frac{\omega_{FCLDC}}{\tan(mf_{DC})} \quad (17)$$

IV. EXPERIMENTAL RESULTS

The proposed control strategy has been implemented using a 16-bit fixed-point DSP-based controller ADMC 401 (Analog Devices). This DSP unit represents a powerful tool for digital control implementation for high-performance industrial applications, thanks to its fast arithmetic unit (38.5 ns cycle and 26 MIPS).

A geometric space vector modulation, working with centered pulse, was used to command the switches with 12 kHz as switching and sampling frequency. Therefore, as it was said above, in this application it was used 200 samples of every variable in each 60 Hz period. The resolution for the β angle adjustment is $\frac{360^{\circ}}{200 \text{ samples}} = 1.8 \text{ degrees}/\text{samples}$ due to the PWM updating (one sample for each period of switching). However, 0.03° of resolution is related to the event timer unit (EVU) of the ADMC 401. A 3 kW experimental setup was built to verify the system operation.

A. System Operation

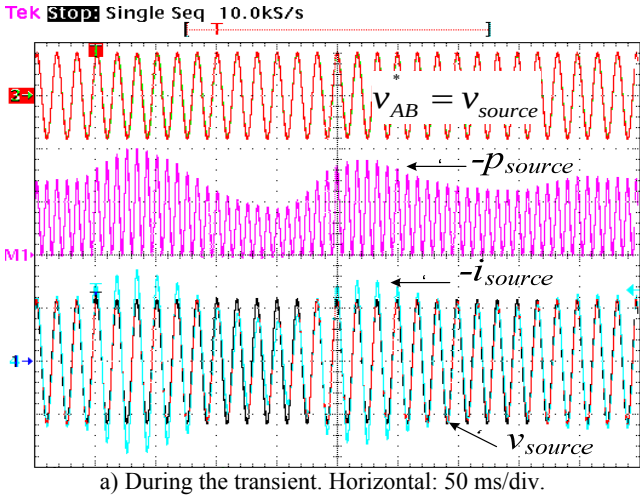
To analyze the system operation, a drastic situation was considered: a 0.5 Hz step variation was imposed to the single-phase source (programmable voltage source). A balanced three-phase 1500 W linear load was connected to the AC bus.

The results of the experiment are shown in Figure 9.a. As can be seen, the synchronism between the reference voltage generated inside of the DSP v_{AB}^{*} and v_{source} measured at the feeder are quickly restored due to the performance of the PLL controller. However, such variation produces a power fluctuation between the system (load plus inverter) and the single-phase power source. For more realistic frequency changes, such oscillation is not so problematic. Variation on the single-phase source frequency alters the β angle, and produces a power flow perturbation, which causes a variation on the DC link voltage.

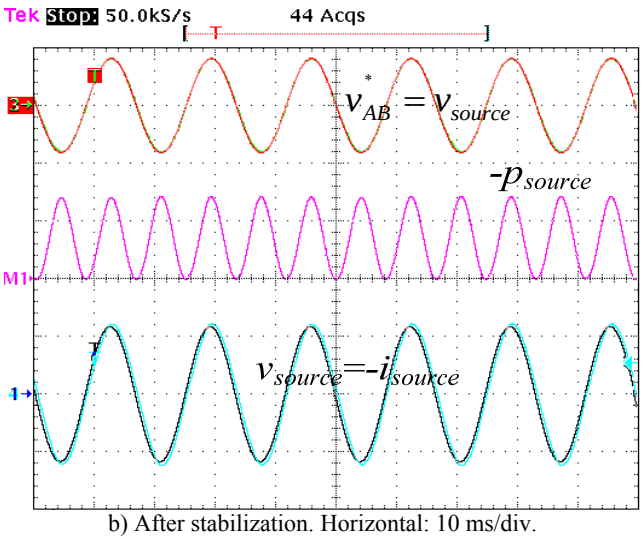
The DC link PI regulator, whose output is the desired β angle is adjusted to damping p_{source} according to (8). Figure 9.a and Figure 9.b presents the same signals before and after the stabilization.

B. Non-linear Load

A 1.7 kW non-linear load (three-phase rectifier with *R.C* load) is connected to the AC bus. Figs. 10 and 11 present the harmonic compensation capability of the control for non-linear load with and without 5th harmonic compensation. The v_{AB} THD is reduced from 6 % (without) to 3.8 % (with) for an i_L with total harmonic distortion (THD) of 60 %. The current harmonics flow through the inverter, maintaining sinusoidal source current. The spectra in Figs. 11.a and 11.b shown, mainly, the harmonic reduction when a multiple selective filter is introduced to compensate the 5th harmonic, the harmonic amplitude of v_{AB} with and without selective compensation is reduced 8 times (≈ 18 db).

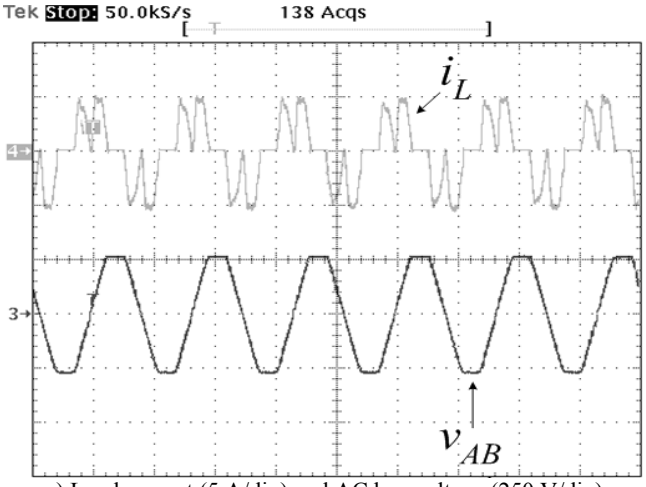


a) During the transient. Horizontal: 50 ms/div.

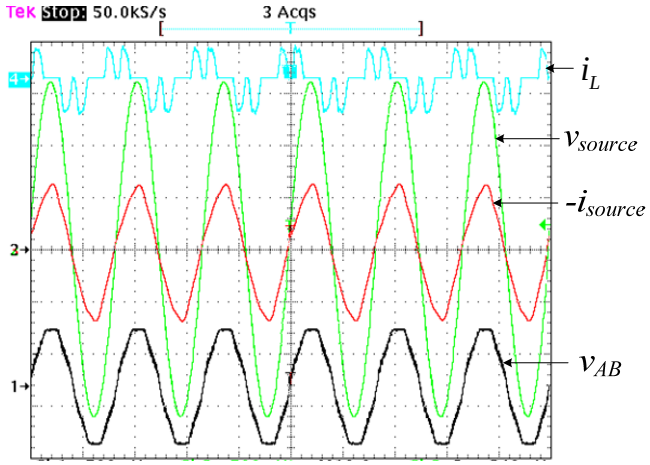


b) After stabilization. Horizontal: 10 ms/div.

Fig. 9. Top traces: internal reference and single-phase feeder voltage (360 V/div). Middle Traces: instantaneous source power (2500W/div). Bottom Traces: source voltage (250 V/div) and source current (10 A/div).

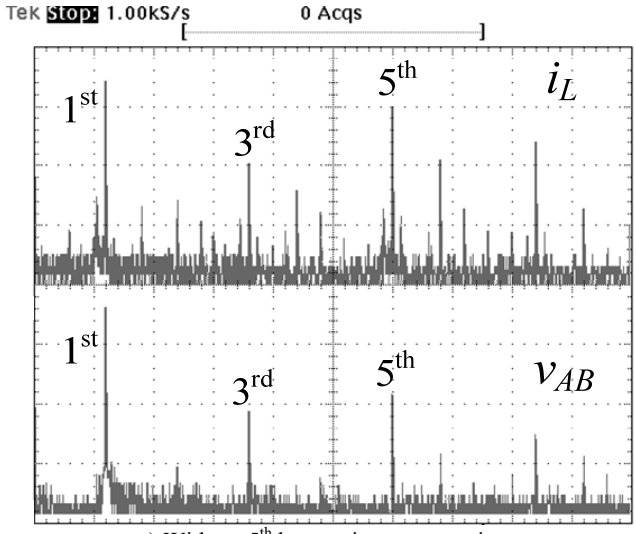


a) Load current (5 A/div) and AC bus voltage (250 V/div). Horizontal: 10 ms/div. Without 5th harmonic compensation.

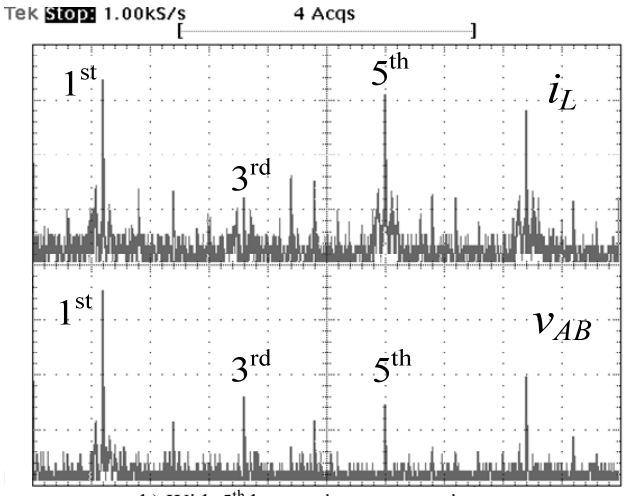


b) Load current (10 A/div), source voltage (100 V/div), source current (10 A/div) and AC bus voltage (250 V/div). Horizontal: 10 ms/div. With 5th harmonic compensation.

Fig. 10. Steady-state operation with non-linear load.



a) Without 5th harmonic compensation.



b) With 5th harmonic compensation.

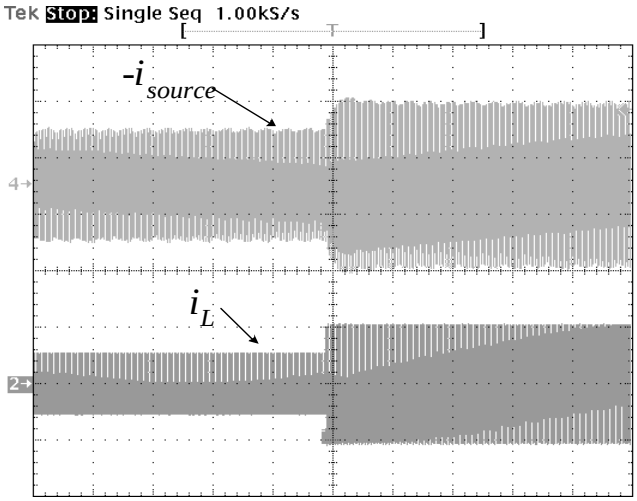
Fig. 11. Spectra of the load current (20db/div) and AC bus voltage (20 dB/div). Horizontal: 50 Hz/div.

C. Dynamic Analysis

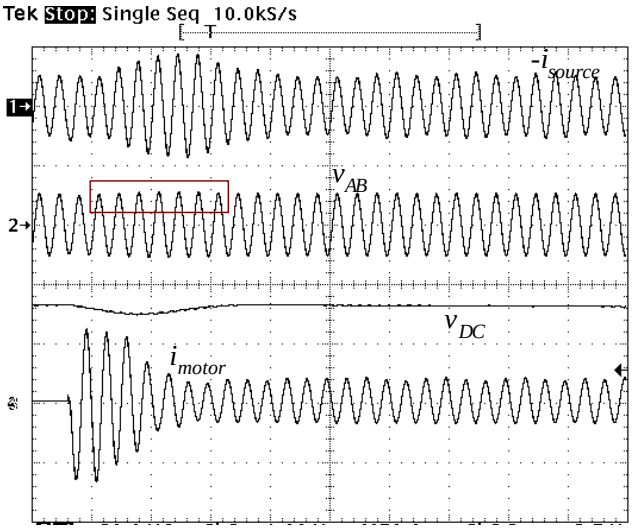
A 1.3 kW non-linear load (three-phase rectifier with resistive load) is connected to the PCC. Suddenly, an additional load is inserted; the control detects the DC link voltage variation and quickly changes the β angle absorbing from the feeder the necessary additional power, Figure 12.a. Figure 12.b shows a three-phase induction motor startup.

The additional power necessary during the acceleration is partially provided by the inverter DC bus capacitor, while the control circuit changes the β angle in order to absorb power from the feeder. The three-phase bus voltage remains almost constant due to the independent control strategy used in the AC and the DC voltage loops.

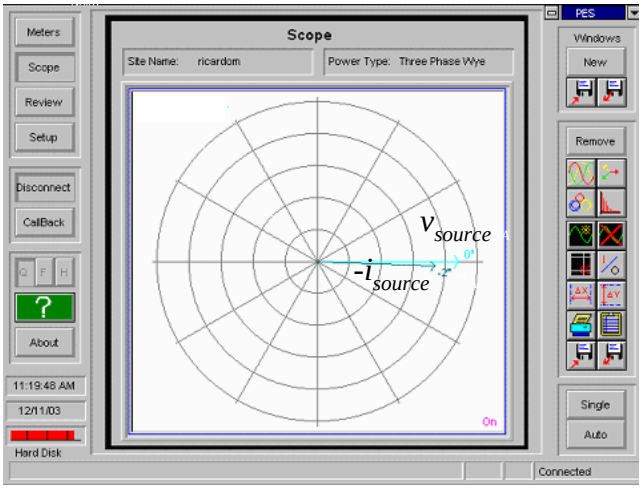
The DC voltage sag does not reflect in the AC voltage, but produces an oscillation in single-phase current. After stabilization, the displacement between v_{source} and i_{source} is 2° (Figure 12.c), due to the angle adjustment resolution. The source voltage THD is 1 %.



a) Source (10 A/div) and load current (5 A/div). Horizontal: 500 ms/div.



b) From top to bottom: single-phase current (20 A/div), AC bus voltage (500 V/div), DC link voltage (200 V/div) and motor current (5 A/div). Horizontal: 50 ms/div.



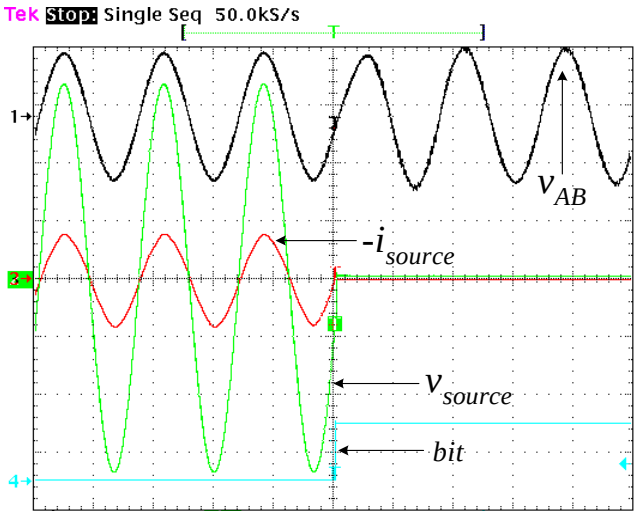
c) Phase diagram of the single-phase feeder voltage (100 V/div) and single-phase current (10 A/div).

Fig. 12. Dynamic analysis.

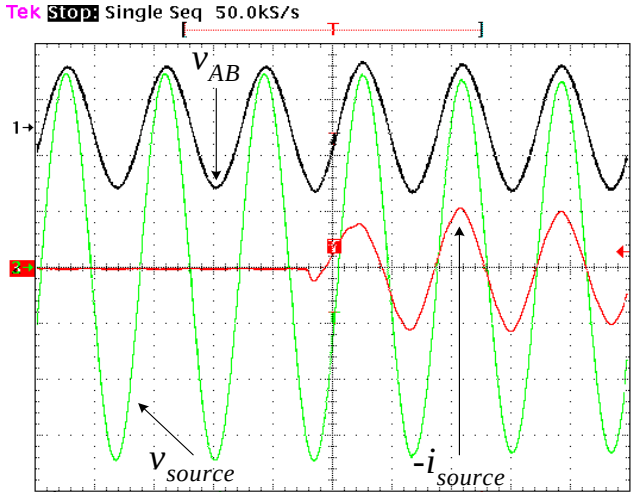
D. Grid failure (islanding operation mode)

A 1000 W three-phase resistive load was connected to the AC bus. When an island situation is detected, an interrupt routine automatically changes the inverter reference dependent of the single-phase voltage to a fixed value; in this case, 220 V. After the island detection, the energy is provided by the DC source, as shown in Figure 13.a.

The oscillation present in the waveform v_{AB} is due to the quick connection of the DC source. When the single-phase returns, another interrupt routine detects that the single-phase voltage is present and waits about 1 s to close the solid-state relay and reconnect the system (Figure 13.b).



a) From top to bottom: AC bus voltage (250V/div), single-phase current (10A/div), Single-phase feeder voltage (90V/div) and failure bit detector of the single-phase voltage. Horizontal: 10ms/div.



b) From top to bottom: AC bus voltage (250V/div), single-phase current (10A/div) and single-phase feeder voltage (90V/div). Horizontal: 10ms/div.

Fig. 13. Grid failure operation.

V. CONCLUSION

The digital control strategy of a line-interactive single-phase to three-phase conversion system was presented. It is suitable for sensitive loads because it guarantees the three-phase power quality, i.e. sinusoidal, balanced and symmetrical voltages even with non-linear loads.

A three-phase inverter is controlled in order to stabilize the three-phase voltage while absorbing current from the single-phase, under unity power factor. Any frequency variation is quickly synchronized by the PLL control.

A 3 kW experimental set-up was built to illustrate the potentialities of the proposed solutions.

APPENDIX

As L_s is designed to obtain a small β angle (from no

power to rated power) and due to the no circulation of reactive power required by the system ($Q_{source} \cong 0$), it is possible to define the behavior of the system proposed in this paper according to the diagram presented in Figure 2. In this case, (1) is obtained rearranging (8) and (17). Regarding to (2) the imposition of no reactive power is sufficient making in (18) $Q_{source} \cong 0$ and rearranging it.

$$\tan\beta = \frac{\sin\beta}{\cos\beta},\ \sin\beta = \frac{V_{L_S}}{V_{AB}} \text{ and } \cos\beta = \frac{V_{source}}{V_{AB}} \quad (17)$$

$$Q_{source} = \frac{V_{source}^2}{2.\left|X_{L_S}\right|} - \frac{V_{source}.V_{AB}}{2.\left|X_{L_S}\right|}.\cos\beta \quad (18)$$

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