A SOFT SWITCHING HALF-BRIDGE DOUBLER BOOST CONVERTER OPERATING WITH UNITY POWER FACTOR

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***Abstract* – This paper proposes a half-bridge doubler boost converter associated with an active commutation cell in order to minimize commutation losses. The converter operates with unity power factor and is able to provide high output voltages. The voltages across the semiconductor devices are low and approximately equal to the output voltage, as doubled output voltages and reduced high frequency ripple can be achieved. A detailed mathematical analysis concerning its operation is presented, since simulation and experimental results describe the converter performance.**

***Keywords* – Doubler boost converters, half-bridge converters, PFC, soft switching.**

I. INTRODUCTION

In order to meet the requirements in the proposed standards such as IEC 61000-3-2 and IEEE Std 519 on the quality of the input current that can be drawn by low-power equipment, a power factor correction (PFC) circuit is typically added to the utility interface of an AC–DC switch-mode power supply. The boost PFC circuit operating in continuous conduction mode (CCM) is by far the popular choice for medium and high power (400W to a few kilowatts) application. This is because the continuous nature of the boost converter's input current results in low electromagnetic interference (EMI) compared to other active PFC topologies such as buck-boost and buck converters.

The half-bridge boost topology shown in Fig. 1 requires an additional switch and a additional capacitor, but does not need a diode rectification bridge at the input. Only one semiconductor device conducts at any instant of time, as opposed to three in the boost rectifier, which should lead to higher efficiency. However, the voltage across each semiconductor device is equal to twice the output voltage. An additional advantage is the adjustable power factor, which can vary from -1.0 to +1.0 [1]-[3].

If four diodes are added, the improved topology in Fig. 2 results, as reduced voltages across the semiconductor devices are obtained. This converter is recommended for telecom applications [4] [5] and rectifier/inverter drive systems [6]. It is also employed as PFC front-end stage in a battery charger circuit, associated with a double forward converter [7]. Since the conduction losses in the primary side of isolated converters are inversely proportional to the input voltage, the application of this topology seems prominent.

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The requirement of high frequency operation is evident to reduce of the audible noise, the volume and the weight of magnetic elements, as well as to improve output voltage quality. However, at high frequency operation, switching losses and electromagnetic interference (EMI) become significant and must be analyzed in detail. Soft switching aim is to reduce the overlap between voltage and current during the commutation, in order to reduce switching losses, enabling high frequency operation and achieving higher power density.

Within this context, this paper presents a soft-switched half-bridge doubler boost converter, which has prominent advantages e.g. the voltage across each semiconductor is equal to V_o and the voltage ripple across capacitors C_{b1} and C_{b2} is reduced. An active commutation circuit is also described, as soft switching is obtained.

II. HALF BRIDGE DOUBLER BOOST CONVERTER WITHOUT COMMUTATION LOSSES

Many lossless switching schemes have been proposed so far in order to minimize commutation losses, and they are classified as active or passive.

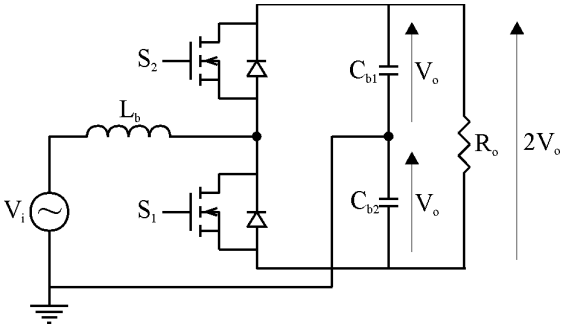


Fig. 1. Half-bridge doubler boost topology.

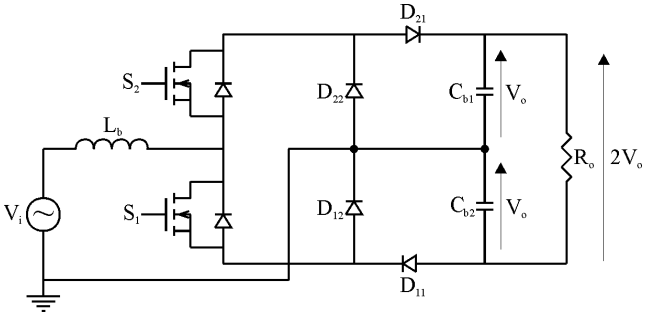


Fig. 2. Half-bridge doubler boost topology with reduced voltage stresses.

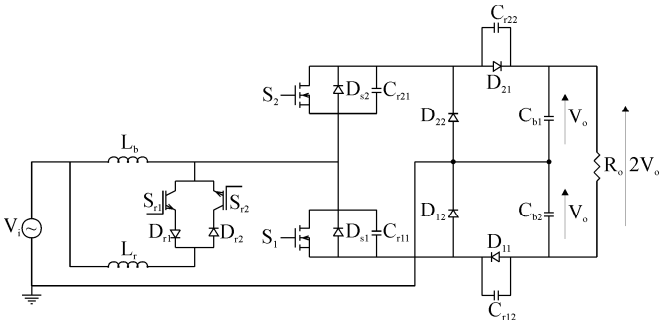


Fig. 3. Half-bridge doubler boost converter associated with the soft commutation circuit.

The work developed in [8] shows results on a boost converter employing passive and active methods, which are eventually compared. It can be seen that passive methods are better recommended for high power application, while active methods present better performance at low power levels. However, the results could not be generalized, and one is supposed to determine which method is more adequate for this topology.

A complete analysis to establish the better choice for this case is rather extensive and is not the scope of the paper. This is the main reason why the resonant circuit proposed by one of the authors in [9] and [10], which demonstrated satisfactory performance in the achievement of soft switching, was adapted to this converter.

Fig. 3 illustrates the half-bridge doubler boost converter associated with the active auxiliary commutation cell. It is composed of four resonant capacitors C_{r11}, C_{r12}, C_{r21} and C_{r22}, one resonant inductor L_r, two auxiliary switches S_{r1} and S_{r2}, and also two diodes D_{r1} and D_{r2}, so that the zero voltage transition in main switches S_1 and S_2 can be obtained. Switches S_{r1} and S_{r2} are turned on under ZCS condition. Passive snubbers are associated with the auxiliary diodes in order to minimize parasitic oscillation.

The operating stages are presented in Fig. 4. The analysis focuses only on the positive semicycle of the input voltage, where switches S_1 and S_{r1} are involved in process, but switches S_2 and S_{r2} remain turned off. The operation in the negative semicycle is analogous, although the opposite occurs. Fig. 5 shows the main theoretical waveforms necessary to the analysis of the converter operation.

A. Description of Operating Stages

• First stage [t_0-t_1] (Fig. 4 (a)) – First linear stage.

Before instant $t=t_0$, diodes D_{S2} and D_{21} conduct the boost current I_b and capacitor C_{b1} keeps charging. At $t=t_0$, switch S_{r1} is turned on under ZCS mode due to resonant inductor L_r. The voltage across L_r remains constant and equal to $2 \cdot V_o$, and the current through L_r increases linearly from null to I_m, where I_m is the constant current through the boost inductor. The current through D_{S2} and D_{21} decreases linearly as well. This stage finishes when i_{Lr} equals I_m, what can be described mathematically according to expression (1).

$$i_{Lr}(t) = \left(V_o - V_i\right) \cdot \frac{1}{L_r} \cdot t \tag{1}$$

The time interval that defines this stage is:

$$\Delta t_1 = \frac{I_m}{\left(V_o - V_i\right)} \cdot L_r \tag{2}$$

• Second stage [t_1-t_2] (Fig. 4 (b)) – First resonant stage.

The resonance involving all the resonant capacitors begins when the current through inductor L_r becomes greater than I_m. The resonant current $i_{Lr}(t)$ is divided equally between two resonant networks, which are formed by two capacitor sets i.e. C_{r11}-C_{r12} and C_{r21}-C_{r22}. In order to assure the analogous operation of the converter in the negative semicycle, the following assumptions are made:

$$C_{r11} = C_{r21} \tag{3}$$

$$C_{r12} = C_{r22} \tag{4}$$

$$K = \frac{C_{r11}}{C_{r12}} = \frac{C_{r21}}{C_{r22}} \tag{5}$$

The behavior of the voltages across the resonant capacitors is:

- $v_{Cr11}(t)$ decreases from $2 \cdot V_o$ to null;
- $v_{Cr21}(t)$ increases from null to V_o;
- $v_{Cr12}(t)$ decreases from $2 \cdot V_o$ to $v_{Cr12}(t_2)$;
- $v_{Cr22}(t)$ increases from null to $v_{Cr22}(t_2)$.

The resonant frequency and the characteristic impedance are given by (6) and (7), respectively.

$$f_o = \frac{1}{2\pi} \cdot \sqrt{\frac{1}{2 \cdot L_r \cdot C_r}} \tag{6}$$

$$Z_o = \sqrt{\frac{L_r}{2 \cdot C_r}} \tag{7}$$

where:

$$C_r = C_{r11} + C_{r12} = C_{r21} + C_{r22} \tag{8}$$

This stage finishes when the voltage across C_{r11} is null, and it can be defined according to expressions (9) to (13).

$$i_{Lr}(t) = \frac{2 \cdot \left(V_o - V_i\right)}{Z_o} \sin\left(2\pi \cdot f_0 \cdot t\right) + I_m \tag{9}$$

$$v_{Cr11}(t) = V_o - \left(V_o - V_i\right) \cdot \frac{K}{1+K} \cdot \left[1 - \cos\left(2\pi \cdot f_0 \cdot t\right)\right] \tag{10}$$

$$v_{Cr12}(t) = V_o - \left(V_o - V_i\right) \cdot \frac{1}{1+K} \cdot \left[1 - \cos\left(2\pi \cdot f_0 \cdot t\right)\right] \tag{11}$$

$$v_{Cr21}(t) = \left(V_o - V_i\right) \cdot \frac{K}{1+K} \cdot \left[1 - \cos\left(2\pi \cdot f_0 \cdot t\right)\right] \tag{12}$$

$$v_{Cr22}(t) = \left(V_o - V_i\right) \cdot \frac{1}{1+K} \cdot \left[1 - \cos\left(2\pi \cdot f_0 \cdot t\right)\right] \tag{13}$$

According to the complete mathematical study of the converter developed in [7], the time interval that defines the second stage is:

$$\Delta t_2 = \frac{1}{2\pi \cdot f_0} \cdot \arccos\left(1 - V_o \cdot \frac{K+1}{K\left(V_o - V_i\right)}\right) \tag{14}$$

From (14), it can be seen that the maximum value for Δt_2 is π rad. It means that the voltage across resonant capacitor C_{r11} must decrease to null within this interval to assure soft switching. Therefore the following condition, stated in [7], must be observed:

$$V_o = 2 \cdot V_i + V_x \tag{15}$$

where V_x is about 10% to 20% of the input voltage.

Additionally, parameter K must be greater enough so that the second stage finishes before π rad [7].

$$K > \frac{2 \cdot V_i + V_x}{V_x} \tag{16}$$

• **Third stage [t_2-t_3] (Fig. 4 (c)) – Second resonant stage.**

When the voltage across capacitor C_{r11} is null and remains clamped, switch S_1 can be turned on under ZVS condition. Diode D_{S1} starts conducting and the current through capacitor C_{r12} increases almost instantly. Since the current through C_{r12} increases, both currents through C_{r21} and C_{r22} must decrease almost instantly. Once resonant inductor L_r conducts the entire boost current I_b, switch S_1 is turned on in ZCS mode as well. The behavior of the voltages across the resonant capacitors is:

- $v_{Cr21}(t)$: increases from V_o to $v_{Cr21}(t_3)$;
- $v_{Cr12}(t)$: decreases from $v_{Cr12}(t_2)$ to $v_{Cr12}(t_3)$;
- $v_{Cr22}(t)$: increases from $v_{Cr22}(t_2)$ to $v_{Cr22}(t_3)$.

In this stage, there are low voltage stresses across switch S_2, and it finishes when $i_{Cr12}(t)=i_{Cr21}(t)=i_{Cr22}(t)=0$ and $i_{Lr}(t)=I_b$.

A new resonant frequency and a new characteristic impedance are defined in this stage, according to (17) and (18), respectively.

$$Z_1 = \sqrt{\frac{L_r}{(2+K)\cdot C_r}} \tag{17}$$

$$f_1 = \frac{1}{2\pi} \cdot \sqrt{\frac{1}{(2+K)\cdot C_r \cdot L_r}} \tag{18}$$

The expressions that describe this stage mathematically are as follows:

$$i_{Lr}(t) = \left[\frac{(V_o - V_i)}{Z_o} \cdot \sqrt{1 - \left(\frac{V_o \cdot (K+1)}{K(V_o - V_i)} - 1 \right)^2} \right] \cdot \cos(2 \cdot \pi \cdot f_1 \cdot t) + I_m - \frac{1}{Z_1} \cdot \left(\frac{V_o}{K} + V_i \right) \cdot \sin(2 \cdot \pi \cdot f_1 \cdot t) \tag{19}$$

$$v_{Cr12}(t) = \left(V_o - \frac{V_o}{K} \right) - \left[\begin{array}{l} \frac{\sqrt{4+2\cdot K}}{2+K} \cdot \\ \left(\frac{(V_o - V_i)}{2} \cdot \sqrt{1 - \left(\frac{V_o \cdot (K+1)}{K \cdot (V_o - V_i)} - 1 \right)^2} \right) \\ \cdot \sin(2 \cdot \pi \cdot f_1 \cdot t) \\ + \left(\frac{V_o}{K} + V_{in} \right) \cdot (1 - \cos(2 \cdot \pi \cdot f_1 \cdot t)) \end{array} \right] \tag{20}$$

$$v_{Cr21}(t) = V_o + \left[\begin{array}{l} \frac{K\sqrt{4+2\cdot K}}{(2+K)\cdot(1+K)} \cdot \\ \left(\frac{(V_o - V_i)}{2} \cdot \sqrt{1 - \left(\frac{V_o \cdot (K+1)}{K(V_o - V_{in})} - 1 \right)^2} \right) \cdot \sin(2 \cdot \pi \cdot f_1 \cdot t) \\ + \frac{K}{K+1} \cdot \left(\frac{V_o}{K} + V_i \right) \cdot (\cos(2 \cdot \pi \cdot f_1 \cdot t) - 1) \end{array} \right] \tag{21}$$

$$v_{Cr22}(t) = V_o + \left[\begin{array}{l} \frac{K\sqrt{4+2\cdot K}}{(2+K)\cdot(1+K)} \cdot \\ \left(\frac{(V_o - V_i)}{2} \cdot \sqrt{1 - \left(\frac{V_o \cdot (K+1)}{K(V_o - V_{in})} - 1 \right)^2} \right) \cdot \sin(2 \cdot \pi \cdot f_1 \cdot t) \\ + \frac{K}{K+1} \cdot \left(\frac{V_o}{K} + V_i \right) \cdot (\cos(2 \cdot \pi \cdot f_1 \cdot t) - 1) \end{array} \right] \tag{22}$$

The time interval that defines this stage is:

$$\Delta t_3 = \arctan \left(\frac{\frac{K\sqrt{4+2\cdot K}}{(2+K)\cdot(1+K)} \cdot \left(\frac{(V_o - V_i)}{2} \cdot \sqrt{1 - \left(\frac{V_o \cdot (K+1)}{K(V_o - V_i)} - 1 \right)^2} \right)}{\frac{K}{K+1} \cdot \left(\frac{V_o}{K} + V_i \right)} \right) \tag{23}$$

• **Fourth stage [t_3-t_4] (Fig. 4 (d)) – Third resonant stage.**

Diode D_{S1} is reverse biased and switch S_1 conducts the current through capacitor C_{r12}. The relevant resonant circuit is the same one presented in the third stage. This stage finishes when i_{Lr} is null so that switch S_{r1} can be turned off, and the time interval that defines it is:

$$\Delta t_4 = \arctan \left(\frac{\left(I_m + \frac{(V_o - V_i)}{2 \cdot Z_o} \right) \cdot \sqrt{1 - \left(\frac{V_o \cdot (K+1)}{K(V_o - V_i)} - 1 \right)^2}}{\frac{K}{K+1} \cdot \left(\frac{V_o}{K} + V_i \right) \cdot \frac{1}{Z_1}} \right) \tag{24}$$

• **Fifth stage [t_4-t_5] (Fig. 4 (e)) – Second linear stage.**

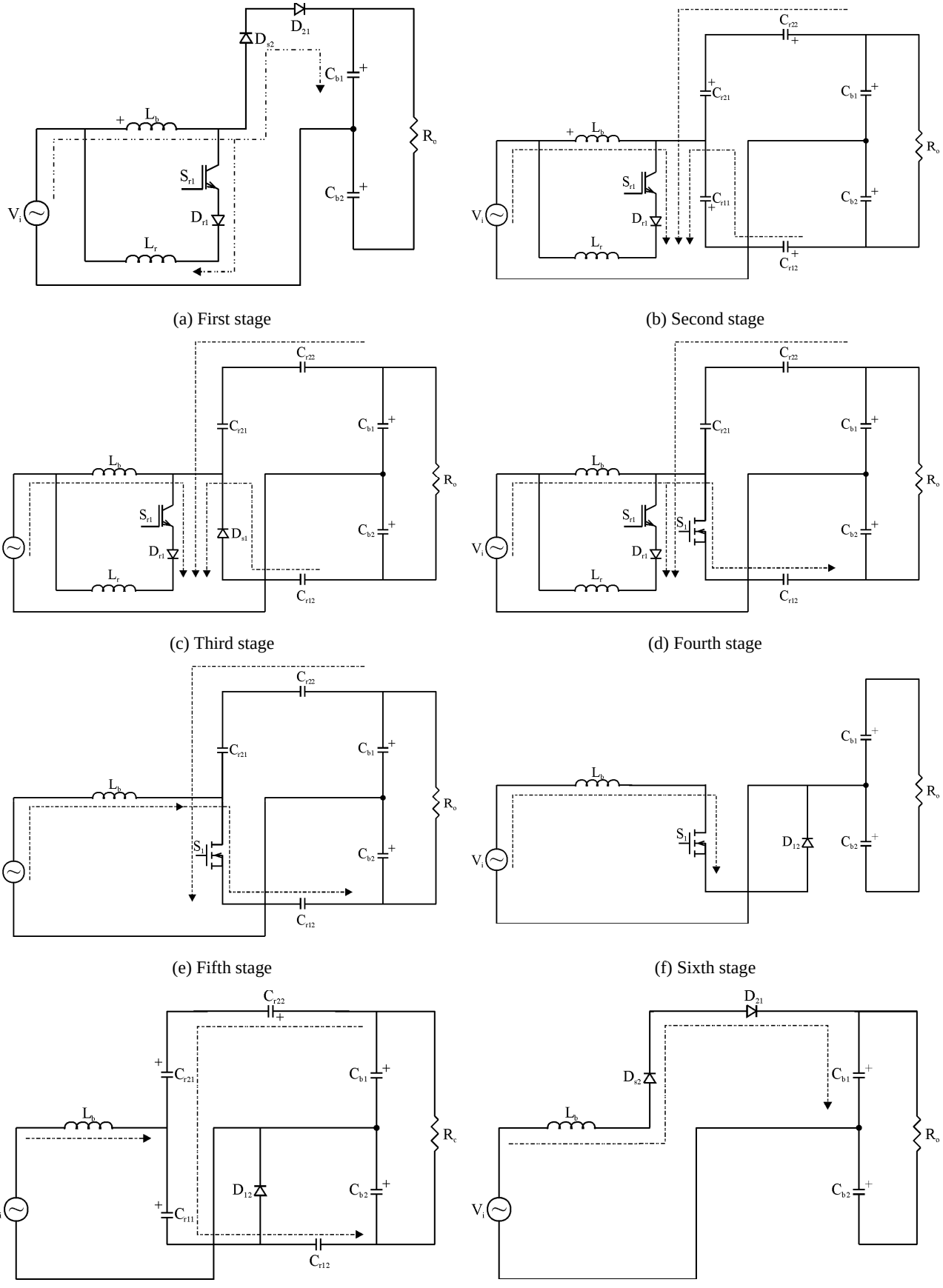
Since the current through the resonant inductor is null when this stage begins, switch S_{r1} is turned off in ZCS mode at instant t_4. As diodes D_{21}, D_{22} and D_{12} are reverse biased, the boost current I_b flows through capacitors C_{r12}, C_{r21} and C_{r22}. The behavior of the voltages across the resonant capacitors is:

- $v_{Cr21}(t)$ decreases linearly from V_o to $v_{Cr21}(t_5)$;
- $v_{Cr12}(t)$ increases linearly from $v_{Cr12}(t_4)$ to V_o;
- $v_{Cr22}(t)$ decreases linearly from $v_{Cr22}(t_4)$ to $v_{Cr22}(t_5)$.

This stage finishes when diode D_{12} starts conducting and the currents through capacitors C_{r12}, C_{r21} and C_{r22} become null instantly. It can be mathematically described according to expressions (25) to (27).

$$v_{Cr12}(t) = v_{Cr12}(t_4) + \left(\frac{1+K}{2+K} \right) \cdot \frac{I_m}{C_{r12}} \cdot t \tag{25}$$

$$v_{Cr21}(t) = v_{Cr21}(t_4) - \left(\frac{1}{2+K} \right) \cdot \frac{I_m}{C_{r21}} \cdot t \tag{26}$$



(a) First stage

(b) Second stage

(c) Third stage

(d) Fourth stage

(e) Fifth stage

(f) Sixth stage

(g) Seventh stage

(h) Eighth stage

Fig. 4. Equivalent circuits concerning the operating stages of the proposed converter.

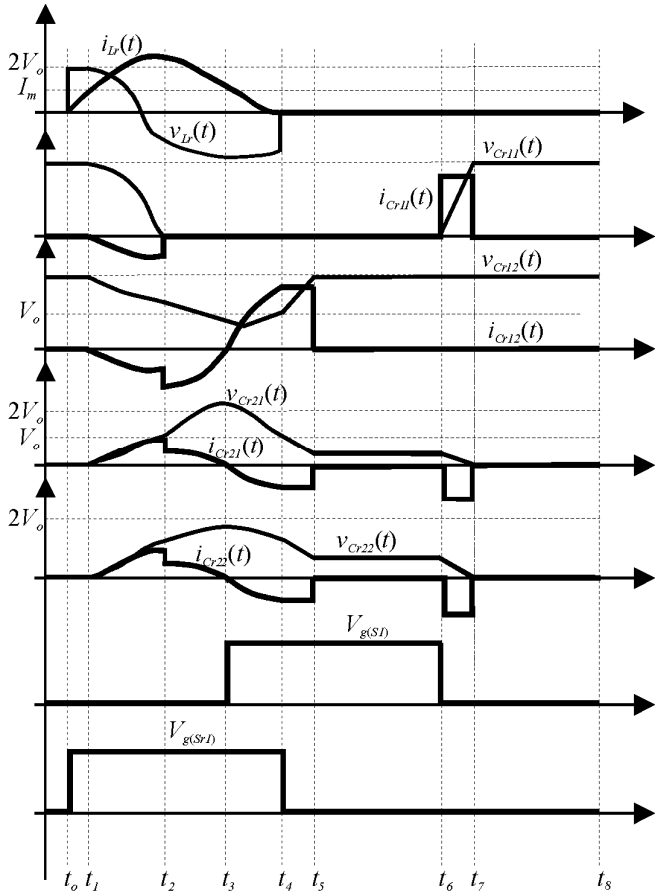


Fig. 5. Main theoretical waveforms.

$$v_{Cr22}(t) = v_{Cr22}(t_4) - \left(\frac{1}{2+K}\right)\cdot\frac{I_m}{C_{r22}}\cdot t \qquad (27)$$

The time interval that defines this stage is:

$$\Delta t_5 = \left(V_o - v_{Cr12}(t_4)\right)\cdot\left(\frac{2+K}{1+K}\right)\cdot\frac{C_{r12}}{I_m} \qquad (28)$$

• **Sixth stage [t_5-t_6] (Fig. 4 (f)) – First constant stage.**

In this stage, the whole variables set remains constant, as the control circuit defines time interval Δt_6. This stage finishes when switch S_1 is turned off.

• **Seventh stage [t_6-t_7] (Fig. 4 (g)) – Third linear stage.**

When switch S_1 is turned off in ZVS mode, capacitor C_{r11} is charged linearly by current I_b, as capacitors C_{r21} and C_{r22} discharge completely. This stage finishes when $v_{Cr11}(t_7)=2\cdot V_o$ and $v_{Cr21}(t_7)=v_{Cr22}(t_7)=0$, what can be mathematically described according to expressions (29) to (31).

$$v_{Cr11}(t) = \left(\frac{K+1}{2\cdot K+1}\right)\cdot\frac{I_m}{C_{r11}}\cdot t \qquad (29)$$

$$v_{Cr21}(t) = \left[v_{Cr21}(t_4) - \frac{K}{1+K}\cdot\left(V_o - v_{Cr12}(t_4)\right)\right] - \left(\frac{K}{2\cdot K+1}\right)\cdot\frac{I_m}{C_{r21}}\cdot t \qquad (30)$$

$$v_{Cr22}(t) = \left[v_{Cr22}(t_4) - \frac{1}{1+K}\cdot\left(V_o - v_{Cr12}(t_4)\right)\right] - \left(\frac{K}{2\cdot K+1}\right)\cdot\frac{I_L}{C_{r22}}\cdot t \qquad (31)$$

This stage is defined by:

$$\Delta t_7 = \left(\frac{2\cdot K+1}{K+1}\right)\cdot\frac{C_{r11}}{I_m}\cdot V_o \qquad (32)$$

• **Eighth stage [t_7-t_8] (Fig. 4 (h)) – Second constant stage.**

The controller defines time interval Δt_8, and this stage finishes when switch S_{r1} is turned on, and the next switching cycle begins.

If the current through the boost inductor is low, the voltage across C_{r11} does not reach V_o during the seventh stage, and the voltages across C_{r21} and C_{r22} do not become null. Hence diodes D_{21} and D_{s2} remain blocked during the eighth stage, which is not considered in the analysis of the converter operation. When the control circuit enables switch S_{r1} to be turned on, the first stage begins. During the second stage, capacitors C_{r11} and C_{r12} are fully discharged, while capacitors C_{r21} and C_{r22} are charged until the voltage across C_{r21} equals V_o. Since the remaining resonant stages occur independently on the current through the boost inductor, resonance is not influenced and, consequently, turning on and turning off of the switches are not affected when such current is low.

B. Influence of The Soft Switching Cell in The Duty Cycle

Considering the positive semicycle of the current through the boost inductor, an expression for the maximum duty cycle can be obtained according to the analysis presented below.

During the first and second stages, switch S_1 is turned off due to the resonance, and capacitor C_{r11} remains charged. In the third stage, v_{Cr11} becomes null, and switch S_1 is enabled to be turned on when C_{r11} is fully discharged. Since the current through C_{r12} is negative, it flows through diode D_{s1} and resonant inductor L_r.

In the fourth stage, the current through C_{r12} becomes positive, and S_1 is turned on. The boost current is constant and flows through the path defined by S_1-C_{r12}-C_{b2}-C_{b1}-C_{r22}-C_{r21}.

Since the voltage across C_{r12} is not equal to the output voltage in the fifth stage, D_{12} is reverse biased. Part of the boost inductor current charges C_{r11} and discharges C_{r21} and C_{r22}., and switch S_1 is on. In the sixth stage, S_1 remains turned on, and the current flows through diode D_{12}.

During the seventh stage, switch S_1 is turned off under ZVS condition, and it remains off as well in the next stage.

In front of the aforementioned assumptions, the following expression becomes valid.

$$D_{\max} = \frac{\Delta t_5 + \Delta t_6}{T_s} = \frac{\Delta t_5 + \Delta t_6}{\sum_{i=1}^{8}\Delta t_i} \qquad (33)$$

C. Some Aspects Regarding The Input Current

The resonant circuit employed in the converter imposes an undesirable effect to the input current, which is in discontinuous mode. In order to solve this problem, a small LC filter is applied to the input of the converter, where a cut-off frequency f_c equal to about 5% to 10% of the switching frequency is set. Therefore, expression (34) is valid, where C_f must not be big enough to cause a displacement between the input current and the input voltage.

$$L_f = \frac{1}{\left(2 \cdot \pi \cdot f_c\right)^2 \cdot C_f} \tag{34}$$

III. CONTROL SYSTEM

The strategy employed in the proposed topology is the average current mode control, which can be implemented with a PFC integrated circuit [11]. The closed-loop diagram is presented in Fig. 6.

The half-bridge doubler boost converter operates with isolated gate drivers, adding complexity to the control system, since different circuits are used for the main and auxiliary switches. Auxiliary switches use optocouplers and dedicated gate driver IC [7]. Main switches are driven with dual thyristor schemes [7] [12]. A diagram representing the gating signals applied to the switches is shown in Fig. 7.

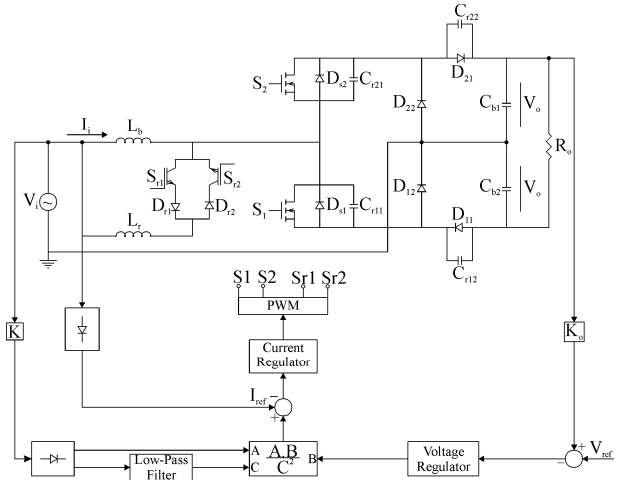


Fig. 6. Half-bridge doubler boost converter operating with average current mode control.

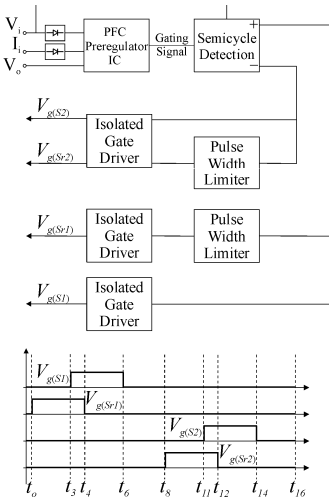


Fig. 7. Gating signals applied to main and auxiliary switches.

IV. DESIGN PROCEDURE

From the study developed in [7], the following expressions for the calculation of the circuit parameters could be obtained.

The boost inductance is given by:

$$L_b = 2 \cdot \frac{25000 \cdot P_o}{f_s \cdot \eta} \tag{35}$$

where P_o is the output power, f_s is the switching frequency and η is the efficiency of the converter.

The output capacitors are calculated according to (36).

$$C_{b1} = C_{b2} = 2 \cdot \frac{P_o}{2 \cdot \pi \cdot \left(2 \cdot N \cdot f\right) \cdot V_o \cdot \Delta V_o} \tag{36}$$

where N is the number of phases, f is the line frequency and ΔV_o is the maximum output voltage ripple.

The first step to calculate the resonant elements lies is the choice of the resonant frequency, which must be at least ten times the switching frequency to assure the accurate operation of the circuit. If the resonant inductor is chosen arbitrarily (typically a few microhenries), expression (6) can be used to determine parameter C_r, defined in (8). Additionally, if parameter K is calculated according to (16), the resonant capacitors are then obtained from (37) and (38).

$$C_{r11} = C_{r21} = \frac{K+1}{K} \cdot C_r \tag{37}$$

$$C_{r12} = C_{r22} = (1+K) \cdot C_r \tag{38}$$

V. ANALYTICAL RESULTS

In order to validate the study developed above, evaluation tests of the proposed converter were performed using the parameters set presented in Table I.

Fig. 8 shows the voltages across the resonant capacitors and the current through the resonant inductor. It can be seen that the maximum voltage peaks across the resonant capacitors do not exceed half of the output voltage in any circumstances. The aforementioned results were obtained using software OrCAD release 9.2, and demonstrate the validity of the theoretical analysis.

Furthermore, an experimental prototype of the converter was implemented. Fig. 9 shows the switching detail in auxiliary switch S_{r1}, where it can be seen that it is turned on with null current and turned off with null current and null voltage.

Fig. 10 corresponds to the switching detail in main switch S1, where the soft switching is achieved with reduced *dv*/*dt* rates, without current and/or voltage stresses.

Fig. 11 shows the input current in discontinuous mode, without the low-pass filter.

Fig. 12 evidences power factor correction, where it can be seen that the total harmonic distortion is low and a high power factor is achieved i.e. current THD is 5.5% and power factor is 0.990. Fig. 13 represents the harmonic content of the input current.

Table I
Parameters set employed in the tests

Parameter	Description
Line frequency	f=60Hz
Switching frequency	f_s=50kHz
Rms input voltage	V_i=110V
Output voltage	V_o=300V
Maximum output voltage ripple	ΔV_o=5%·V_o
Output power	P_o=800W
Efficiency	η=97%
Boost inductor	L_b=380μH
Resonant inductor	L_r=4.9μH
Resonant capacitors	C_{r11}=C_{r21}=3.3nF
Resonant capacitors	C_{r12}=C_{r22}=18.8nF
Output capacitors	C_{b1}=C_{b2}=1000μF
Input filter inductor	L_f=80μH
Input filter capacitor	C_f=10μF
Diodes	MUR1560
Main switches S_1 and S_2	MOSFET – IRFP460
Auxiliary switches S_{r1} and S_{r2}	IGBT – IRG4BC30U

Finally, Fig. 14 presents the converter efficiency as a function of the output power. Hard-switching and soft-switching topologies shown in Fig. 2 and Fig. 3 are compared, as both them operate at 100kHz with the parameters set detailed in Table I. It can be seen that the use of the soft commutation cell becomes interesting at a few hundreds of watts, and efficiency is about 97% at nominal load.

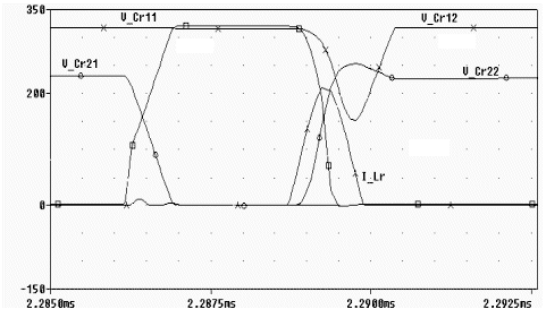


Fig. 8. Resonant tank waveforms.

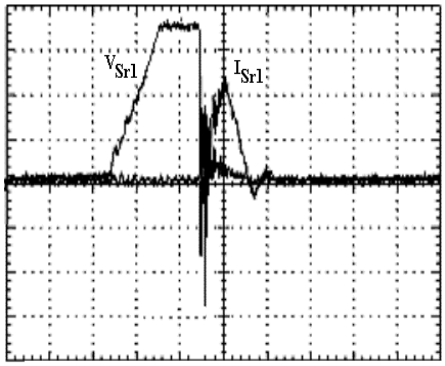


Fig. 9. Switching detail in S_{r1}.
Scales: V_{Sr1} – 100V/div.; I_{Sr1} – 5A/div.; time – 1μs/div.

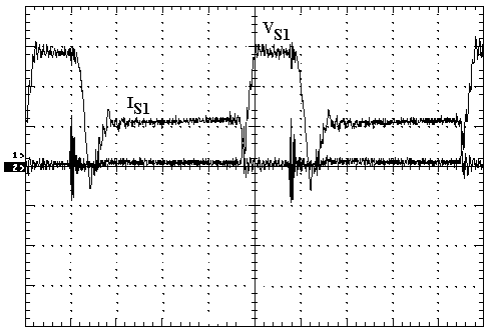


Fig. 10. Switching detail in S_1.
Scales: V_{S1} – 100V/div.; I_{S1} – 5A/div.; time – 2μs/div.

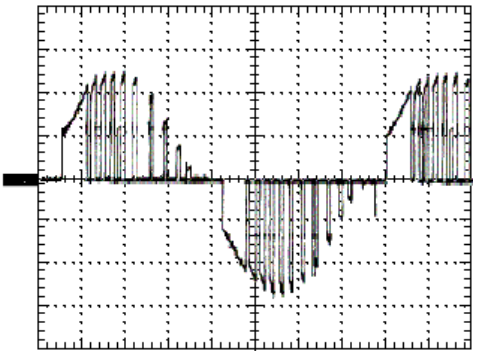


Fig. 11. Input current in discontinuous mode.
Scales: I_i – 10A/div.; time – 2ms/div.

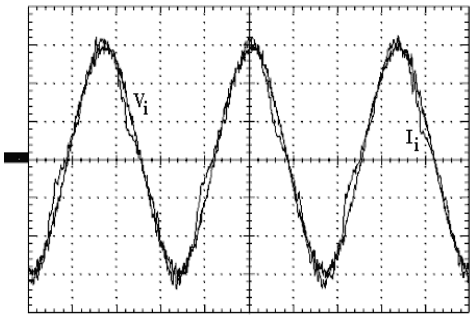


Fig. 12. Input voltage and input current.
Scales: V_i – 50V/div.; I_i – 10A/div.; time – 5ms/div.

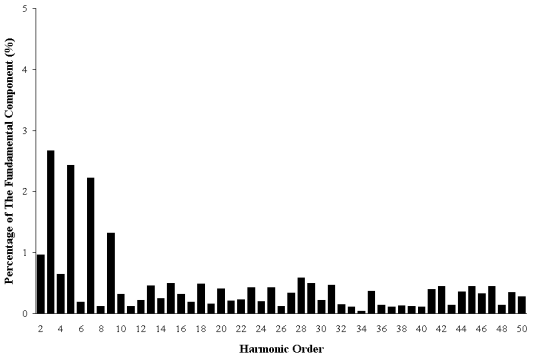


Fig. 13. Harmonic spectrum of the input current.

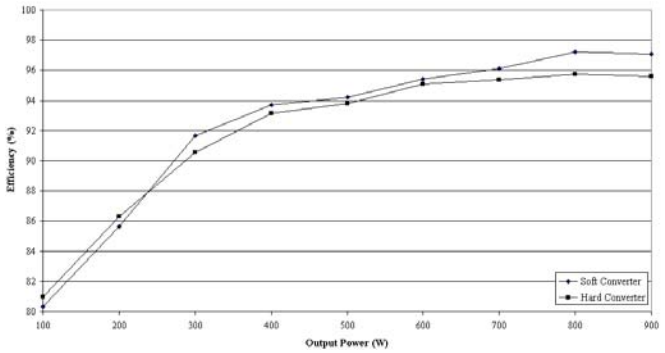


Fig. 14. Efficiency versus output power.

VI. ABOUT THE PROPOSED TOPOLOGY

The half-bridge structure shown in Fig. 1 is a prominent alternative if compared with the conventional boost converter, since conduction losses are drastically reduced. However, the voltage stresses across the switches are twice the output voltage. An improvement results if the topology depicted in Fig. 2 is adopted, because the voltages across the switches are equal to the output voltage instead.

If an active auxiliary circuit is added, complexity is supposed to increase and reliability is affected, because four capacitors, one inductor, two auxiliary switches, and two diodes are employed in this case. Furthermore, conduction losses increase as well, but they are mainly due to the components existent in the hard-switched topology presented in Fig. 2.

Soft switching is a desired feature in power converters because it reduces the overlap between voltage and current, enabling high frequency operation, minimizing switching losses and giving a longer life for the switch. The choice between passive and active soft switching methods depends on a series of conditions [8]. This is not the scope of the paper, which aims to analyze the performance of the soft switching cell associated with the half-bridge doubler boost converter. Possibly, improved soft switching schemes can be proposed for this topology, as the one described here is not a definitive solution.

Possible advantages of the proposed configuration are:
- The voltages across the semiconductor devices are reduced and approximately equal to the output voltage;
- Doubled output voltages can be achieved;
- Reduced high frequency ripple of the output voltage is obtained due to diodes D_{12} and D_{22};
- Switching losses are negligible;
- In Fig. 14, one can see that the efficiency increases about 2% at nominal power.

VII. CONCLUSION

This paper has reported the study of a soft-switched half-bridge doubler boost converter that can be used in PFC applications. The main purpose of this work deals with the development of a structure without commutation losses so that higher output voltages and reduced voltage stresses across the semiconductor devices can be achieved, as high power factor and low harmonic content are obtained. The results show that the main advantages of the proposed topology are the reduced voltages across the semiconductor devices, achievement of doubled output voltages, reduced high frequency ripple and also lossless commutation of the switches. As drawbacks, one can mention the complexity added to control system and drivers due to the cell, and also increased number of components.

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