FULL-BRIDGE ZVS-PWM HYBRID SWITCHED-CAPACITOR ISOLATED DC-DC CONVERTER

Anderson Alves[1], Ivo Barbi[1]
[1]Federal University of Santa Catarina (UFSC), Florianópolis - Santa Catarina, Brazil
e-mail: anderson.alves031@gmail.com, ivobarbi@gmail.com

Abstract – **This paper presents a new hybrid switched-capacitor (HSC) isolated DC-DC converter topology generated from the integration of the ladder switching cell with the full-bridge ZVS-PWM converter. This new topology reduces the voltage stress on the switches and other components on the primary side of the transformer to half of the bus voltage, spontaneously equalizes the voltage in the divider capacitors and presents zero-voltage-switching (ZVS) in all switches for a wide load range. The principle of operation, static gain, current stress in the power semiconductors, and commutation analysis are presented in this paper. A theoretical and experimental comparative analysis of the new topology with the TL-NPC converter is also performed. Experimental results with a laboratory prototype with 2 kW rated power, 800 V input voltage, 60 V output voltage and 100 kHz switching frequency show a maximum efficiency of 97.12% for the HSC converter against 96.49% for the TL-NPC converter.**

Keywords – **Full-bridge ZVS-PWM converter, Hybrid converter, Isolated DC-DC converter, Ladder cell, Switched-capacitor converter, Zero-voltage-switching.**

I. INTRODUCTION

The growing interest in DC distribution and transmission systems, DC microgrids, photovoltaic energy systems, storage systems, electric vehicles and auxiliary power supplies for medium and high voltage is driving the development of high efficiency DC-DC converters for medium and high voltage systems. Converters with series connected power switches [1], [2], series connected modular converters [3], [4] and multilevel converters [5]–[8] are often used for this purpose. A notable example is the three-level neutral-point-clamped (TL-NPC) DC-DC converter [5], operating at half the bus voltage on the power semiconductors and zero-voltage-switching (ZVS). However, the equalization of the voltage on the power switches and input capacitors does not occur spontaneously, being sensitive to the parametric variations of the components and to asymmetries in the command gate signals of the switches, and requiring additional control circuits to ensure voltage equalization.

Another technique traditionally employed in signal processing circuits and introduced in energy processing systems is the use of switched-capacitor (SC) cells to process power. These SC cells promote a reduction in the voltage level on the power switches spontaneously, eliminating the need for a control circuit for this purpose. This lowering of the voltage level across the switches makes it possible to operate high voltage converters using low voltage power semiconductors. Low voltage MOSFETs have lower conduction resistance (R_{DSon} proportional to $V_{DS}{}^{2.5}$)[9] and parasitic capacitances (C_{oss}) of lower value, so their use reduces the conduction and fixed losses, consequently increasing the efficiency of the converter. Despite these advantages, this type of converter has limitations in terms of voltage control as a function of the duty cycle variation, making it necessary to use a hybrid switched-capacitor (HSC) topology formed by integrating the SC cells with the conventional converters that have inductors.

The ladder cell [10] is an SC topology that is easy to integrate with other converters. It allows the creation of hybrid topologies with lower voltage stress on the components and spontaneous equalization of the voltage division and is used in non-isolated DC-DC converters [11]–[14] and in isolated DC-DC converters [15], [16].

This paper presents a new HSC full-bridge isolated DC-DC converter topology generated from the integration of the ladder switching cell with the FB-ZVS-PWM converter [17]. This new topology preserves the characteristics of the original FB-ZVS-PWM converter and adds the advantage of spontaneous equalization of the voltage stress in the primary side power components to half the value of the bus voltage. This offers an alternative for applications that operate with high input voltage.

II. PROPOSED CONVERTER

The proposed converter integrates the ladder switching cell with the FB-ZVS-PWM converter, the power stage for which is shown in Figure 1.a. In this figure, the capacitors C_1 and C_2 represent the input capacitive divider, C_S is the switched capacitor that ensures voltage equalization in C_1 and C_2, S_1 to S_6 are the power switches, C_{C1} to C_{C6} represent the capacitances used in commutation, L_r is the resonant inductor used for commutation, Tr is the high frequency isolating transformer, D_{o1} and D_{o2} represent the output rectifier diodes, L_o and C_o comprise the output filter and R_o represents the load resistance. The diodes D_{g1} and D_{g2} form the input clamp circuit [18].

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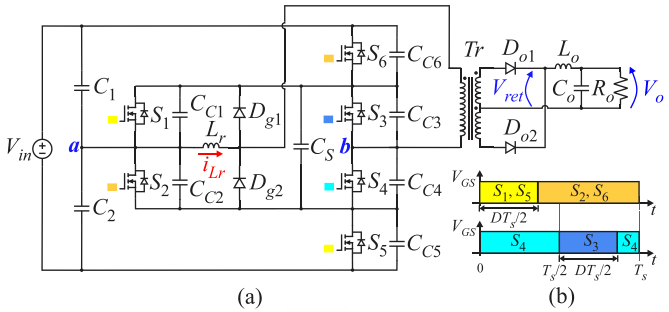

Fig. 1. (a) Schematic of the proposed converter power stage and (b) power semiconductor command signals.

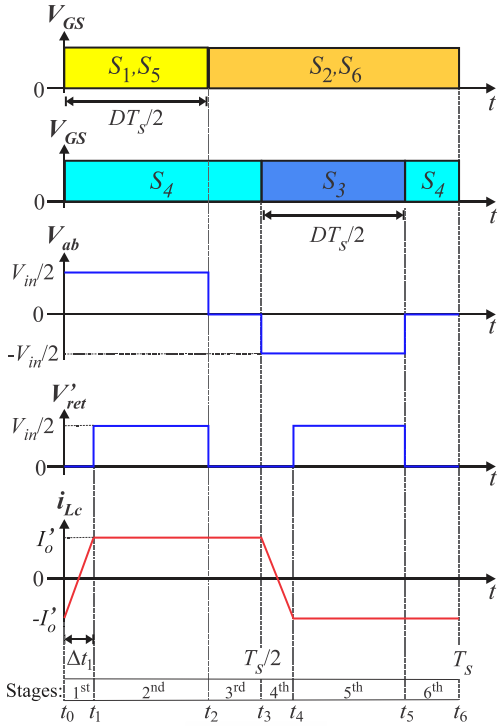

Fig. 2. Main waveforms of the proposed converter.

The voltage on the components of the primary circuit is equalized spontaneously and is equal to half of the bus voltage, dispensing with the need for a control circuit. This provides the new converter with a significant advantage when compared to solutions that use the series connection of power switches, series connected modular converters and multilevel converters.

Figure 1(b) shows the switch command signals. The proposed converter operates with symmetrical PWM command signals. The duty cycle D of the converter is defined as the ratio between the activation time of the gate signal of switches S_1 and S_3 and the switching period. The switches S_1, S_5 and S_2, S_6, which form the ladder cell, are commanded by complementary signals.

III. PRINCIPLE OF OPERATION

For analysis of the operation stages, the following simplifying assumptions are adopted: (a) the converter is operating in steady state; (b) MOSFETs are replaced by ideal switches with a resistor R_{DSon} in series; (c) the magnetizing current of the transformer is considered null; (d) the inductance L_C represented in the circuit is the sum of the physical inductance L_r and the leakage inductance of the transformer primary L_d; (e) capacitors, inductors and diodes are considered ideal; (f) the output filter is replaced by a constant current source; (g) the output stage is reflected to the primary side of the transformer; and (h) the output voltage, the rectified voltage and the output current reflected to the primary side are represented, respectively, by V_o', V_{ret}' and I_o'.

Figure 2 shows the main waveforms, Figure 3 the operating stages and Figure 4 the equivalent circuits for the different topological states.

A. First Stage of Operation (t_0 - t_1) - [Figure 3.a]

In this operating stage, switches S_1, S_4 and S_5 are ON and S_2, S_3 and S_6 are OFF. The current i_{Lc}, in absolute value, becomes smaller than the output current I_o', and the four output rectifier diodes are forward biased. Thus, the current I_o' flows in freewheeling through the output diodes and the voltage V_{ret}' is zero. The input source V_{in} supplies energy to the capacitors, and the L_C inductor, and the current in L_C increases linearly from $-I_o'$ until reaching the value of I_o'. Capacitors C_S and C_2 are connected in parallel through switches S_1 and S_5, and the peak current in these capacitors is limited by the R_{DSon} of these switches. Disregarding the voltage drop across R_{DSon}, we have $V_{ab} = V_{Cs} = V_{C1} = V_{C2} = V_{Lc} = V_{in}/2$.

B. Second Stage of Operation (t_1 - t_2) - [Figure 3.b]

At instant t_1, the current i_{Lc} reaches I_o', and the diodes D_{o2} and D_{o3} are reverse biased. At this moment, V_{in} starts to supply energy to the load. The current i_{Lc} remains constant and equal to I_o', so the voltage drop across L_C is zero. Disregarding the voltage drop across R_{DSon}, we have $V_{ret}' = V_{ab} = V_{Cs} = V_{C1} = V_{C2} = V_{in}/2$.

C. Third Stage of Operation (t_2 - t_3) - [Figure 3.c]

At instant t_2, switches S_1 and S_5 are turned OFF and S_2 and S_6 are turned ON. Thus, switches S_2, S_4 and S_6 are conducting while S_1, S_3 and S_5 are blocked. Capacitors C_S and C_1 are connected in parallel through switches S_2 and S_6, and the peak current in these capacitors is limited by the R_{DSon} of these switches. The current in the L_C inductor

remains constant and equal to $I_o^{'}$, so the voltage drop across L_C is zero. Disregarding the voltage drop across R_{DSon}, we have $V_{ret}^{'} = V_{ab} = 0V$.

D. Fourth Stage of Operation (t_3 - t_4) - [Figure 3.d]

In this operating stage, switches S_2 and S_6 are ON and S_1 and S_5 are OFF. At instant t_3, switch S_3 is turned ON and S_4 is turned OFF. The current i_{Lc}, in absolute value, becomes smaller than $I_o^{'}$, and the four output rectifier diodes are forward biased. Thus, the current $I_o^{'}$ flows in freewheeling through the output diodes and the $V_{ret}^{'}$ is zero. The current in the L_C inductor decreases linearly from $I_o^{'}$ until it reaches $-I_o^{'}$. The voltage V_{ab} reverses polarity, assuming the value of $-V_{in}/2$.

E. Fifth Stage of Operation (t_4 - t_5) - [Figure 3.e]

At instant t_4, the current i_{Lc} reaches $-I_o^{'}$, and the diodes D_{o1} and D_{o4} are reverse biased. At this moment, V_{in} starts to supply energy to the load. The current i_{Lc} remains constant and equal to $-I_o^{'}$, so the voltage drop across L_C is zero. Disregarding the voltage drop across R_{DSon}, we have $V_{ret}^{'} = V_{Cs} = V_{C1} = V_{C2} = V_{in}/2$ and $V_{ab} = -V_{in}/2$.

F. Sixth Stage of Operation (t_5 - t_6) - [Figure 3.f]

At instant t_5, switch S_3 is turned OFF and S_4 is turned ON. The current i_{Lc} is constant and equal to $-I_o^{'}$, so the voltage drop across L_C is zero. Disregarding the voltage drop across R_{DSon}, we have $V_{ret}^{'} = V_{ab} = 0V$.

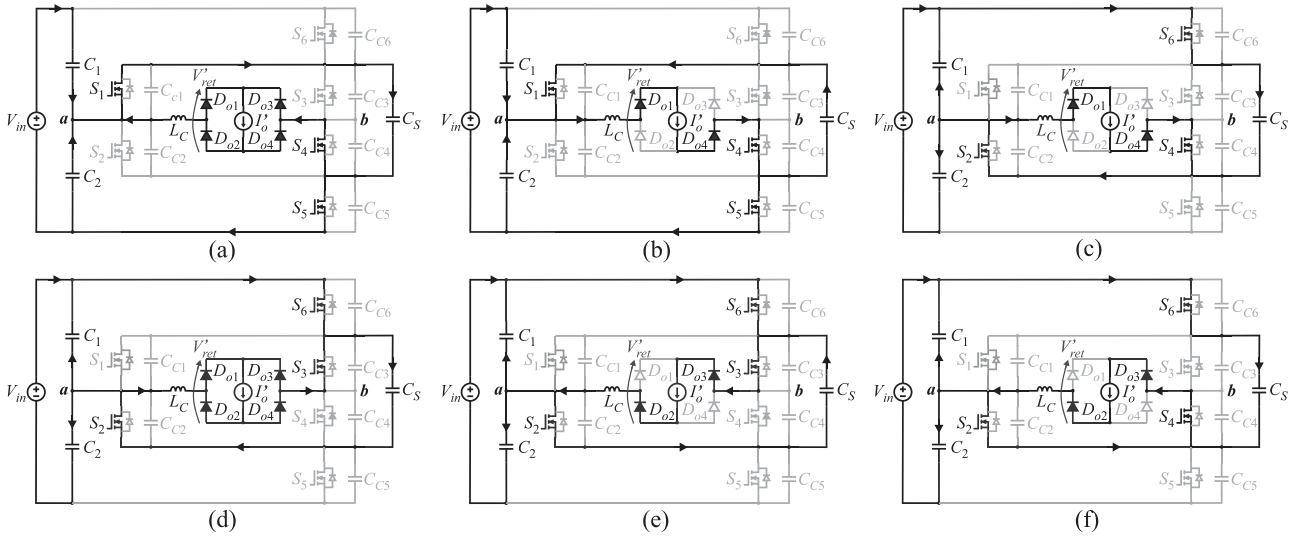

Fig. 3. Operation stages: (a) First stage ($t_0 - t_1$), (b) Second stage ($t_1 - t_2$), (c) Third stage ($t_2 - t_3$), (d) Fourth stage ($t_3 - t_4$), (e) Fifth stage ($t_4 - t_5$) and (f) Sixth stage ($t_5 - t_6$).

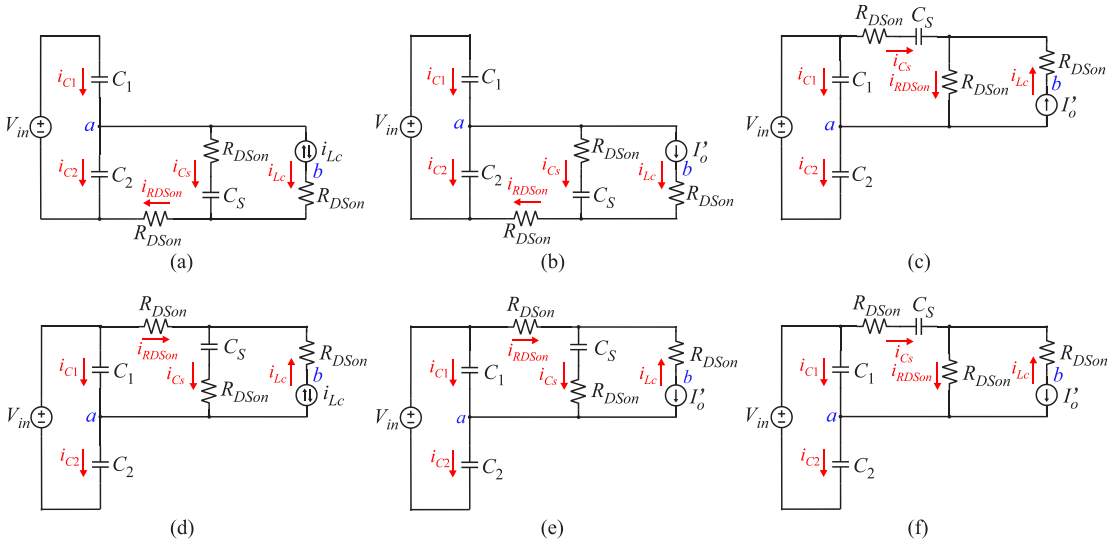

Fig. 4. Equivalent circuits of the operating stages: (a) First stage ($t_0 - t_1$), (b) Second stage ($t_1 - t_2$), (c) Third stage ($t_2 - t_3$), (d) Fourth stage ($t_3 - t_4$), (e) Fifth stage ($t_4 - t_5$) and (f) Sixth stage ($t_5 - t_6$).

IV. THEORETICAL ANALYSIS OF THE PROPOSED CONVERTER

The theoretical analysis of the static gain, the current stress in the inductor, the capacitors and switches, and the commutation of the proposed converter are presented in the next section.

*A. S*tatic Gain

According to the waveforms shown in Figure 2, the average output voltage is given by

$$V_o = \frac{V_{in}}{2n_{tr}}\left(D - \frac{2\Delta t_1}{T_s}\right) \tag{1}$$

where:

$n_{tr} = N_p / N_s$: transformer turns ratio;

N_p : number of turns of the primary winding;

N_s : number of turns of the secondary winding.

The static gain of the converter is represented by

$$q = \frac{V_o}{V_{in}} = \frac{1}{2n_{tr}}(D - \Delta D) \tag{2}$$

where the term ΔD is represented by

$$\Delta D = \frac{2\Delta t_1}{T_s} = \frac{8 f_s L_C I_o}{n_{tr} V_{in}} \tag{3}$$

which denotes the duty cycle loss caused by the voltage drop across the commutation inductance L_C.

Figure 5 shows the static gain as a function of ΔD, with the duty cycle D as a parameter. It shows that the converter presents a linear reduction of the static gain as a function of the load current, as occurs with the conventional FB-ZVS-PWM converter [19].

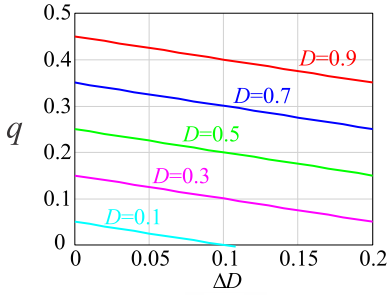

Fig. 5. Converter static gain as a function of duty cycle loss.

B. Current Stress on Inductor LC and Capacitors C1, C2 and CS.

From the equivalent circuits presented in Figure 4, the instantaneous currents in capacitors C_S and C_1 are defined by the expressions in Table I for each operating stage. Table I also provides the set of equations for instantaneous currents in L_C, and the initial conditions for the current in C_S, represented by $I_{Cs(10)}$ to $I_{Cs(60)}$.

Considering $C_1 = C_2 = C_S$, we define the time constant τ given by

$$\tau = \frac{4}{3} R_{DSon} C_S \ . \tag{4}$$

The effective current in the inductor L_C is determined by

$$I_{Lc,ef} = I_o' \sqrt{1 - \frac{2\Delta D}{3}} \ . \tag{5}$$

The effective currents in capacitors C_S, C_1 and C_2 are obtained through (6), (7) and (8).

$$I_{Cs,ef} = \sqrt{\frac{1}{T_s}\left\{\begin{array}{l}\int_{t_0}^{t_1}\left[i_{Cs(1)}(t)\right]^2 dt + \int_{t_1}^{t_2}\left[i_{Cs(2)}(t)\right]^2 dt \\ + \int_{t_2}^{t_3}\left[i_{Cs(3)}(t)\right]^2 dt + \int_{t_3}^{t_4}\left[i_{Cs(4)}(t)\right]^2 dt \\ + \int_{t_4}^{t_5}\left[i_{Cs(5)}(t)\right]^2 dt + \int_{t_5}^{t_6}\left[i_{Cs(6)}(t)\right]^2 dt\end{array}\right\}} \tag{6}$$

$$I_{C1,ef} = \sqrt{\frac{1}{T_s}\left\{\begin{array}{l}\int_{t_0}^{t_1}\left[i_{C1(1)}(t)\right]^2 dt + \int_{t_1}^{t_2}\left[i_{C1(2)}(t)\right]^2 dt \\ + \int_{t_2}^{t_3}\left[i_{C1(3)}(t)\right]^2 dt + \int_{t_3}^{t_4}\left[i_{C1(4)}(t)\right]^2 dt \\ + \int_{t_4}^{t_5}\left[i_{C1(5)}(t)\right]^2 dt + \int_{t_5}^{t_6}\left[i_{C1(6)}(t)\right]^2 dt\end{array}\right\}} \tag{7}$$

$$I_{C2,ef} = I_{C1,ef} \ . \tag{8}$$

C. Current Stress on Power Semiconductors

The effective currents in power semiconductors S_1, S_2, S_3, S_4, S_5 and S_6 are defined by the expressions (9), (10), (11), (12), (13) and (14), respectively.

$$I_{S1,ef} = \sqrt{\frac{1}{T_s}\left\{\int_{t_0}^{t_1}\left[i_{Cs(1)}(t)\right]^2 dt + \int_{t_1}^{t_2}\left[i_{Cs(2)}(t)\right]^2 dt\right\}} \tag{9}$$

$$I_{S2,ef} = \sqrt{\frac{1}{T_s}\left\{\begin{array}{l}\int_{t_2}^{t_3}\left[i_{Cs(3)}(t) + i_{Lc(3)}(t)\right]^2 dt + \int_{t_3}^{t_4}\left[i_{Cs(4)}(t)\right]^2 dt \\ + \int_{t_4}^{t_5}\left[i_{Cs(5)}(t)\right]^2 dt + \int_{t_5}^{t_6}\left[i_{Cs(6)}(t) + i_{Lc(6)}(t)\right]^2 dt\end{array}\right\}} \tag{10}$$

$$I_{S3,ef} = I_o' \sqrt{\frac{D}{2} - \frac{\Delta D}{3}} \tag{11}$$

$$I_{S4,ef} = I_o' \sqrt{1 - \frac{D}{2} - \frac{\Delta D}{3}} \tag{12}$$

$$I_{S5,ef}=\sqrt{\frac{1}{T_s}\left\{\begin{array}{l}\int_{t_0}^{t_1}\left[i_{Cs(1)}(t)+i_{Lc(1)}(t)\right]^2dt\\+\int_{t_1}^{t_2}\left[i_{Cs(2)}(t)+i_{Lc(2)}(t)\right]^2dt\end{array}\right\}} \quad (13)$$

$$I_{S6,ef}=\sqrt{\frac{1}{T_s}\left\{\begin{array}{l}\int_{t_2}^{t_3}\left[i_{Cs(3)}(t)\right]^2dt+\int_{t_3}^{t_4}\left[i_{Cs(4)}(t)-i_{Lc(4)}(t)\right]^2dt\\+\int_{t_4}^{t_5}\left[i_{Cs(5)}(t)-i_{Lc(5)}(t)\right]^2dt+\int_{t_5}^{t_6}\left[i_{Cs(6)}(t)\right]^2dt\end{array}\right\}} \quad (14)$$

TABLE I

Equations for the Current in the Inductor L_C and Current in Capacitors C_S and C_1 for Each Operating Stage

Operation Stages	Current in the inductor L_C	Current in capacitors C_S and C_1
1st Stage $0<t\le t_1=\frac{T_s\Delta D}{2}$	$i_{Lc(1)}(t)=\left(\frac{4}{T_s\Delta D}t-1\right)I_o^{'}$	$I_{Cs(10)}=I_o^{'}\frac{D-\Delta D+2f_s\tau\left(2-e^{-\frac{D}{2f_s\tau}}\right)-\frac{(2f_s\tau)^2}{\Delta D}\left(e^{-\frac{D-\Delta D}{2f_s\tau}}-e^{-\frac{D}{2f_s\tau}}\right)}{6f_s\tau\left(1-e^{-\frac{D}{2f_s\tau}}\right)}$ $i_{Cs(1)}(t)=I_{Cs(10)}e^{-\frac{t}{\tau}}-\frac{I_o^{'}}{3\Delta D}\left[4f_st+(2f_s\tau-\Delta D)\left(1-e^{-\frac{t}{\tau}}\right)\right]$ $i_{C1(1)}(t)=\frac{I_{Cs(10)}}{2}e^{-\frac{t}{\tau}}-\frac{I_o^{'}}{6\Delta D}\left[3\Delta D-8f_st+(2f_s\tau-\Delta D)\left(1-e^{-\frac{t}{\tau}}\right)\right]$
2nd Stage $t_1<t\le t_2=\frac{DT_s}{2}$	$i_{Lc(2)}(t)=I_o^{'}$	$I_{Cs(20)}=I_{Cs(10)}e^{-\frac{\Delta D}{2f_s\tau}}-\frac{I_o^{'}}{3\Delta D}\left[2\Delta D+(2f_s\tau-\Delta D)\left(1-e^{-\frac{\Delta D}{2f_s\tau}}\right)\right]$ $i_{Cs(2)}(t)=I_{Cs(20)}e^{-\left(\frac{t}{\tau}-\frac{\Delta D}{2f_s\tau}\right)}-\frac{I_o^{'}}{3}\left[1-e^{-\left(\frac{t}{\tau}-\frac{\Delta D}{2f_s\tau}\right)}\right]$ $i_{C1(2)}(t)=\frac{I_{Cs(20)}}{2}e^{-\left(\frac{t}{\tau}-\frac{\Delta D}{2f_s\tau}\right)}+\frac{I_o^{'}}{6}\left[2+e^{-\left(\frac{t}{\tau}-\frac{\Delta D}{2f_s\tau}\right)}\right]$
3rd Stage $t_2<t\le t_3=\frac{T_s}{2}$	$i_{Lc(3)}(t)=I_o^{'}$	$I_{Cs(30)}=I_o^{'}\frac{\Delta D(D-\Delta D)-(2f_s\tau)^2e^{\frac{\Delta D-1}{2f_s\tau}}+\left[(2f_s\tau)^2+4f_s\tau\Delta D\right]e^{-\frac{1}{2f_s\tau}}-f_s\tau\Delta D\left(6-4e^{\frac{D-1}{2f_s\tau}}\right)}{6f_s\tau\Delta D\left(1-e^{\frac{D-2}{2f_s\tau}}\right)}$ $i_{Cs(3)}(t)=I_{Cs(30)}e^{-\left(\frac{t}{\tau}-\frac{D}{2f_s\tau}\right)}$ $i_{C1(3)}(t)=-\frac{I_{Cs(30)}}{2}e^{-\left(\frac{t}{\tau}-\frac{D}{2f_s\tau}\right)}$
4th Stage $t_3<t\le t_4=\frac{T_s}{2}(1+\Delta D)$	$i_{Lc(4)}(t)=\left[\frac{-4}{T_s\Delta D}(t-t_3)+1\right]I_o^{'}$	$I_{Cs(40)}=I_{Cs(30)}e^{-\frac{1-D}{2f_s\tau}}+I_o^{'}$ $i_{Cs(4)}(t)=I_{Cs(40)}e^{-\left(\frac{t}{\tau}-\frac{1}{2f_s\tau}\right)}+\frac{I_o^{'}}{3\Delta D}\left\{2-4f_st-(2f_s\tau-\Delta D)\left[1-e^{-\left(\frac{t}{\tau}-\frac{1}{2f_s\tau}\right)}\right]\right\}$ $i_{C1(4)}(t)=-\frac{I_{Cs(40)}}{2}e^{-\left(\frac{t}{\tau}-\frac{1}{2f_s\tau}\right)}+\frac{I_o^{'}}{6\Delta D}\left\{4+3\Delta D-8f_st+(2f_s\tau-\Delta D)\left[1-e^{-\left(\frac{t}{\tau}-\frac{1}{2f_s\tau}\right)}\right]\right\}$
5th Stage $t_4<t\le t_5=\frac{(D+1)T_s}{2}$	$i_{Lc(5)}(t)=-I_o^{'}$	$I_{Cs(50)}=I_{Cs(40)}e^{-\frac{\Delta D}{2f_s\tau}}-\frac{I_o^{'}}{3\Delta D}\left[2\Delta D+(2f_s\tau-\Delta D)\left(1-e^{-\frac{\Delta D}{2f_s\tau}}\right)\right]$ $i_{Cs(5)}(t)=I_{Cs(50)}e^{-\left(\frac{t}{\tau}-\frac{1+\Delta D}{2f_s\tau}\right)}-\frac{I_o^{'}}{3}\left[1-e^{-\left(\frac{t}{\tau}-\frac{1+\Delta D}{2f_s\tau}\right)}\right]$ $i_{C1(5)}(t)=-\frac{I_{Cs(50)}}{2}e^{-\left(\frac{t}{\tau}-\frac{1+\Delta D}{2f_s\tau}\right)}-\frac{I_o^{'}}{6}\left[2+e^{-\left(\frac{t}{\tau}-\frac{1+\Delta D}{2f_s\tau}\right)}\right]$
6th Stage $t_5<t\le t_6=T_s$	$i_{Lc(6)}(t)=-I_o^{'}$	$I_{Cs(60)}=I_{Cs(50)}e^{-\frac{D-\Delta D}{2f_s\tau}}+\frac{I_o^{'}}{3}\left(2+e^{-\frac{D-\Delta D}{2f_s\tau}}\right)$ $i_{Cs(6)}(t)=I_{Cs(60)}e^{-\left(\frac{t}{\tau}-\frac{1+D}{2f_s\tau}\right)}$ $i_{C1(6)}(t)=-\frac{I_{Cs(60)}}{2}e^{-\left(\frac{t}{\tau}-\frac{1+D}{2f_s\tau}\right)}$

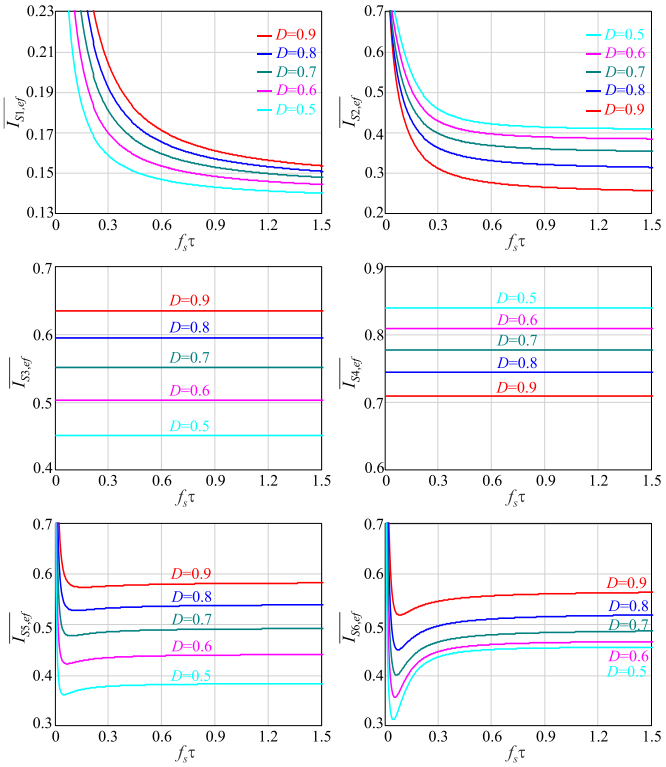

Fig. 6. Normalized effective current in semiconductors as a function of $f_s\tau$, with the duty cycle D as a parameter.

Figure 6 shows the effective currents in the power semiconductors normalized by $I_o^{'}$ and as a function of $f_s\tau$, with the duty cycle D as a parameter. It can be observed that the effective currents in S_1 and S_2 decrease exponentially with an increase in $f_s\tau$. Also, the effective currents at S_3 and S_4 are not dependent on the $f_s\tau$ factor and the effective currents at S_5 and S_6 are practically constant for $f_s\tau > 0.3$. The normalized effective current in semiconductors is defined by

$$\overline{I_{S,ef}} = \frac{I_{S,ef}}{I_o^{'}} \quad . \tag{15}$$

D. Normalized Equivalent Resistance of Equivalent Circuit

The total conduction losses, considering the six power semiconductors, are determined by (16).

$$P_{S,total} = R_{DSon}\left(I_{S1,ef}{}^2 + I_{S2,ef}{}^2 + I_{S3,ef}{}^2 + I_{S4,ef}{}^2 + I_{S5,ef}{}^2 + I_{S6,ef}{}^2\right) \tag{16}$$

The equivalent resistance considered for determining the conduction losses in the switches is obtained by

$$R_{eq} = \frac{P_{S,total}}{\left(I_o^{'}\right)^2} \quad . \tag{17}$$

The equivalent resistance normalized by R_{DSon} is defined by

$$\overline{R_{eq}} = \frac{R_{eq}}{R_{DSon}} \quad . \tag{18}$$

Figure 7.a shows the equivalent circuit considered for determining the conduction losses in the switches and Figure 7.b shows the normalized equivalent resistance curves as a function of $f_s\tau$, for different values of the duty cycle D. It can be observed that for $f_s\tau < 0.3$ the equivalent resistance increases exponentially, increasing the conduction losses in the power semiconductors, and for $f_s\tau > 0.3$ this resistance remains practically constant. For this reason, when selecting the values for the converter parameters, $f_s\tau \approx 0.3$ is adopted.

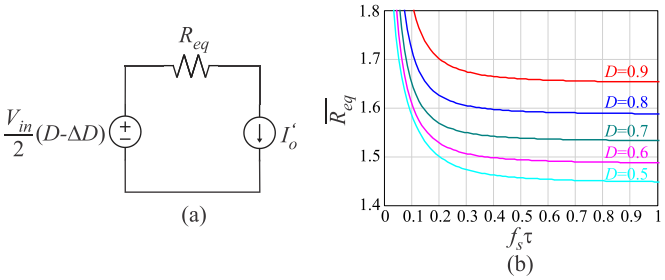

Fig. 7. (a) Equivalent circuit for determining conduction losses in power semiconductors and (b) normalized equivalent resistance.

V. COMMUTATION ANALYSIS

Each pair of switches has a linear commutation occurring at constant current equal to $I_o^{'}$, and a resonant commutation depending on the energy stored in L_C. To obtain soft switching over a wide range of load current, it is necessary to increase the value of L_C, which in turn causes a reduction in the value of the effective duty cycle and an increase in the conduction losses. Thus, to optimize the efficiency of the converter, there is a trade-off between the soft switching range and conduction losses.

The commutation of switches S_1, S_5 and S_2, S_6 occurs at a current in the capacitors C_C equal to a quarter of the current of the inductor L_C, while the commutation of switches S_3 and S_4 occurs at a current equal to half the current of the inductor L_C. The resonant commutation of switches S_1, S_5 and S_2, S_6 is considered the most critical since it defines the longest dead time necessary to ensure ZVS. For each switching stage, there are two topological states, one where the voltage transition occurs in the switching capacitors C_C and another from when the switch body diode starts to conduct until the corresponding switch is commanded to conduct with ZVS. Figures 8 to 11 show the two topological states of each commutation.

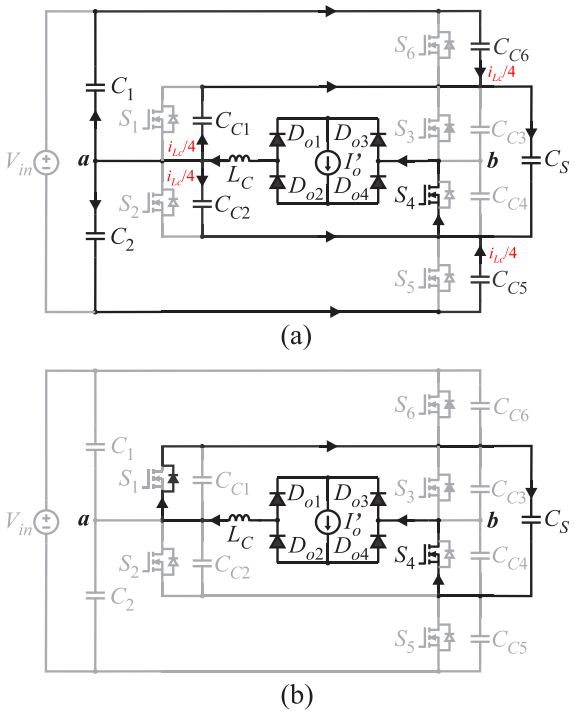

Fig. 8. Resonant commutation stages of switches S_1, S_2, S_5 and S_6: (a) voltage transition stage over the commutation capacitors and (b) body diode conduction stage.

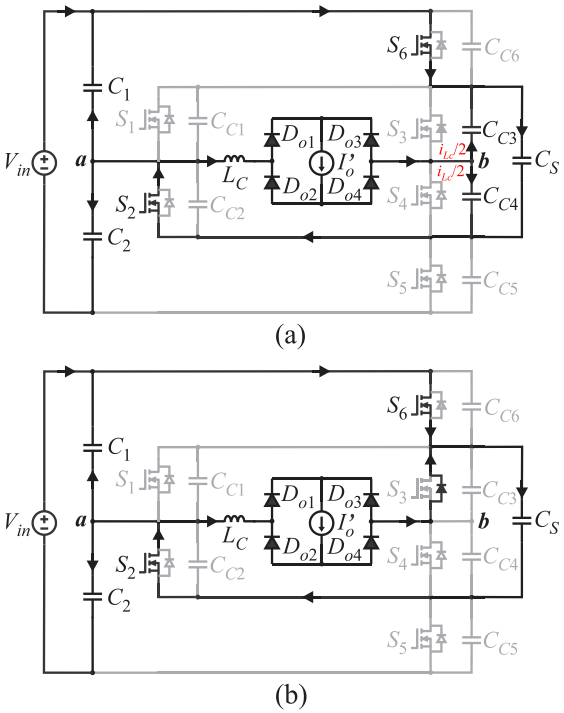

Fig. 10. Resonant commutation stages of switches S_3 and S_4: (a) voltage transition stage over the commutation capacitors and (b) body diode conduction stage.

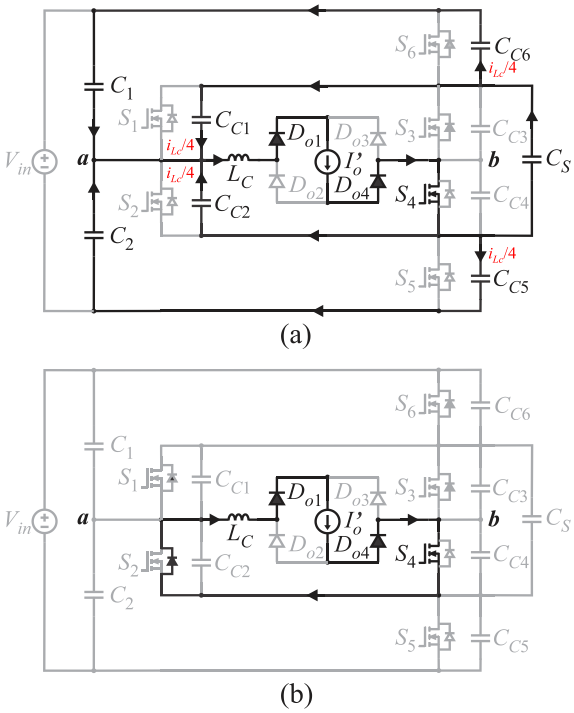

Fig. 9. Linear commutation stages of switches S_1, S_2, S_5 and S_6: (a) voltage transition stage over the commutation capacitors and (b) body diode conduction stage.

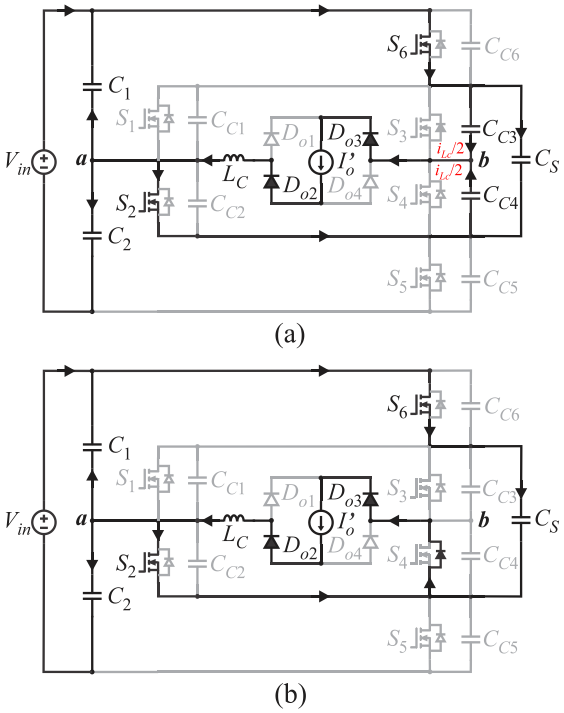

Fig. 11. Linear commutation stages of switches S_3 and S_4: (a) voltage transition stage over the commutation capacitors and (b) body diode conduction stage.

Figure 12 shows the main waveforms for commutation analysis, highlighting the resonant and linear commutation transients for each pair of switches. The resonant transitions are represented by Δt_{r1} and Δt_{r2}, the linear transitions by Δt_{l1} and Δt_{l2}, and the dead time by t_{d1} to t_{d4}.

Table II presents a summary of the switching times, dead time and the design constraints equations used to obtain the ZVS.

TABLE II
Summary with Equations for Switching Times, Dead Time and Constraints for ZVS

Commutation	Constraints for ZVS	Time interval	Equation
Resonant S_1, S_2, S_5 and S_6.	$I'_{o,zvs1} \geq \sqrt{\frac{4C_C}{L_C}}\frac{V_{in}}{2}$ and $\Delta t_{r1} < t_{d1} < t_{d1(\max)}$	Δt_{r1} $t_{d1(\max)}$	$\Delta t_{r1} = \left[\frac{\pi}{2} - \cos^{-1}\left(\frac{V_{in}}{2I'_o}\sqrt{\frac{4C_C}{L_C}}\right)\right]\sqrt{4L_CC_C}$ $t_{d1(\max)} = \Delta t_{r1} + \frac{2L_CI'_{o,zvs1}}{V_{in}}\cos\left(\frac{1}{\sqrt{4L_CC_C}}\Delta t_{r1}\right)$
Linear S_1, S_2, S_5 and S_6.	$t_{d2} > \Delta t_{l1}$	Δt_{l1}	$\Delta t_{l1} = \frac{2C_CV_{in}}{I'_o}$
Resonant S_3 and S_4.	$I'_{o,zvs2} \geq \sqrt{\frac{2C_C}{L_C}}\frac{V_{in}}{2}$ and $\Delta t_{r2} < t_{d3} < t_{d3(\max)}$	Δt_{r2}	$\Delta t_{r2} = \left[\frac{\pi}{2} - \cos^{-1}\left(\frac{V_{in}}{2I'_o}\sqrt{\frac{2C_C}{L_C}}\right)\right]\sqrt{2L_CC_C}$ $t_{d3(\max)} = \Delta t_{r2} + \frac{2L_CI'_{o,zvs2}}{V_{in}}\cos\left(\frac{1}{\sqrt{2L_CC_C}}\Delta t_{r2}\right)$
Linear S_3 and S_4.	$t_{d4} > \Delta t_{l2}$	Δt_{l2}	$\Delta t_{l2} = \frac{C_CV_{in}}{I'_o}$

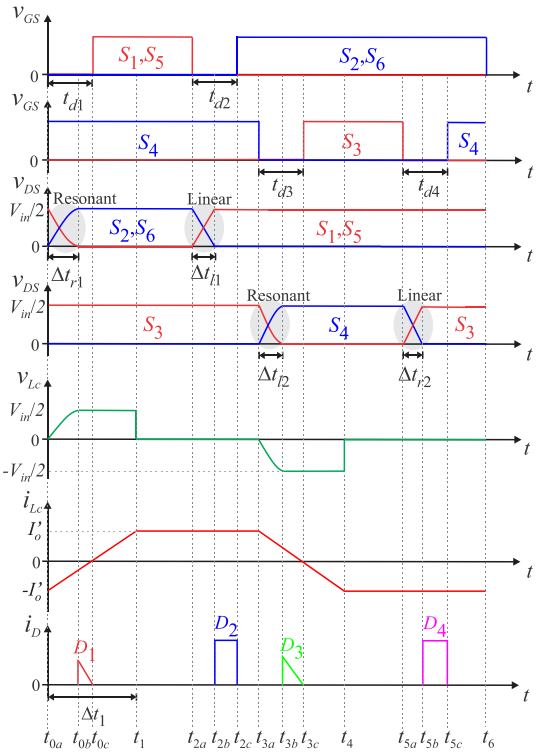

Fig. 12. Main waveforms for commutation analysis.

VI. THEORETICAL ESTIMATE OF LOSSES AND EFFICIENCY

Figure 13 shows the curves for the total conduction losses in power semiconductors as a function of $f_s\tau$ for different values of D. It can be noted that for $f_s\tau < 0.3$ the conduction losses increase exponentially and for $f_s\tau > 0.3$ they remain practically constant. Also, as the value of D increases these losses decrease. In this study, $f_s\tau = 0.316$ and $D = 0.92$ were adopted.

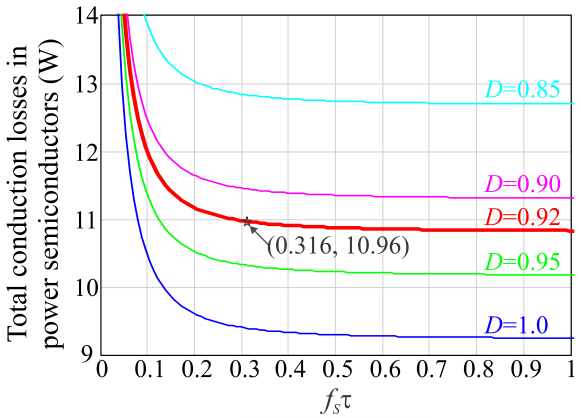

Fig. 13. Total conduction losses in power semiconductors as a function of $f_s\tau$, with the duty cycle D as a parameter.

Figure 14 shows the theoretical estimate of the losses distribution and efficiency of the HSC and NPC converter considering the specifications and components presented, respectively, in Tables III and IV. Compared with the NPC, the HSC converter has 0.89 W less losses in the MOSFETs and 5.52 W less in the output voltage clamping circuit, being consequently 0.3% more efficient.

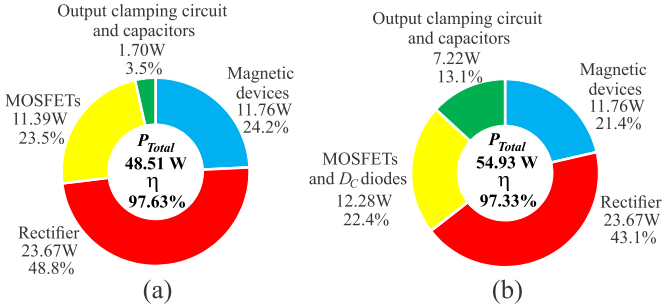

Fig. 14. Theoretical losses distribution in the converters: (a) HSC and (b) NPC.

VII. EXPERIMENTAL RESULTS

In order to validate the theoretical analysis of the proposed topology, a laboratory prototype was designed, built and tested. Its specifications are detailed in Table III.

The prototype was conceived to be reconfigurable, working as the HSC converter or as the NPC converter on the same printed circuit board.

A photograph of the prototype power stage is shown in Figure 15.

Figure 16 shows the respective schematic, configurable for the HSC or NPC converter.

Table IV provides a list of the components used in the construction of the power stage of the converter.

TABLE III
Converter Specifications

Parameter	Symbol	Value
Input voltage	V_{in}	800 V
Output voltage	V_o	60 V
Rated output power	P_o	2 kW
Switching frequency	f_s	100 kHz
ZVS range	$P_{o,ZVS}$	> 40% P_o
Duty cycle loss	ΔD	14%

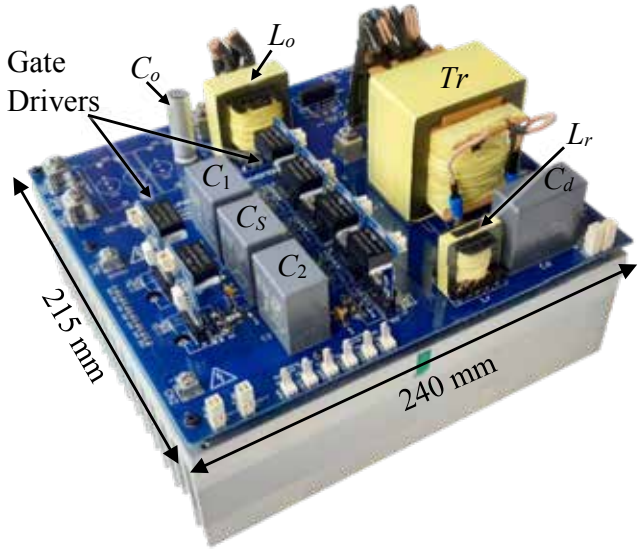

Fig. 15. Photograph of the laboratory prototype power stage in the HSC converter configuration.

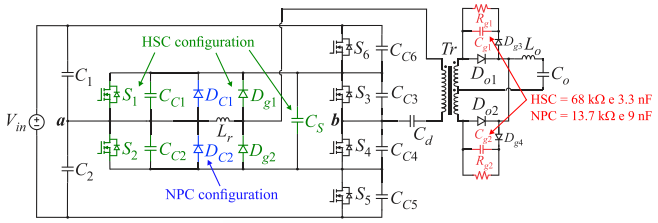

Fig. 16. Power stage schematic with HSC and NPC converter configuration options.

TABLE IV
Components Used in the Prototype

Reference	Description	Part Number
S_1 - S_6	SiC MOSFET 21 A / 650 V	SCT3120AL
D_{g1}, D_{g2}	Ultrafast diode 4 A / 600 V	MUR460
D_{C1}, D_{C2}	Ultrafast diode 4 A / 600 V	MUR460
D_{o1}, D_{o2}	Schottky diode 40 A / 250 V	MBR40250TG
C_1, C_2, C_S	Film capacitor 15 µF / 650 V	C4AQCBU5150A12J
C_{C1} - C_{C6}	Ceramic capacitor 150 pF / 1 kV	F151K25Y5RN63J5R
C_d	Film capacitor 4.7 µF / 650 V	-
C_o	Electrolytic capacitor 430 µF / 100V	UBY2A431MHL
C_{g1}, C_{g2}	Capacitor 3.3 nF (for HSC) Capacitor 9 nF (for NPC)	-
R_{g1}, R_{g2}	Resistor 68 kΩ / 3 W (for HSC) Resistor 13.7 kΩ (for NPC)	-
Tr	Core Thornton NEE-65/33/39 N_p = 26 turns (220 x 38 AWG) N_{s1} =N_{s2}= 5 turns (880 x 38AWG) n_{tr} = 5.2 Leakage inductance (L_d) = 8 µH	NEE-65/33/39 – 7200
L_r	Inductor L_r: 14 µH N = 9 turns (220 x 38 AWG) *Air gap (lg)* = 0.44 mm	MMT140EE3007
L_o	Inductor L_o: 12.65 µH N = 8 turns (880 x 38 AWG) *Air gap (lg)* = 1.15 mm	MMT140EE4215
PCB	FR4 / 2oz / 240 x 215 x 1.6 mm	FB-ZVS-PWM-HSC

Figure 17.a shows that the output characteristics of the HSC and NPC converters are identical, with a linear drop in the output voltage as a function of the load current.

Figure 17.b shows the voltage across the voltage divider capacitors C_1 and C_2 as a function of the output power. It can be observed that, for the HSC converter, the voltages on the capacitors remain naturally equalized for the entire output power range, while, for the NPC, the voltages on the capacitors are unbalanced and vary with the power, reaching a difference of up to 40 V.

The effect of the asymmetry of the command signals of the switches on the voltage balance in capacitors C_1 and C_2 was also evaluated by numerical simulation. It was verified that, for the NPC, a difference of 5% between the command signals causes an unbalance of 20 V in capacitors C_1 and C_2. While, for the HSC, the voltages on the capacitors remain balanced.

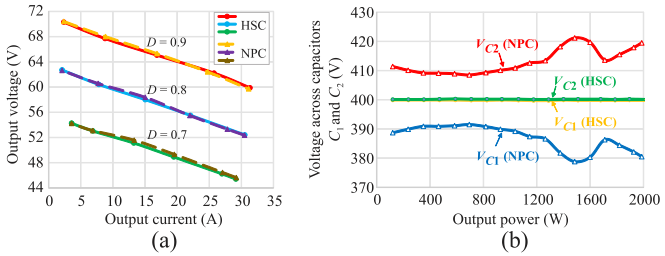

Fig. 17. (a) Output characteristic of the HSC and NPC converter and (b) voltage across capacitors C_1 and C_2 as a function of output power.

Figure 18 shows the efficiency curve as a function of the output power P_o for the HSC and NPC converters. It can be noted that the HSC converter presents a maximum efficiency of 97.12% at 816 W output power, while the NPC reaches 96.49% at 1150 W output power. The HSC converter presents higher efficiency than the NPC for the entire power range between 240 W and 2 kW. This higher efficiency of the HSC is mainly because it allows the use of a regenerative clamping circuit on the primary side of the converter, thus reducing the losses in the clamping circuit of the output diodes.

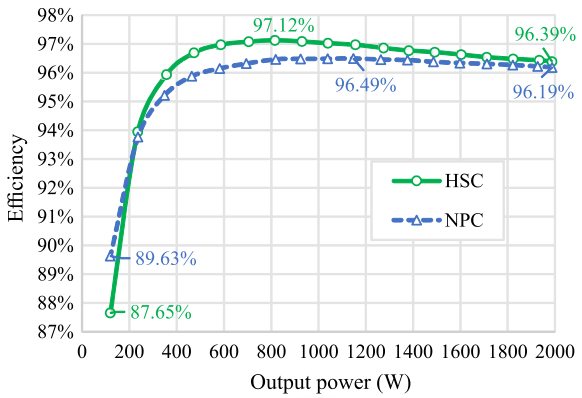

Fig. 18. Efficiency curves for HSC and NPC converters.

The losses in the output voltage clamping circuit were 772 mW for the HSC converter and 5.16 W for the NPC converter. Added to this is the fact that the HSC converter operates with lower conduction losses in the input power semiconductors (switches and diodes), as shown in Figure 19.

Figures 20 and 21 show, respectively, the typical waveforms during the commutation of the power semiconductors of the HSC and NPC, and the soft commutation threshold of each of them.

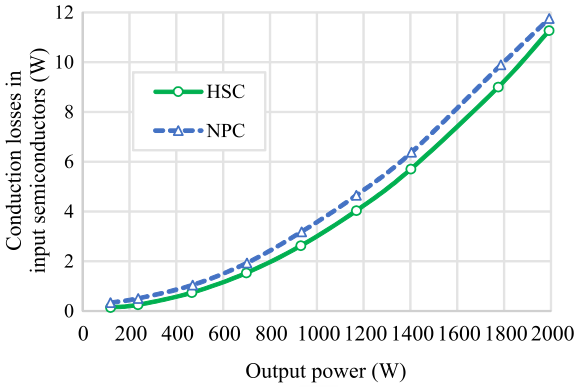

Fig. 19. Total conduction losses in the input semiconductors of the HSC converter and the NPC converter.

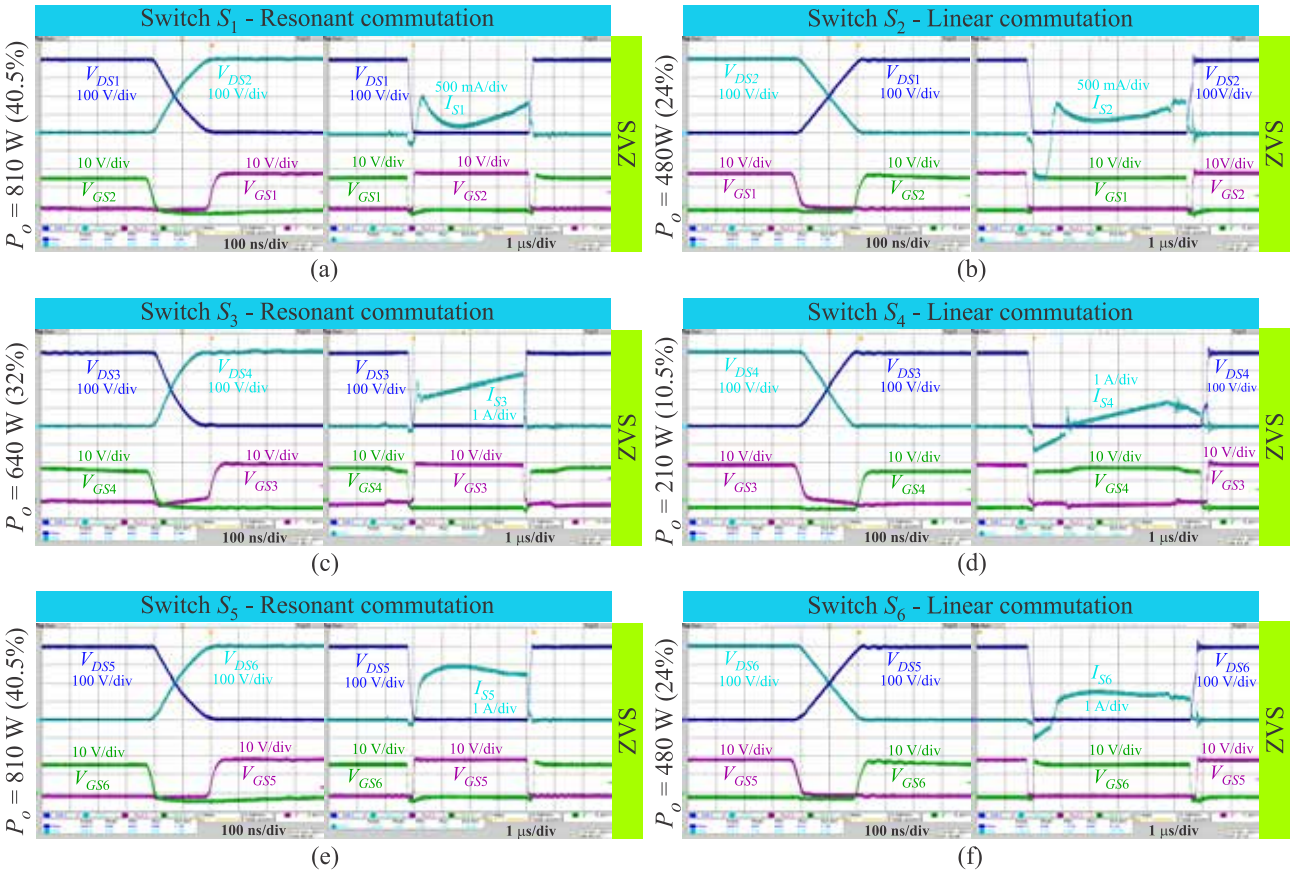

Fig. 20. Experimental results for the soft commutation threshold of each switch of the HSC converter: (a) commutation S_1, (b) commutation S_2, (c) commutation S_3, (d) commutation S_4, (e) commutation S_5 and (f) commutation S_6.

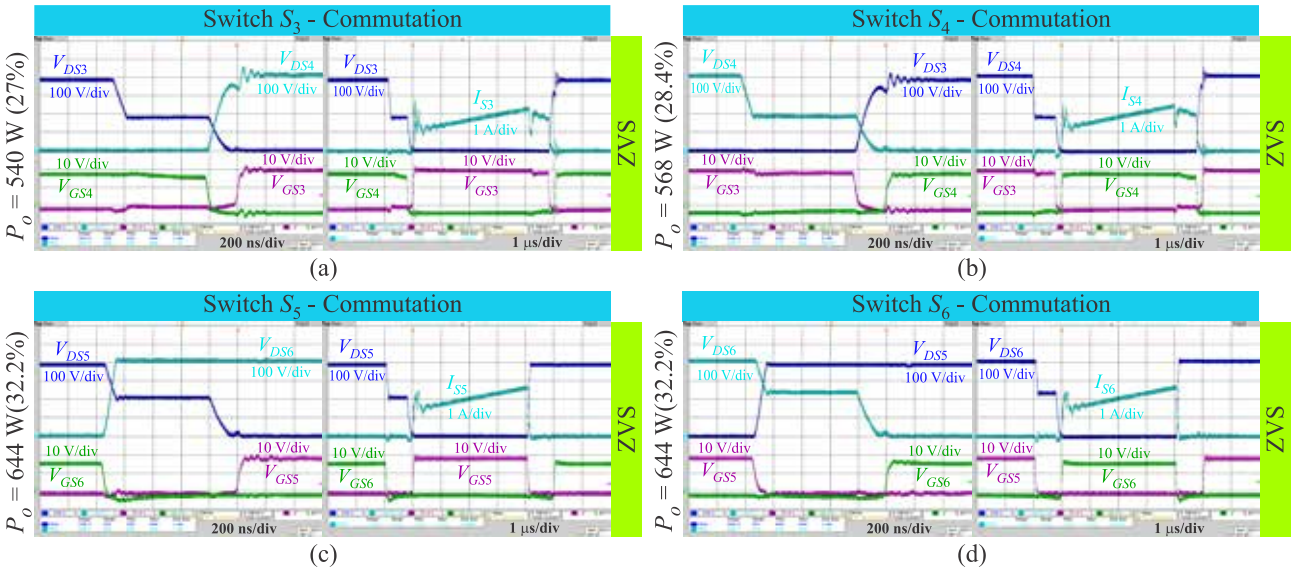

Fig. 21. Experimental results for the soft commutation threshold of each switch of the NPC converter: (a) commutation S_3, (b) commutation S_4, (c) commutation S_5 and (d) commutation S_6.

TABLE V
Comparison of the Theoretical and Experimental ZVS Threshold

HSC			
Switch	Theoretical	Experimental	Error
S_1	34.7%	40.5%	16.7%
S_2	21.1%	24.0%	13.7%
S_3	33.4|%	32.0%	4.2%
S_4	10.5%	10.5%	0.0%
S_5	34.7%	40.5%	16.7%
S_6	21.1%	24.0%	13.7%
NPC			
Switch	Theoretical	Experimental	Error
S_3	21.2%	27.0%	27.4%
S_4	21.2%	28.4%	34.0%
S_5	21.2%	32.2%	51.9%
S_6	21.2%	32.2%	51.9%

Table V shows a comparison between the theoretical and experimental values of the ZVS threshold for the HSC and NPC converters. It represents the minimum values in terms of the percentage of rated output power that ensures ZVS. The theoretical values for the HSC converter were calculated considering a dead time of 200 ns. It can be seen that the theoretical and experimental values for the HSC converter are very close, with a maximum error of 16.7%, thus validating the theoretical analysis performed.

The experimental results show that the HSC converter presents soft commutation in all switches from 810 W of output power (40.5% of the rated power) and the NPC from 644 W (32.2% of the rated power). It is also observed that switches S_2, S_4, and S_6 of the HSC converter have a wider soft commutation range than the switches of the NPC converter.

VIII. CONCLUSIONS

A new isolated DC-DC converter topology, generated through the integration of the full-bridge converter with the switched-capacitor ladder cell, with reduced voltage on the switches, was proposed, analyzed, dimensioned and tested in the laboratory. The experimental results validated the theoretical analysis. A comparative analysis of the proposed HSC converter with the NPC converter showed that the HSC has the advantages of spontaneous voltage equalization on the capacitors, lower conduction losses, it allows voltage clamping in the transformer primary side, and it is easy to expand to more voltage levels. On the other hand, the NPC converter presents a wider ZVS range and a smaller number of switches.

The main features of the new converter are:

- spontaneous voltage equalization in the capacitors;
- the input stage components are subjected to half the bus voltage;
- it allows generalization to divide the voltage into more levels;
- it allows the use of a simple, non-dissipative voltage clamper in the primary side;
- a wide range of soft commutation is possible; and
- high efficiency can be achieved.

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BIOGRAPHIES

Anderson Alves was born in Florianópolis, Brazil. He received B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, SC, Brazil, in 1999 and 2002, respectively.

He worked as a researcher for Whirlpool Latin America group, Joinville, Brazil, from 2002 to 2012 and 2013 to 2015. Since 2016 he has been a Professor with the Department of Electronics, Federal Institute of Santa Catarina (IFSC), Florianópolis, SC, Brazil.

He is currently a PhD student in Electrical Engineering at UFSC, in the Power Electronics and Electrical Drives area.

Ivo Barbi (Life Fellow, IEEE) was born in Gaspar, Brazil. He received B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, SC, Brazil, in 1973 and 1976, respectively, and a Dr.Ing. degree in electrical engineering from the Institut National Polytechnique de Toulouse (INPT), Toulouse, France, in 1979.

He founded the Brazilian Power Electronics Society (SOBRAEP), the Brazilian Power Electronics Conference (COBEP) in 1990, and the Brazilian Power Electronics and Renewable Energy Institute (IBEPE) in 2016. He is currently a researcher with the Solar Energy Research Center and a Professor Emeritus in electrical engineering with UFSC. He served as an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the IEEE TRANSACTIONS ON POWER ELECTRONICS for several years.

Prof. Barbi received the 2020 IEEE William E. Newell Power Electronics Award.