INTEGRATED ZETA – FLYBACK CONVERTER TO SUPPLY HID LAMPS

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***Abstract*— This paper proposes a Metal Halide (MH) lamp electronic ballast based on the integration of Zeta and Flyback converters working in discontinuous conduction mode, in order to provide the ballast power factor correction and to stabilize the lamp current, respectively. The proposed integration besides to reduce the number of ballast components, presents no additional current stress in the shared switch. The lamp is supplied with a low frequency square waveform (400Hz) to avoid the acoustic resonance phenomenon. The proposed topology has been implemented for an input voltage of 110V, 50Hz, in order to supply a 35W MH lamp.**

***Keywords* – Acoustic resonance, electronic ballast, HID lamps, integrated circuits.**

I. INTRODUCTION

Metal Halide (MH) lamps have proven to be suitable for indoor applications due to their characteristics of high color rendering index (CRI) and high luminous efficacy (around 100 lm/W). Besides, in order to achieve good efficiency, no light flicker, audible noise absence, and compact size, these lamps must be supplied by electronic ballasts. However, the operation of these lamps under high frequency current waveforms is susceptible to the occurrence of the acoustic resonance (AR) phenomenon. When the frequency imposed to the lamp is increased and an eigenfrequency is approached, pressure waves become propagational and disturb the discharge path [1]. So, supplying these lamps with a high-frequency (20 to 100 kHz) sinusoidal waveform, as it is done usually with low pressure discharge lamps, such as fluorescent lamps is a difficult task.

Many alternatives have been proposed to avoid the AR, e.g.: avoiding the frequencies where the AR appears by means at low-frequency square-waveform (LFSW) ballasts [2] or extra-high-frequency ballasts [3]; lamp operation in a free-resonance window [4]; high-frequency square-waveform supply [5]; lamp operation with suitable frequency modulated waves, where the threshold value to excite the AR is not achieved [6]; and lamp operation with sinusoidal waveform superposed with third harmonic [7].

The use of a low frequency square waveform (LFSW) to supply the lamp is an option adopted by many researchers in order to deliver constant power to the lamp and avoid the AR occurrence. Conventionally, in this way, a three stages electronic ballast is needed, where: 1) Power factor correction stage (PFC); 2) Lamp power control stage (LPC); and 3) Inverter stage. So, as can be seen, this solution leads to a complex circuit that requires a high number of components, what increases the power losses and the ballast final cost. One of the ideas proposed in the literature to solve the problem is the integration of power stages in order to reduce the number of components of the electronic ballast, thus becoming more attractive to the industry [8-11].

In this way, a single-stage electronic ballast is presented, which consists of integrating a Zeta converter to provide the PFC and a Flyback converter to control the lamp power, without additional current stress in the main switch. The Flyback inductor includes two secondary windings that work complementary to supply the lamp with a LFSW current.

II. PROPOSED INTEGRATION

When two converters are integrated some disadvantages have to be faced. For example, in the integrated topologies proposed in [8], the current handled by the shared switch is the addition of the current of each integrated stage. On the other hand, even though the integration proposed in [9] avoids this effect, the design of this topology for low-voltage mains (90-110V) is very difficult due to the high dependence of the power factor (PF) on the difference between the main voltage and bus voltage.

The solution proposed in this work is the integration of a Zeta and a Flyback converter working in a discontinuous conduction mode (DCM). The shared switch handles only one of the converter currents instead of their addition. Moreover, the input characteristics of the Zeta converter allow it to be used to all range of input voltages (90V – 220V).

The proposed topology is shown in Figure 1, which excludes the rectifier stage that is formed by D_1-D_4 diodes arranged in a single-phase bridge.

The Zeta converter is implemented in the PFC stage, and the Flyback converter is used to guarantee the lamp desired operation.

The use of the Flyback converter in the LPC stage allows the employment of a Half-Bridge inverter to provide the alternating lamp current (square waveform).

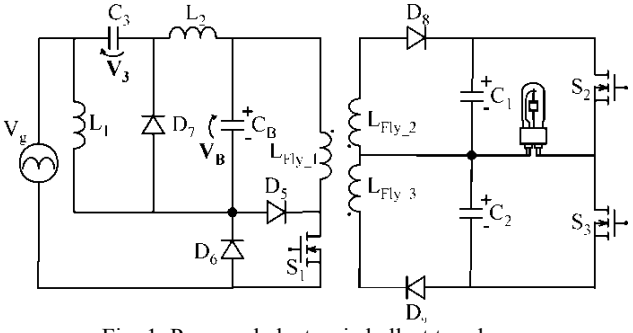

Fig. 1. Proposed electronic ballast topology.

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To understand how the current is distributed among the main switch (S_1) and diodes D_5 and D_6, the equivalent circuit shown in Figure 2 can be depicted.

In this circuit, it can be seen that switch S_1 will handle only the highest current between the two integrated converters (i_{Fly} or $i_{L1}+i_{L2}$). The diode in parallel with the highest current will be open, whereas the diode in parallel with the lowest current will be close. Since the operation is in DCM, the two Zeta and Flyback currents are ramp waveforms starting at the same instant. During one line half period the switch can handle either the Flyback or the Zeta current, because in a specific operation point the Flyback current ramp is nearly constant and will be affected only by the dc bus voltage ripple, and the Zeta current ramp will depend on the instantaneous line voltage value. Therefore, the conclusion is that the current through switch S_1 will be either i_{Fly} or $i_{L1}+i_{L2}$, whichever is higher, but not the addition of the two currents.

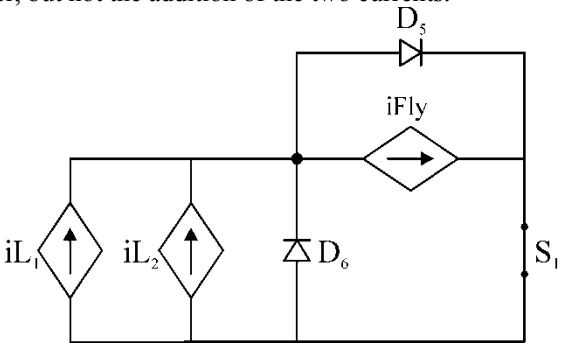

Fig. 2. Equivalent circuit during conduction of S_1.

III. OPERATION MODES

The operation modes of the proposed integration are analyzed through the theoretical waveforms in Figure 3 and illustrated in Figure 4. Both converters operate in a DCM and the load of the integrated stages is considered to be the inverter + lamp.

A. Mode I or II

These modes begin when the main switch S_1 in turned on. The voltage V_3 is equal to V_B. So, the input voltage is applied to the both inductors of Zeta converter (L_1 and L_2).

Currents i_{L1} and i_{L2} increase linearly. At the same time, voltage V_B is applied to L_{Fly_1} charging the Flyback coupled inductors. When $(i_{L1}+i_{L2}) > i_{Fly}$ the mode I shown in Figure4 takes place. On the other hand, when $(i_{L1}+i_{L2}) < i_{Fly}$ the converter operation is in mode II.

These cases can be better analyzed through the theoretical waveforms shown in Figure 3. In the case that $(i_{L1}+i_{L2}) > i_{Fly}$ the shared switch (S_1) handle ($i_{L1}+i_{L2}$) current. It occurs when the input voltage is near to its highest value. On the other hand, when $(i_{L1}+i_{L2}) < i_{Fly}$ the current handled by the shared switch is i_{Fly}. So, depending on the operation point along to the variation of the input voltage mode I or II can takes place.

The lamp during these modes is supplied by the energy stored in capacitor C_{1-2}.

B. Mode III

In this mode switch S_1 is turned off. The currents through inductors L_1 and L_2 decrease linearly through diode D_7, as can be seen in the theoretical waveforms in Figure 3. The value of inductance L_1 is projected to be lower than L_2. So, as they are submitted to the same discharge voltage ($V_B=V_3$), the current through inductor L_1 reaches zero faster than that through L_2, and then it becomes negative until $i_{L2}=-i_{L1}$. At this instant D_7 stops conducting and mode IV begins.

In the LPC stage, the energy stored in the coupled inductors of Flyback converter is now discharged to capacitor C_{1-2} and inverter + lamp.

C. Mode IV

This is a freewheeling mode. When $i_{L2}=-i_{L1}$ diode D_7 is out of conduction and as $V_3=V_B$ the current in both inductors remains constant. During this stage the load is supplied by the energy stored in C_{1-2}.

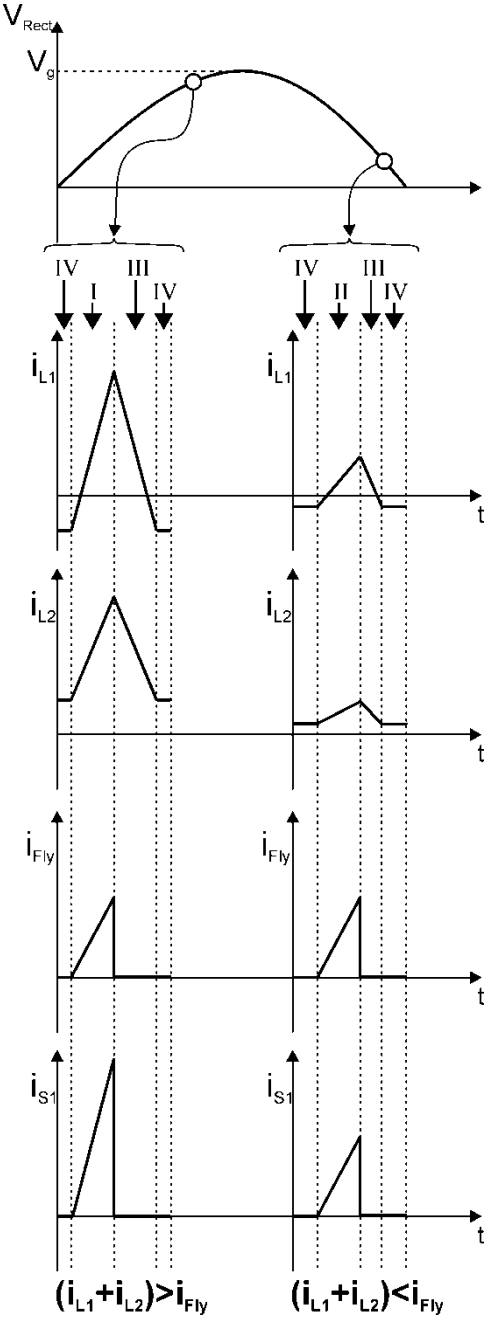

Fig. 3. Theoretical waveforms for both cases: $(i_{L1}+i_{L2})>i_{Fly}$ and $(i_{L1}+i_{L2})<i_{Fly}$.

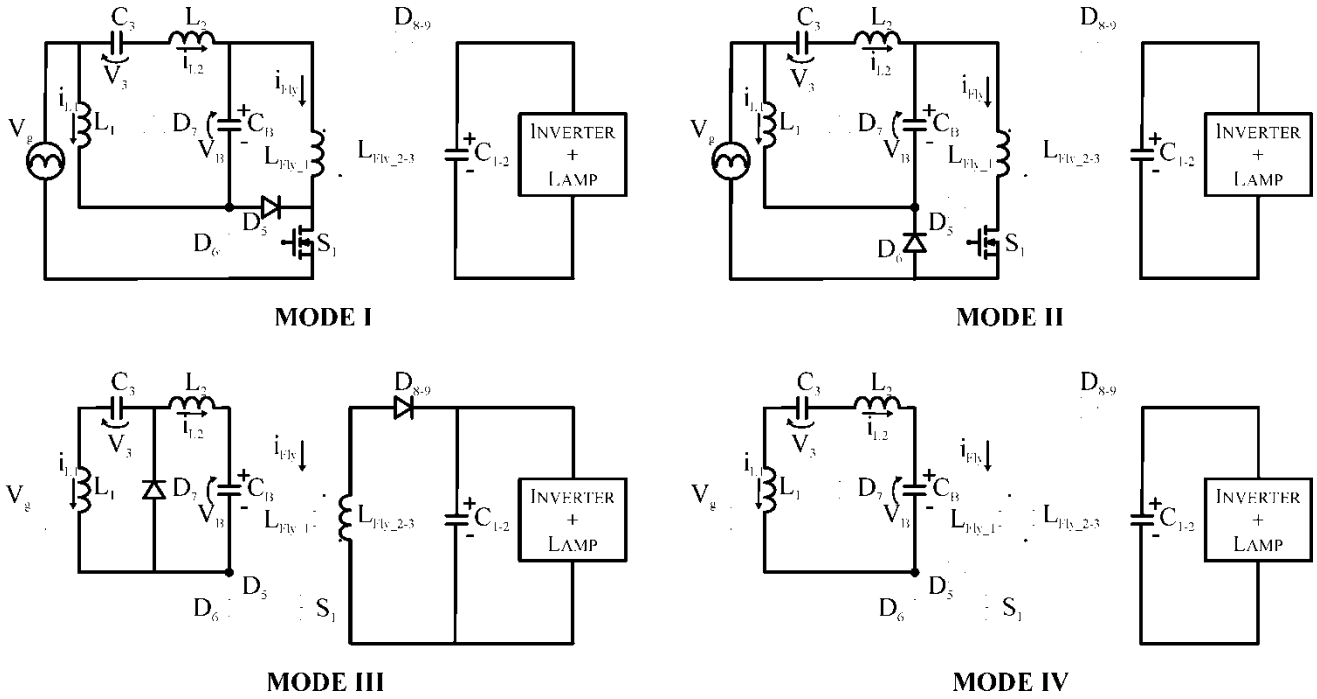

Fig. 4. Electronic ballast operation modes.

IV. DESIGN OF THE PROPOSED INTEGRATED CONVERTER

Figure 5 illustrates the low frequency equivalent circuit of the proposed converter for an idealized situation (efficiency equal to 100%). This circuit is used to analyze the characteristic of the bulk capacitor voltage (V_B), which is the common voltage of PFC and LPC stages. In this way, as both converters operate in DCM, they can be represented by their equivalent input resistances R_{Fly} and R_{Zeta}, which can be expressed, according [9], as follows:

$$R_{Fly} = \frac{2.L_{Fly\_1}}{D^2.T_s} \tag{1}$$

$$R_{Zeta} = \frac{2.L_e}{D^2.T_s} \tag{2}$$

where D is the duty cycle, T_s is the switching period, L_{Fly_1} is the primary Flyback inductance and L_e is the Zeta equivalent inductance (L_1//L_2).

The output current of the Zeta converter $i_B(t)$ can be calculated by equaling input and output powers. The following expression is obtained:

$$i_B(t) = \frac{1}{2}.\frac{{V_g}^2.D^2.T_s}{V_B.L_e}.(\sin \omega.t)^2 \tag{3}$$

where V_g is the input voltage peak value.

The dc component of this current, I_B, can be obtained by integration, as follows:

$$I_B = \frac{1}{\pi}.\int_0^{\pi} i_B(t).dt = \frac{1}{4}.\frac{{V_g}^2.D^2.T_s}{V_B.L_e}. \tag{4}$$

Finally, the bulk capacitor voltage can be derived. Assuming negligible voltage ripple, it can be approximated by its dc component, as shown in the following equation:

$$V_B = I_B.R_{Fly} = \frac{1}{2}.\frac{{V_g}^2.L_{Fly\_1}}{V_B.L_e} \tag{5}$$

The following parameters are defined for simplification:

$$m = \frac{V_g}{V_B} \tag{6}$$

and

$$\alpha = \frac{L_e}{L_{Fly\_1}} \tag{7}$$

Using (6) and (7) in (5), the following expression is obtained:

$$\alpha = \frac{1}{2}.m^2 \tag{8}$$

Therefore, as shown by (8), the operation of the integrated stages in DCM makes the dc bus voltage (V_B) independent on load, duty ratio and switching frequency; it only depends on the ac input voltage and the ratio between the Zeta and Flyback inductances (α).

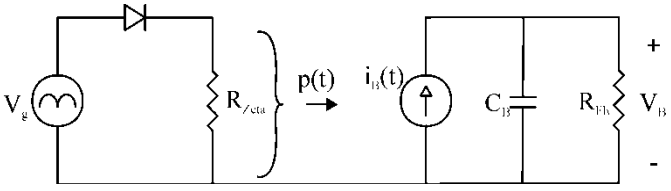

Fig. 5. Low frequency equivalent circuit of the proposed ballast.

Equation (8) has been plotted in Figure 6, which is the main characteristic to carry out the design of the proposed converter.

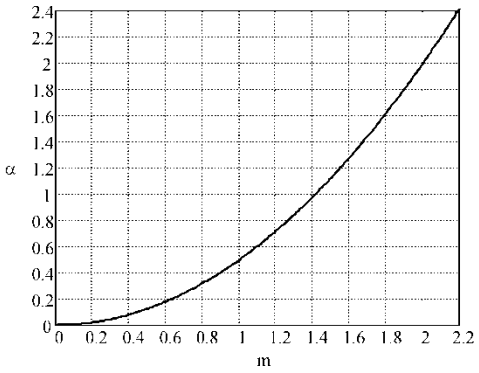

Fig. 6. Voltage ratio m as a function of the inductance ratio α.

The Flyback inductances need to be designed to guarantee the operation of the converter in a DCM, and are calculated according to the procedure presented in [9]. After that, Zeta equivalent inductance L_e can be calculated from (7).

Now, to calculate the value of L_1 and L_2 inductances of Zeta converter a maximum peak to peak current ripple (Δi_B) in L_2 must be chosen. It is defined by the following equation:

$$\Delta i_B = \frac{V_g\, D T_s}{L_2} \tag{9}$$

Representing equation (3) as:

$$i_B(t) = I_{B\_P}\left(\sin \omega t\right)^2 \tag{10}$$

where I_{B_P} is the $i_B(t)$ current peak value. The current ripple factor (δ) is defined as follows:

$$\delta = \frac{\Delta i_B}{I_{B\_P}}. \tag{11}$$

Therefore, using, (3), (9), (10) and (11), the L_2 value can be calculated:

$$L_2 = \frac{2 L_e}{\delta m D} \tag{12}$$

And, consequently, as $L_e = L_1 // L_2$,

$$L_1 = \frac{2 L_e}{2 - \delta m D} \tag{13}$$

Another important issue that must be analyzed before a complete design can be performed is the voltage ripple across the bulk capacitor (ΔV_B), which must be limited to an appropriate value. The peak-to-peak voltage ripple across the bulk capacitor can be calculated as follows:

$$\Delta V_B = \frac{\Delta Q}{C_B} = \frac{1}{2\omega C_B}\int_0^{\pi} \left| i_B(t) - I_B \right| \, dt \tag{14}$$

The bus voltage ripple factor (r) is defined below:

$$r = \frac{\Delta V_B}{V_B}. \tag{15}$$

Then, according to a desired bus voltage ripple, the capacitor C_B value can be calculated:

$$C_B = \frac{m^2 D^2 T_s}{8 \pi L_e f r}, \tag{16}$$

where f is the line frequency.

V. DESIGN EXAMPLE AND EXPERIMENTAL RESULTS

Considering the previously described analysis and equations, an electronic ballast is projected and implemented for an input voltage of 110V, 50Hz, in order to supply a 35W MH lamp. The electronic ballast was designed to have a voltage ratio of m = 1.55, resulting in the relation between the inductances α = 1.2, as can be obtained from the graphic in Figure 6.

The Flyback inductances, designed according to [9], to guarantee the operation in a DCM are: L_{Fly_1}= 223μH and L_{Fly_2}= L_{Fly_3}= 512μH.

Considering (12) and (13) the Zeta inductances L_1 and L_2 are calculated to be 362μH and 1mH, respectively. The converters switching frequency is 80 kHz and the duty cycle for the steady state operation is around 37%.

The projected values and employed components are presented in table I.

TABLE I
Commercial Components

D_5, D_6, D_7, D_8 and D_9	UF4007
C_B	Electrolytic capacitor 250 μF / 250V
S_1	IRFPE50
S_2 and S_3	IRF840
C_1=C_2	Polypropylene capacitor 220 nF / 630 V
C_3	Polypropylene capacitor 100 nF / 630 V

Some experimental results are illustrated in Figures. 7, 8, 9, 10, 11 and 12. Figure 7 shows the input line voltage and current, where an input power factor of 0.998 is obtained. Figure 8 shows the lamp voltage and current (400Hz). As previously described the lamp is operated with a LFSW to avoid the acoustic resonance phenomenon.

Figure 9 presents the current handled by the shared switch. As can be seen this current is not the addition of the two stages current but the highest current of each stage. The shared switch peak voltage and current is shown in detail in Figure 10.

Figure 11 presents the inductors current of Zeta converter. The maximum output current ripple (Δi_B) in L_2 is calculated to be 800mA. As can be seen, the L_1 inductor value is able to guarantee the DCM of the converter.

The bus capacitor voltage is shown in Figure 12. It is calculated to a voltage ripple (r) of approximately 5%. Its value is 220μF.

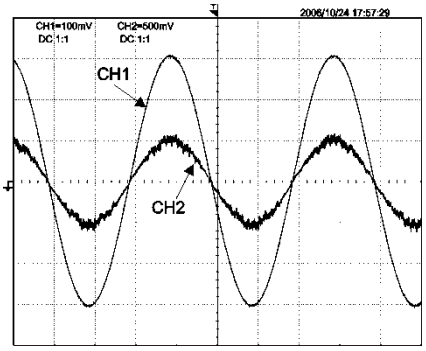

Fig. 7. Input voltage (CH1-50V/div) and current (CH2-500mA/div), 5ms/div.

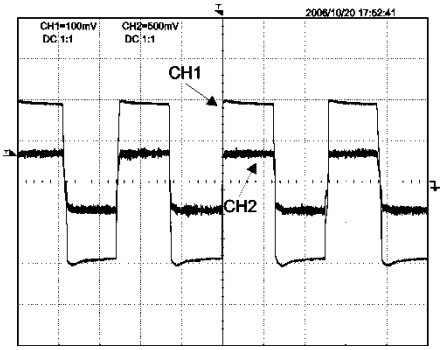

Fig. 8. Lamp voltage (CH1-50V/div) and current (CH2-500mA/div), 1ms/div.

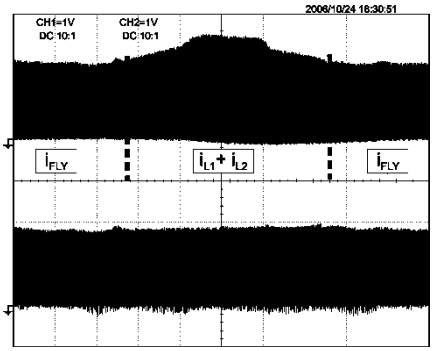

Fig. 9. Shared switch current (top trace – 1A/div) and primary Flyback current (bottom trace – 1A/div), 1ms/div.

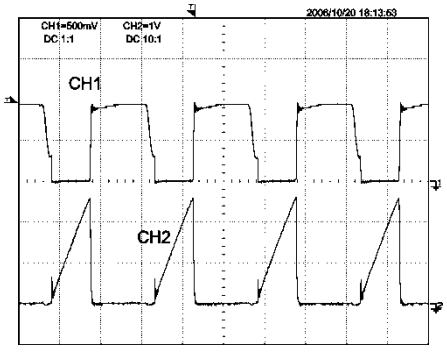

Fig. 10. Shared switch voltage (CH1-250V/div) and current (CH2-1A/div), 5μs/div.

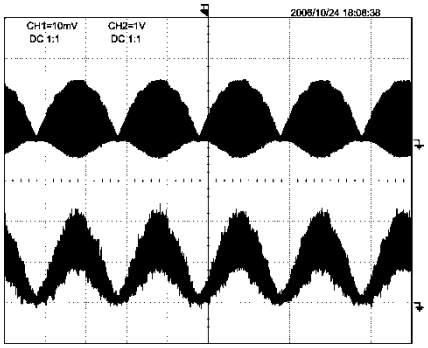

Fig. 11. Zeta converter inductors current: L_1 (top trace - 1A/div) and L_2 (bottom trace - 500mA/div), 5ms/div.

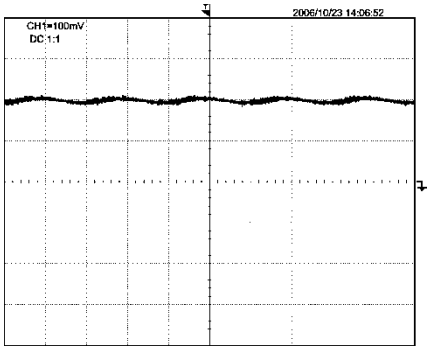

Fig. 12. Bus capacitor voltage (50V/div), 5ms/div.

VI. CONCLUSION

The integration of power stages to supply MH lamps is pointed as a solution to reduce the ballast final cost and to increase its efficiency. Considering the integration of the PFC and LPC stages, an electronic ballast based on the Zeta converter is proposed where the shared switch does not handle the addition of the both stages currents, thus reducing losses and increasing the ballast efficiency. The experimental results validate the proposed configuration, and demonstrate that the proposed electronic ballast is able to provide the desired lamp operation waveforms, while the input current harmonics are in agreement with IEC-61000-3-2 standard. The efficiency of the proposed electronic ballast is around 83% in steady state operation.

Experimental results for this configuration are obtained in [12] for a mains of 220 Vrms / 60 Hz to supply an OSRAM Vialox 70W HPS lamp. The efficiency obtained in that case is 86% employing a COOLMOS SPW17N80C2 in the shared switch. The results show that increasing the input voltage and the output power the efficiency increase. However, the high number of magnetic components of zeta converter penalty the electronic ballast efficiency.

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BIOGRAPHIES

Tiago Bandeira Marchesan was born in Santa Maria, Brazil, in 1980. He received the B.S. in 2003 (with first class honours) and the Ph.D. in 2008, both in electrical engineering from Federal University of Santa Maria, Brazil.

He has been with the electronic Ballast Research Group (GEDRE), as a researcher, since 2000. He is associated professor at the Technology Department of the Regional University of the Northwest of Rio Grande do Sul State.

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Marco A. Dalla Costa was born in Santa Maria, Brazil, in 1978. He received the B.S. and M.Sc. degrees in Electrical Engineering from the Federal University of Santa Maria, Brazil, in 2002 and 2004, and the Ph.D. degree from University of Oviedo, Spain, in 2008.

He is currently a researcher working on the development of electronic systems for lighting and HID lamp modeling. His research interests include dc/dc converters, PFC stages, dimming systems, high-frequency electronic ballasts, discharge lamp modeling, and electronic starters for HID lamps.

J. Marcos Alonso received the M.Sc. degree and Ph.D. both in electrical engineering from the University of Oviedo, Spain, in 1990 and 1994 respectively. From 1990 to 1999 he was assistant professor at the Electrical and Electronic Department of the University of Oviedo, where since 1999 he is an Associate Professor.

Dr. Alonso is the primary author for more than 40 journal and international conference papers in power and industrial electronics, and has co-authored more than 100. His research interests include high-frequency electronic ballasts, discharge lamp modeling, power converters for ozone generation, power converters for electrostatic applications, power factor correction topologies and high frequency switching converters. He was the advisor of four Ph.D. Thesis students in the field of power electronics. He is the holder of four Spanish patents with two under review.

Dr. Alonso was awarded with the Early Career Award of the IEEE Industrial Electronics Society in 2006. He received the second prize paper award of the 2005 IEEE Industry Applications Society Meeting, Production and Application of Light Committee. He was also awarded with the IEEE Industrial Electronics Society Meritorious Paper Award for 1996.

He is an active member of the Institute of Electrical and Electronics Engineers (IEEE), where he usually collaborates as transactions paper reviewer, conference session chairman, among other positions. Since October 2002 he serves as an Associate Editor of the IEEE Transactions on Power Electronics in the field of Lighting Applications. He is also a member of the International Ozone Association (IOA).

Ricardo Nederson do Prado was born in Itapiranga, Brazil, in 1961. He received the B.Sc. degree from the Federal University of Santa Maria, Santa Maria, Brazil, in 1984, and the M.Sc. and Ph.D. degrees from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1987 and 1993, respectively, all in electrical engineering. From 1987 to 1992, he was a Professor in the Electronics Department, Federal University of Minas Gerais, Belo Horizonte, Brazil. Since 1993, he has been with the Federal University of Santa Maria, Brazil, where he is currently an associate Professor in the Electrical Energy Processing Department. From 2005 to 2006, he was with the Fraunhofer Institute, Germany, as a Post doctoral Research Scholar. He is responsible for the Electronic Ballast Research Group (GEDRE). He has co-authored more than 140 technical papers on electronic ballast. His research directions include high-frequency high-density power converters, fluorescent and high pressure lamps, dimming systems, luminous efficiency, electronic ballasts, LED as a source light and power-factor correction.

Dr. Prado is a Founding Member of the Brazilian Power Electronics Society; He is the Member of the Brazilian Automatic Control Society, and several IEEE societies.