ANALYSIS AND DESIGN OF TWO FLYBACK-BASED INTEGRATED CONVERTERS FOR THE IMPLEMENTATION OF LFSW ELECTRONIC BALLASTS

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***Abstract* – This paper presents a simple configuration, based on the integration of two flyback converters, to supply high intensity discharge (HID) lamps with a low frequency square waveform (LFSW), in order to avoid the occurrence of the acoustic resonance (AR) phenomenon. The proposed topology is compared to a previous presented one. Both topologies integrate two flyback converters in different ways. Losses of both integration modes are compared and advantages are discussed in respect to current and voltage components stress. The proposed electronic ballast presents a high efficiency with a reduced number of components and no over current stress in the shared switch. Experimental results validate both configurations.**

***Keywords* – Acoustic resonance, electronic ballasts, HID lamps, integrated converters.**

I. INTRODUCTION

When High Intensity Discharge (HID) lamps are supplied by high frequency sinusoidal current waveforms, they are susceptible to the occurrence of the acoustic resonance (AR) phenomenon [1]. In literature, many works have studied this phenomenon and different methods have been proposed in order to avoid its occurrence [2] - [6].

The option of supplying the lamp with a low frequency square waveform (LFSW) is presented by many researchers as the most reliable technique [7] - [10]. However, the choice for this method demands electronic ballasts with a high number of power stages, increasing cost and decreasing efficiency.

Usually, in this method, three power stages are necessary. The first one, provides the input power factor correction (PFC), the second is the power control (PC) stage, employed to guarantee the stable lamp operation and the last is the inverter stage, used to alternate the lamp current.

The integration of converters has proven to be a good option to reduce the number of stages and components of the ballast, increasing efficiency and decreasing costs, becoming more attractive to the industry [11][12]. However, when two converters are integrated their shared switch is submitted to some extra current or voltage stress.

In this paper, a novel integrated topology is proposed. Two flyback converters employed in the PFC and PC stages of an electronic ballast are integrated in a single one. This topology is compared to a previous presented in [8]. The basic difference between both integrations is that the shared switch of the topology proposed in this paper, is submitted to a voltage stress and in the previous one to extra current. The number of components employed in both topologies is the same and their design is similar. Therefore, the topics to be evaluated are the difference of operation, design, calculation of the shared switch drain to source voltage and rms current, and losses presented in both configurations.

II. INTEGRATED CONFIGURATIONS

The original circuit and both BiFlyback integrated topologies are presented in Figure 1. The previous one, presented in [8] is called BiFlyback Integrated Ballast with Current Stress (BFIB-CS), and the proposed one is BiFlyback Integrated Ballast with Voltage Stress (BFIB-VS). It can be observed, from Figure 1, that both topologies have the same number of components with similar voltage and current characteristics with the exception of the shared switch (S_1) and diodes D_5 and D_6.

In order to understand how the current is distributed among the main switch (S_1) and diodes D_5 and D_6 in both configurations, the equivalent circuits and theoretical waveforms are presented in Figure 2. As can be observed in BFIB-CS, the shared switch (S_1) handles the sum of the currents of both integrated flyback stages. The current through diodes D_5 and D_6 is equal to i_{L1} and iF_{ly_1}, respectively. On the other hand, in BFIB-VS, the shared switch (S_1) only handles the highest current of the two integrated flyback stages in each instant, and diodes D_5 and D_6 only handle the difference between i_{L1} and i_{Fly_1} currents. This is the main difference between both topologies.

III. ANALYSIS OF THE PROPOSED INTEGRATED CIRCUITS

This section presents the theoretical analysis of both integrated circuits, which includes: design equations of the PC and PFC stages, and the analysis of rms current and drain-to-source voltage in the shared switch.

A. Design of the PC and PFC Stages

First of all, the characteristics of the PC stage, performed by the flyback converter, are presented. Some considerations are made, in order to analyze this stage: the former converter (PFC stage) is represented as a DC source, V_B; only one of the secondary windings is taken into account, $L_{Fly\_2\text{-}3}$; the

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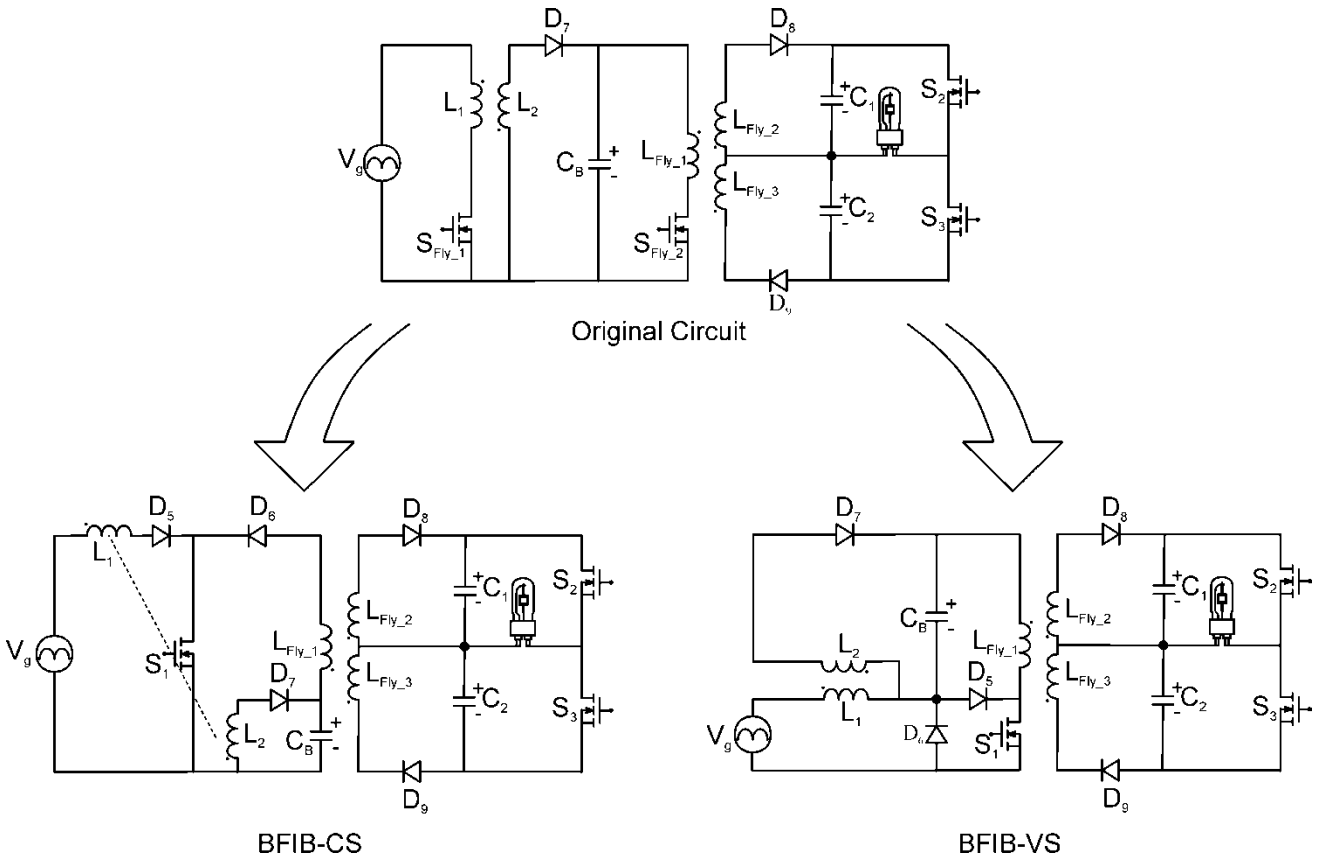


Fig. 1. BiFlyback original circuit and proposed integrated configurations: BFIB-CS and BFIB-VS.

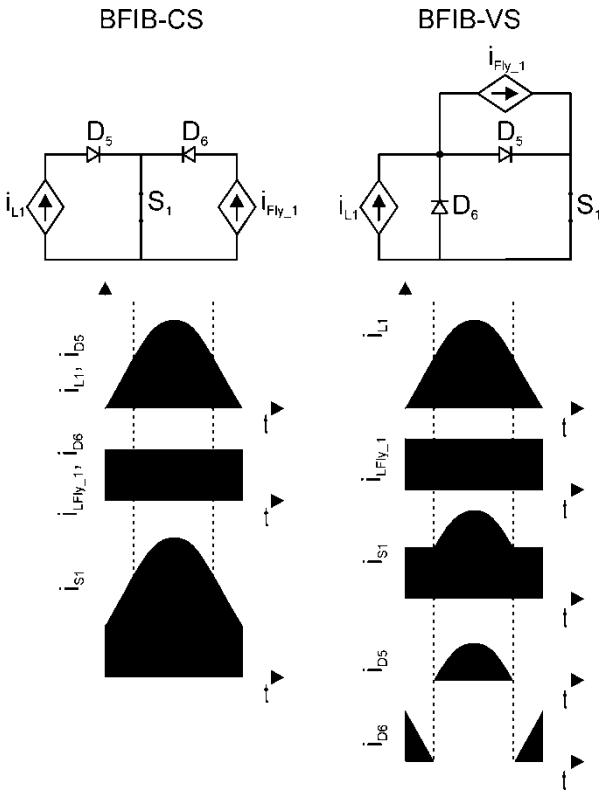


Fig. 2. Equivalent circuit and theoretical waveforms for both configurations.

converter must work in discontinuous conduction mode (DCM); and the lamp is considered as a resistance. Then, the equivalent circuit is shown in Figure 3(a) and the main waveforms of primary and secondary winding currents in Figure 3(b).

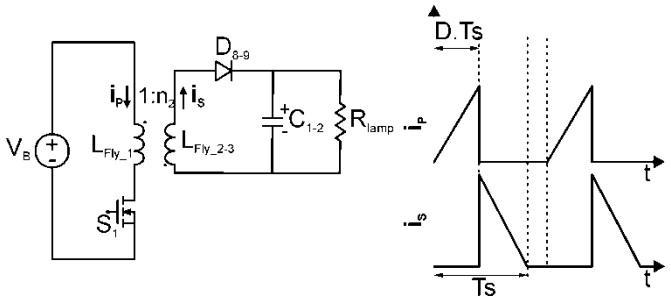
The analysis of the flyback converter supplied from a DC source is already presented in [9]. Therefore, only the relevant equations are presented in this paper. This converter behaves as a resistance working in DCM, R_{Fly}, and its equivalent value is shown in (1). The condition to guarantee the DCM operation is shown in (2).

$$R_{Fly} = \frac{2.L_{Fly\_1}}{D^2.T_S} \tag{1}$$

$$n_2 < \frac{(1-D).V_L}{D.V_B} \tag{2}$$

Where $L_{Fly\_1\ -\ PC}$ flyback primary winding inductance, D – duty cycle, T_S – switching period, n_2 – PC flyback turns ratio, V_L – lamp voltage, and V_B – DC bus voltage.

The PFC stage is also performed by a flyback converter working in DCM. This converter is loaded with the PC stage, which can be represented by its equivalent resistance, R_{Fly}.



a. PC stage – flyback converter supplied from a DC source.

b. Theoretical waveforms.

Fig. 3. PC stage.

The equivalent circuit is presented in Figure 4. The objective of this analysis is: to define the PFC flyback turns ratio in order to guarantee the DCM operation of the converter, n_1; to design the BUS voltage capacitor (C_B) according to a desired voltage ripple; and to define all other ballast components. It is important to emphasize that this analysis is common for both configurations, BFIB-VS and BFIB-CS.

In order to simplify the analysis, the following parameters are defined:

$$m = \frac{V_G}{V_B} \tag{3}$$

$$\alpha = \frac{L_1}{L_{Fly\_1}} \tag{4}$$

Where V_G is the line voltage peak value, and L_1 is the primary winding inductance of the PFC flyback.

The flyback turns ratio, which is designed to the boundary between CCM and DCM operation, is shown below, neglecting the BUS voltage ripple.

$$n_1 = \frac{(1-D)}{D.m} \tag{5}$$

The duty cycle, D, used to calculate n_2 in (2) and n_1 in (5) must be the same, as both flyback converters share the same switch.

As can be seen in Figure 4, the current $i_B(t)$, in the PFC stage, is divided between the BUS capacitor, C_B, and the PC flyback equivalent resistance, R_{Fly}. Then, considering that the AC component of $i_B(t)$ flows only through C_B and that the DC component, I_B, flows only through R_{Fly}, the BUS voltage, V_B, can be defined as:

$$V_B = I_B.R_{Fly} \tag{6}$$

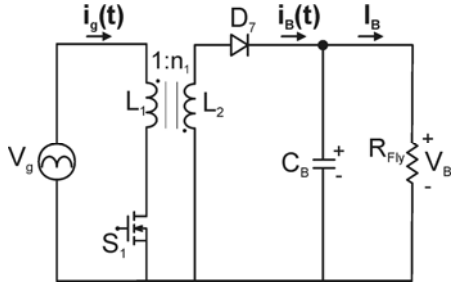


Fig. 4. PFC stage equivalent circuit.

Where,

$$i_B(t) = \frac{V_G.m.D^2.T_S}{2.L_1}.sin^2(\omega.t), \tag{7}$$

$$I_B = \frac{1}{\pi}.\int_0^{\pi} i_B(t).dt = \frac{V_G.m.D^2.T_S}{4.L_1}, \tag{8}$$

ω is the line angular frequency and t the time.

Considering (1), (6) and (8), the voltage ratio, m, is defined in function of the inductance ratio, α, as presented below.

$$m = \sqrt{2.\alpha} \tag{9}$$

Equation (9) is plotted in Figure 5. This graphic allows to define the inductance ratio, α, according to a desired voltage ratio, m. It can be observed that the relation between the bus voltage and the input voltage, m, only depends on the inductance ratio α.

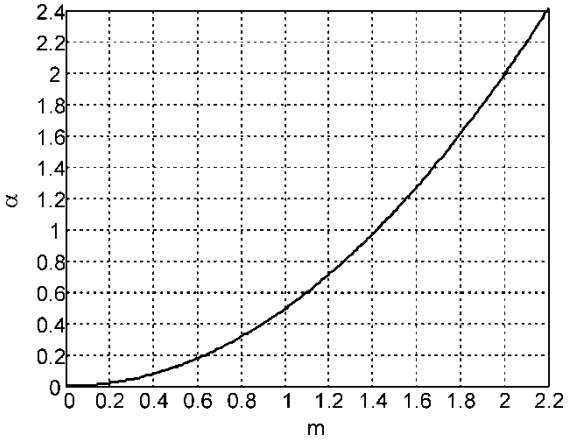


Fig. 5. Inductance ratio α as function of the voltage ratio m.

The equation (10) defines the output power of the analyzed converter, P_{out}. Besides, P_{out} can also be defined as in (11).

$$P_{out} = V_B.I_B \tag{10}$$

$$P_{out} = \frac{P_{lamp}}{\eta} \tag{11}$$

Where P_{lamp} is the lamp power and η the efficiency of the circuit.

Then, using (1), and (10) in (11), a closed equation to calculate L_1 is defined.

$$L_1 = \frac{\eta.V_G.D^2.T_S}{4.P_{lamp}} \tag{12}$$

Another important issue that must be analyzed before a complete design can be performed is the voltage ripple across the bulk capacitor, ΔV_B. The peak-to-peak voltage ripple across the bulk capacitor can be calculated through the charge injected into the capacitor (ΔQ), as follows:

$$\Delta V_B = \frac{\Delta Q}{C_B} = \frac{1}{2.\omega.C_B}.\int_0^{\pi} \left| i_B(t) - I_B \right|.dt \quad (13)$$

The ripple factor is defined in (14). Therefore, the equation that defines the necessary bus capacitance to limit the ripple below to a determined value is shown in (15).

$$v = \frac{\Delta V_B}{V_B} \quad (14)$$

$$C_B = \frac{m^2.D^2}{8.\pi.L_1.f_S.f.v} \quad (15)$$

Where f_S is the switching frequency, and f the line frequency.

B. Voltage and Current in the Shared Switch.

The analysis of maximum drain-to-source voltage and rms current in the shared switch for both circuit configurations is very important, since it is the main difference between the circuits. Besides, this analysis helps to define the suited configuration according to a desired application and, consequently, to choose the appropriate MOSFET to each case. This analysis must be performed for each configuration separately. The theoretical integrated switch current for both analyzed configurations is shown in Figure 6.

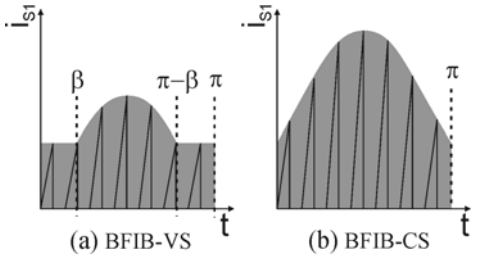


Fig. 6. Integrated switch current waveforms for both configurations (not to horizontal scale).

1) BFIB-VS Analysis - As in this configuration only the highest current between both integrated stages is handled by the shared switch, the current through the main switch, S_1, depends on the conduction angle β, (Figure 6 (a)). During intervals [0,β] and [π-β,π], named PC interval, the switch handles the PC flyback stage current, and during interval [β,π-β], named PFC interval, the switch handles the PFC flyback stage current. The conduction angle, β, depends on the ratio m, defined in (3):

$$\beta = sin^{-1}\left(\frac{m}{2}\right) \quad (16)$$

This β value is in radians. Thus, the following equation represents it in seconds:

$$T_\beta = \frac{\beta}{\omega} \quad (17)$$

Therefore, for m ≤ 2, the rms current through the main switch, I_{rms_VS}, can be defined as:

$$I_{rms\_VS} = \sqrt{\left[\left(I_{PC\_VS}\right)^2 + \left(I_{PFC\_VS}\right)^2\right]} \quad (18)$$

Where I_{PC_VS} is the switch rms current during the PC interval, and I_{PFC_VS} is the switch rms current during the PFC interval, which are defined below:

$$I_{PC\_VS} = \sqrt{\frac{2}{T}.\sum_{n=1}^{NT_{PC}} \int_0^{D.T_S} \left(\frac{V_B.t}{L_{Fly\_1}}\right)^2.dt} \quad (19)$$

$$I_{PFC\_VS} = \sqrt{\frac{2}{T}.\sum_{n=1}^{NT_{PFC}} \int_0^{D.T_S} \left(\frac{V_G.sin\left[2.\pi.f.\left(T_\beta + n.T_S\right)\right].t}{L_1}\right)^2.dt} \quad (20)$$

Where T is the line period,

$$NT_{PC} = \frac{2.T_\beta}{T_S} \quad (21)$$

and

$$NT_{PFC} = \frac{\pi - 2.\beta}{\omega.T_S}. \quad (22)$$

Therefore, solving the integrals and using (12), equations (23) and (24) can be defined:

$$\left(I_{PC\_VS}\right)^2 = \frac{8.NT_{PC}.P_{lamp}{}^2}{3.V_B{}^2.f_S.D.\eta^2} \quad (23)$$

$$\left(I_{PFC\_VS}\right)^2 = \frac{16.P_{lamp}{}^2}{3.V_G{}^2.f_S.D.\eta^2}.\sum_{n=1}^{NT_{PFC}}\left(sin\left[2.\pi.f.\left(T_\beta + n.T_S\right)\right]\right)^2 \quad (24)$$

In the case that m > 2 (V_B<V_β), the PC stage current is always higher than the PFC stage current in steady state. In this case, the main switch handles only the PC stage current, and its value can be defined as:

$$I_{rms\_PC\_VS} = \frac{2.P_{lamp}}{V_B.\eta.\sqrt{3.D}} \quad (25)$$

Another important parameter to be considered is the maximum drain-to-source voltage in the main switch, V_{S_VS}. Thus, neglecting the flyback leakage inductance, this parameter can be defined as:

$$V_{S\_VS} = V_G + V_B + \frac{V_B}{n_1} + \frac{V_L}{n_2} \quad (26)$$

Simplifying this equation:

$$V_{S\_VS} = \frac{V_G + V_B}{1 - D} \quad (27)$$

2) BFIB-CS Analysis - In opposite to the former analysis, the rms current through the main switch does not depend on

any conduction angle (Figure 6 (b)), and can be directly defined as:

$$I_{rms\_CS} = \sqrt{\frac{2}{T}.\left[\sum_{n=1}^{NT}\int_{0}^{D.T_S}\left(\frac{V_B.t}{L_{Fly\_1}} + \frac{V_G.sin\left[2.\pi.f.(n.T_S)\right]t}{L_1}\right)^2.dt\right]} \quad (28)$$

Thus, simplifying the equation, the following expression is obtained:

$$I_{rms\_CS} = \frac{2.P_{lamp}}{V_B.V_G.\eta}.\sqrt{\frac{2}{3.T.f_S.D}.\sum_{n=1}^{NT}\left[V_G + 2.V_B.sin\left(2.\pi.f.n.T_S\right)\right]^2} \quad (29)$$

Where:

$$NT = \frac{T}{T_S} \quad (30)$$

The maximum drain-to-source voltage in the main switch in this case, V_{S_CS}, can be one of the indicated in (31) and (32), whichever is higher. It depends on the projected input and BUS voltage. If $V_G > V_B$ the shared switch voltage is calculated using (31), on the other hand, (32) must be used.

$$V_{S\_CS} = \frac{V_G}{1-D} \quad (31)$$

$$V_{S\_CS} = \frac{V_B}{1-D} \quad (32)$$

3) Shared Switch Design - Considering the previous analysis the abacus of Figure 7 for both configurations (BFIB-VS and BFIB-CS) can be build. This abacus makes possible to design the electronic ballast evaluating the shared switch necessary characteristics for each case.

To build this abacus the following parameters have to be defined: mains – 110 Vrms / 50 Hz; lamp - PHILIPS Master Color CDM-T 35 W, converters switching frequency – 80 kHz and expected electronic ballast efficiency – 90%.

The characteristics of switch voltage and current are plotted in function of V_B and D, which can be chosen according to the desired MOSFET parameters.

IV. PROJECT EXAMPLE

Two Electronic ballasts are projected and implemented for an input voltage of 110 V, 50 Hz, in order to supply a 35 W MH lamp. The ballasts were designed to a bus voltage of 100 V. So, m = 1.55 is calculated in (3), and through the graphic of Figure 5, a relation between the inductances α = 1.2 is obtained. Once the flyback employed in the PC stage is projected according [5], the input flyback can be designed through the α ratio. The considered switching frequency is 80 kHz and the duty cycle for the steady state operation is around 39%. The bus capacitor value is calculated in (15) for a maximum bus voltage ripple of 10%.

The projected values and employed components are presented in table I.

TABLE I
Commercial Components

BFIB-CS and BFIB-VS	
D_5, D_6, D_7, D_8 and D_9	UF4007
C_B	Electrolytic capacitor 150 µF / 160 V
S_1	IRFPE50
S_2 and S_3	IRF840
L_1=L_2	278 µH - 68 winds NEE - 30/15/7 core from Thornton®
L_{Fly_1} L_{Fly_2}= L_{Fly_3}	232 µH - 44 winds 348 µH - 54 winds NEE - 30/15/7 core from Thornton®
C_1=C_2	Polypropylene capacitor 220 nF / 630 V

Through the abacus of Figure 7 the expected peak voltage and rms current across the shared switch can be obtained as shown in Figure 8. However, in the proposed BFIB-VS there is no over current in the shared switch; nevertheless the voltage stress is higher than in the previous presented topology (BFIB-CS).

V. EXPERIMENTAL RESULTS

Experimental results shown in Figure 9 and 10 validate BFIB-VS and BFIB-CS integrations. In Figures 9a, 10a and 9b, 10b the input and output characteristics of both configurations are presented; the measured input power factor was 0.996. In Figure 9c it can be observed that only the highest current between both flyback stages is handled by the shared switch (BFIB-VS) and not the sum of them as shown in Figure 10c (BFIB-CS). The drain-to-source voltage in both topologies is shown in Figures 9d and 10d and is in accordance with the previous calculated values.

Figure 11 shows the measured input current harmonics for BFIB-VS configuration. It is in accordance to the IEC-61000-3-2 standard limits.

It is important to notice that the input current harmonics and, consequently, the input power factor for both configurations are the same, as the difference between the topologies is located in the circuit connection done across the main switch and diodes D_5 and D_6, as explained in section II.

VI. LOSSES ANALYSIS

The main purpose of this section is to compare the losses in the shared switch (S_1) and diodes D_5 and D_6, as there is no losses difference in the other components. The shared switch employed for both topologies are the same (IRFPE50), because the drain-to-source voltage (V_{DS}) for this project presents a difference of 164 V, which is not significant to employ different MOSFETS. Losses are studied through simulation and presented in the graphic of Figure 12. The efficiency obtained through experimental results, for the BFIB-VS configuration is 85% and for the BFIB-CS is 81%.

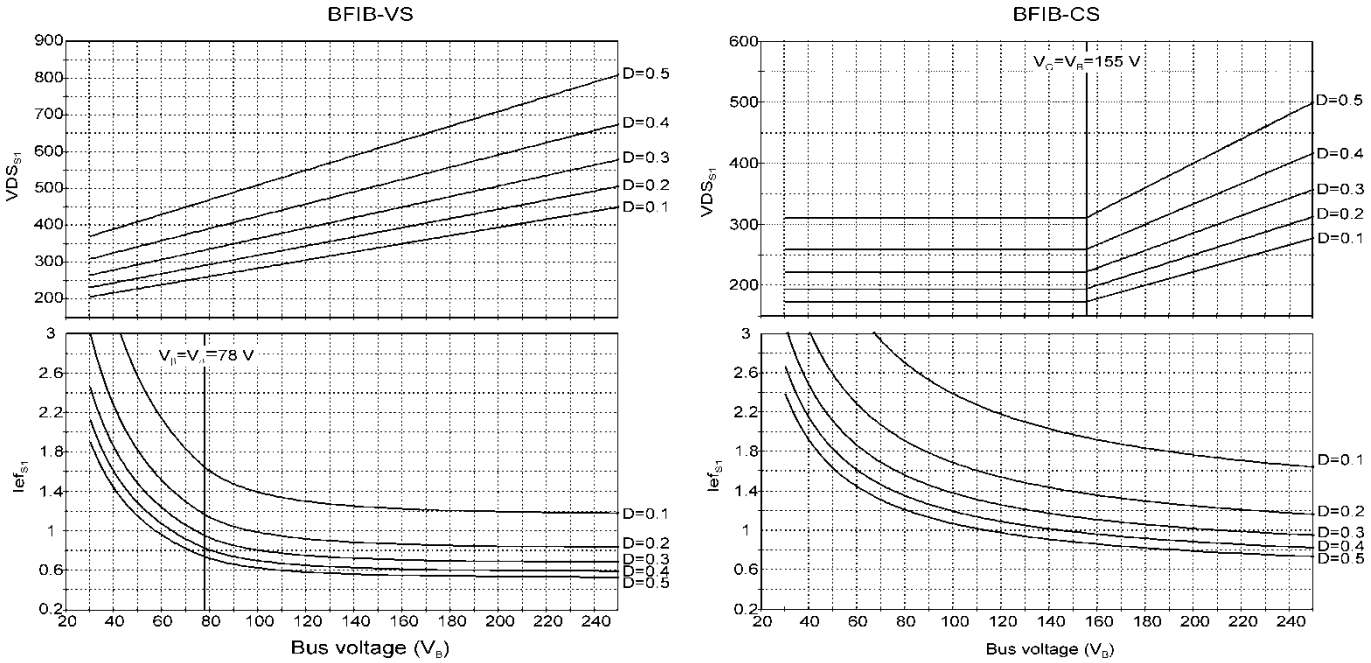


Fig. 7. Integrated switch drain-to-source voltage and rms current characteristic.

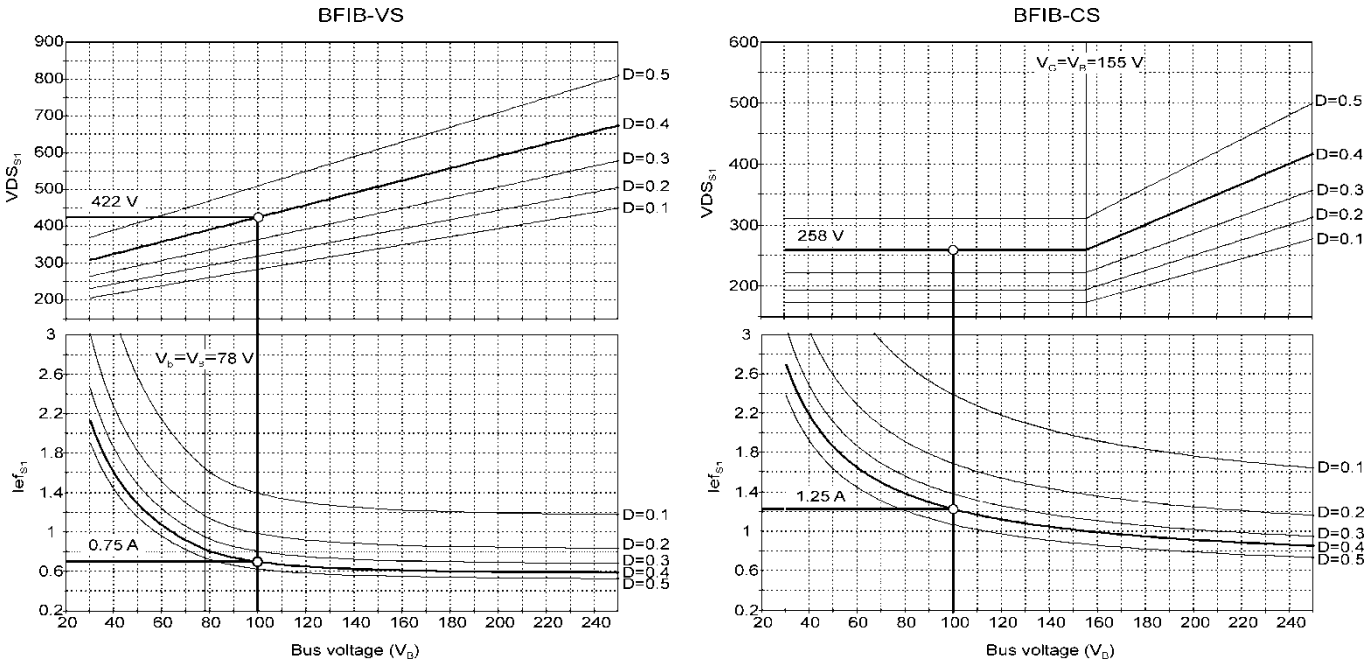


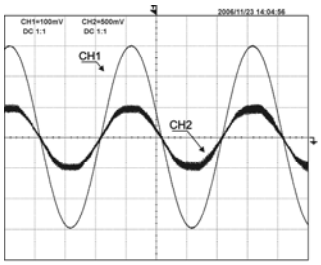
Fig. 8. Defined shared switch drain-to-source voltage and rms current to V_B=100 V and D=0.4.

The lower efficiency of BFIB-CS occurs due to the higher shared switch conduction losses presented by this configuration, as can be seen in Figure 12.

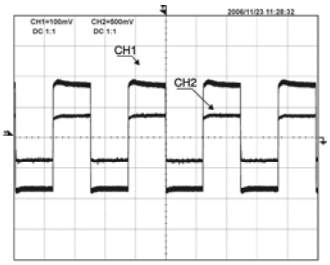
Also, experimental results for both integrations are obtained in [13] for a mains of 220 Vrms / 60 Hz to supply an OSRAM Vialox 70 W HPS lamp. The efficiency obtained in that case for the BFIB-VS configuration is 91.6% and for the BFIB-CS is 84.5% employing a COOLMOS SPW17N80C2 in the shared switch.

The results show that increasing the input voltage and the output power the efficiency of both configurations tends to increase, and, as expected the BFIB-VS efficiency is higher than the BFIB-CS configuration.

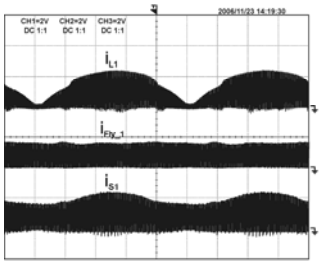
The maximum power that these integrations may provide to the load, in order to supply different lamp wattages, depends on the limits of the flyback converter working on DCM. This issue is being evaluated and will be presented in a future work.



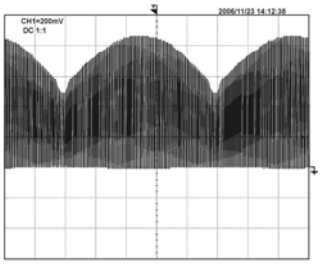
a. Input voltage (CH1-50 V/div) and current (CH2-500 mA/div), 5 ms/div.



b. Lamp voltage (CH1-50 V/div) and current (CH2-500 mA/div), 1 ms/div.

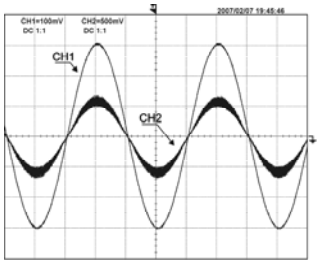


c. Converter currents: PFC stage (i_{L1} – 2 A/div), PC stage (i_{Fly_1} – 2 A/div) and shared switch (i_{S1} – 2 A/div), 2 ms/div.

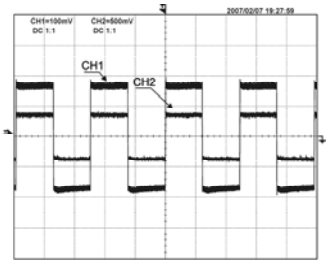


d. Shared switch voltage (CH1-100 V/div), 2 ms/div.

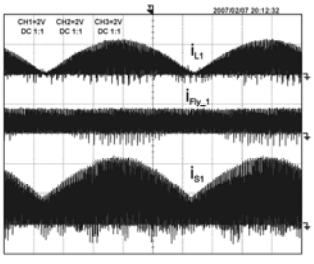
Fig. 9. BFIB-VS experimental results.



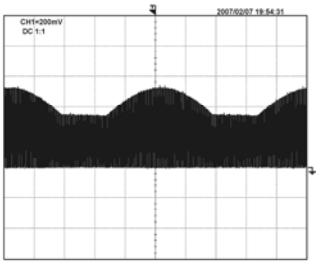
a. Input voltage (CH1-50 V/div) and current (CH2-500 mA/div), 5 ms/div.



b. Lamp voltage (CH1-50 V/div) and current (CH2-500 mA/div), 1 ms/div.



c. Converter currents: PFC stage (i_{L1} – 2 A/div), PC stage (i_{Fly_1} – 2 A/div) and shared switch (i_{S1} – 2 A/div), 2 ms/div.



d. Shared switch voltage (CH1-100 V/div), 2 ms/div.

Fig. 10. BFIB-CS experimental results

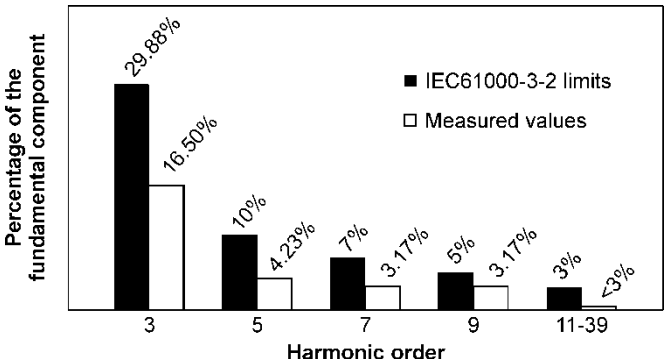


Fig. 11. Measured input current harmonics compared to the IEC61000-3-2 standard limits for the BFIB-VS.

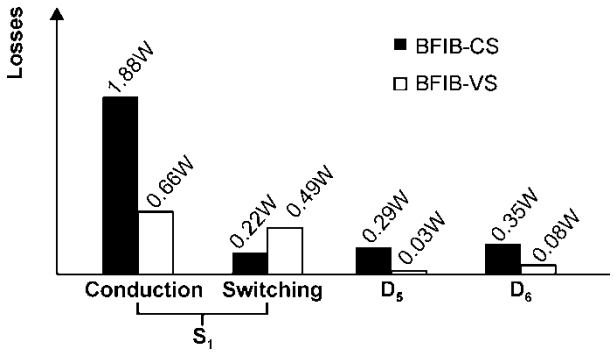


Fig. 12. Comparison between losses in the two electronic ballasts configurations.

VII. CONCLUSION

The proposed BFIB-VS electronic ballast complies with the industry claims on reducing the product final costs, maintaining high efficiency, input power factor correction and the desired lamp operation. Experimental results validate both configurations and losses comparison show that BFIB-VS configuration presents better efficiency than BFIB-CS to supply a 35 W Metal Halide lamp considering an input voltage of 110 Vrms. The main difference between both topology losses takes place in the shared switch (S_1). Although the switching losses for the BFIB-VS are higher, the difference of the conduction losses percentage is considerable, leading to a lower overall efficiency of the BFIB-CS configuration in relation to the proposed one, BFIB-VS.

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