DUAL-OUTPUT DC-DC BUCK CONVERTER

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***Abstract* – This paper presents a single-input double-output synchronous dc-dc buck converter, for applications that demand two dc controlled output voltages. The proposed converter presents a component count reduction and it is considered as a monolithic device with both output voltages generated by the same integrated power converter. Besides the proposal of the suitable power converter, this paper presents its model, control strategy, modulation approach, and design technique. Selected simulated and experimental results are presented as well.**

***Keywords* – Buck converter, Dc-dc converter, Power electronics.**

I. INTRODUCTION

Power electronics can be defined as the study of electronic circuits intended to control the flow of electrical energy. These circuits handle power flow (with the help of switches) at levels much higher than the individual switches ratings. In this context, dc-dc power electronics deal with dc variables at input and output converter sides [1,2].

High-efficiency and high-power density step-down dc-dc converters have been demanded for applications like voltage regulator (VR) in communication power systems [3]. Sometimes, in the standard buck converter, the freewheeling diode is replaced by an active power switch [4–8], which is designed to operate at low output voltage and high efficiency typically required for battery-operated systems [9], this converter is called as synchronous dc-dc buck converter [10]. A detailed comparison between synchronous buck converter and flyback topology is presented in [14], different figures of merit were presented in this study, such as number of elements used, switches stresses, efficiency, stability, transient response and magnetic components. Despite the advantages of the flyback converter, synchronous buck converter uses fewer components and presents higher efficiency. As mentioned in [11], synchronous buck converter is the most popular topology for today's VRs, the use of MOSFET results in tremendous conduction loss reduction.

In many applications is required a dc-dc buck converter with two controlled outputs, such as in systems with on-board distribution schemes where different dc bus voltages have been required, see Figure 1. In this type of system, synchronous buck converters are popular because of their high efficiency and compact size [12]. In [13] was proposed a single-inductor dual output switching converter topology able to independently regulate two output voltages. Besides using only one inductor, the solution presented in [13] employs four power switches. The direct solution for a dc-dc buck converter with two outputs is depicted in Figure 2(a), in which two standard buck converters are employed to control independently two output voltages. As far as this solution replicates the conventional converter, the number of active and passive elements is doubled with respect to the single converter.

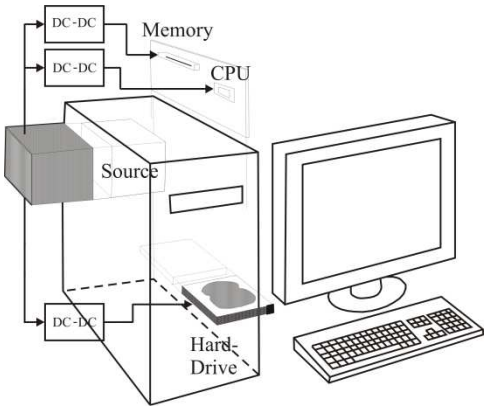

Fig. 1. On-board application with a demand for different dc bus voltages.

This paper presents a single-input double-output synchronous dc-dc buck converter, as observed in Figure 2(b). Notice from this figure that, one power switch is eliminated when compared to the direct solution [see Figure 2(a)]. Besides the proposal of the suitable power converter, this paper presents its model, control strategy, modulation approach, and design technique. Selected simulated and experimental results are presented as well.

II. PROPOSED BUCK CONVERTER

The proposed single-input double-output converter is composed of three power switches S_1, S_2 and S_s and two low-pass filters ($L_1 - C_1$ and $L_2 - C_2$). A binary variable is associated with each switch, i.e., $q_x = 1$ when the power switch S_x is closed, while $q_x = 0$ when the power switch S_x is open, with $x = 1,2,s$. Eight possible switching states could be obtained in the proposed buck converter, since there are three switches with two stages each ($q_x = 1$ and $q_x = 0$).

Many of these switching states are prohibited, as far as it means either a short-circuit of the source or one of the switches would have to absorb (or dissipate) the inductive energy and therefore it may be destroyed. Table I shows all possible states with the indication of prohibited ones, which are marked with "–".The other no-prohibited states (4, 6 and 7) are related to three equivalent circuits (EC-1, EC-2 and EC-3), as observed in Figure 3, which will be described below:

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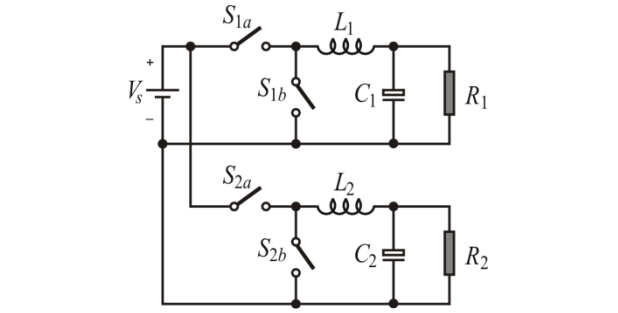
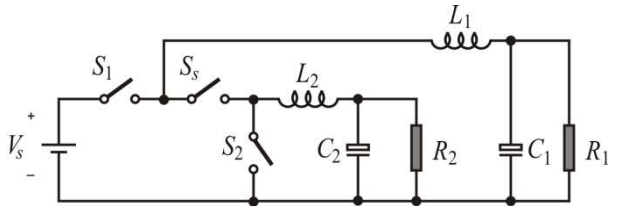


(a)



(b)

Fig. 2. Single-input double-output buck converter: (a) Direct solution and (b) proposed converter.

- During EC-1 [see Figure 3(a) - $q_1 = 1$, $q_s = 1$ and $q_2 = 0$], the input provides energy to both loads as well as to the inductors, in this sense L_1 and L_2 will be charged.
- During EC-2 [see Figure 3(b) - $q_1 = 1$, $q_s = 0$ and $q_2 = 1$], the input provides energy to R_1-L_1 and current i_{L2} flows through S_2, transferring some of its stored energy to the load R_2. In this case, L_1 will be charged and L_2 will be discharged.
- During EC-3 [see Figure 3(c) - $q_1 = 0$, $q_s = 1$ and $q_2 = 1$], the current i_{L1} flows through S_s and S_2, while i_{L2} flows through S_2 transferring part of its stored energy to the load R_1 and R_2, respectively. In this case both inductors will be discharged.

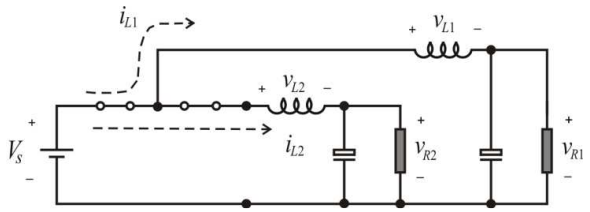
Notice from EC-2 [Figure 3(b)] that the time related to energy transfer from source to R_1-L_1 is always higher than the time related to energy transfer from source to R_2-L_2. In other words, it is not possible to charge L_2 without charging L_1, which means a direct impact in terms of the output voltages, i.e., $V_{R1} \geq V_{R2}$. Observe that State 3 generates the same equivalent circuit of that obtained in State 4, when $i_{L1} > 0$, but is represents a prohibited state if a bi-directional power flow is an important aspect to be considered.

III. STEADY-STATE ANALYSIS

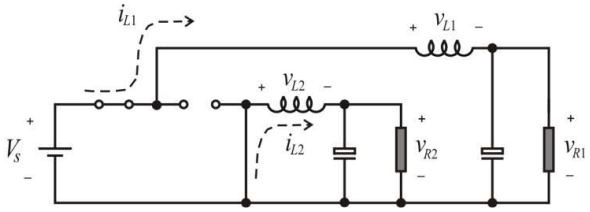
Normally in applications of dc-dc converters, it is required a nearly constant instantaneous output voltage, i.e., $v_{R1} \approx V_{R1}$ and $v_{R2} \approx V_{R2}$. To simplify the analysis, the capacitor filter at output converter side is assumed to be very large. In this case, and considering the continuous-conduction mode, it is possible to depict the inductors waveforms associated to each equivalent circuit (EC-1, EC-2 and EC-3), as observed in Figure 4. From this figure, it is possible to notice that switch S_1 (t_{on1}) will deal with the control of V_{R1}, while S_2 (t_{on2}) will handle the control of V_{R2}. On the other hand, switch S_s must be controlled to avoid the prohibited states (see table I).

TABLE I
EQUIVALENT CIRCUITS OBTAINED WITH THE STATE OF THE SWITCHES.

States	q_1	q_2	q_s	Equivalent Circuits (EC)
1	0	0	0	-
2	0	0	1	-
3	0	1	0	-
4	0	1	1	EC-3
5	1	0	0	-
6	1	0	1	EC-2
7	1	1	0	EC-1
8	1	1	1	-



(a)



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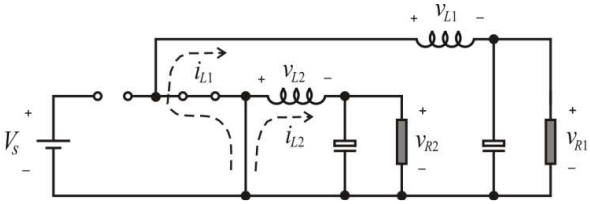


(c)

Fig. 3. Equivalent circuits (EC) of the proposed converter in different switching states: (a) EC-1, (b) EC-2 and (c) EC-3.

Since in steady-state operation the waveforms must repeat from one time period (T_s) to the next one, as well as the passive element characteristic of the inductors, the integral of the inductor voltages v_{L1} and v_{L2} over one time period must be zero, which means

$$\int_0^{T_s} v_{L1}\, dt = 0 \tag{1}$$

$$(V_S - V_{R1})t_{on1} = V_{R1}(T_s - t_{on1}) \tag{2}$$

and

$$\int_0^{T_s} v_{L2}\, dt = 0 \tag{3}$$

$$(V_S - V_{R2})(T_s - t_{on2}) = V_{R1} t_{on2} \tag{4}$$

developing these equations, it yields

$$V_{R1} = D_1 V_s \tag{5}$$

$$V_{R2} = (1 - D_2) V_s \tag{6}$$

where $D_1 = t_{on1}/T_s$ and $D_2 = t_{on2}/T_s$. In the continuous conduction mode, the output voltage V_{R1} varies linearly with the duty ratio of the switch S_1, while the output V_{R2} varies linearly with $1 - D_2$, or $V_{R2} = D_2' V_s$ where $D_2' = 1 - D_2$.

IV. MODULATION STRATEGY

As described before the switches S_1 and S_2 will control the voltages v_{R1} and v_{R2}, respectively. The gating signal of the switch S_s must be obtained to avoid the prohibited states presented in Table I. The modulation strategy presented in Figure 5(a) deals with these constraints.

Notice that both gating signals of switches S_1 and S_2 are obtained directly from the comparison of V_{R1}^* and V_{R2}^* with the saw-tooth, as observed in Figure 5(b). The other switch S_s must be turned on when either S_1 or S_2 is open and must be turned off when both S_1 and S_2 are closed to avoid short-circuit of the source. To do so, an "exclusive or" logic (XOR) can be used, as in Figure 5(c).

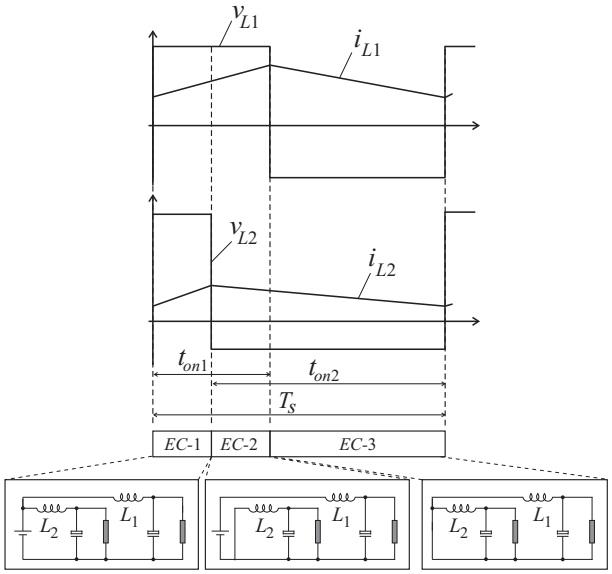


Fig. 4. Voltages and currents of the inductors associated with equivalents circuits.

V. STATE-SPACE AVERAGING AND BLOCK DIAGRAM MODEL

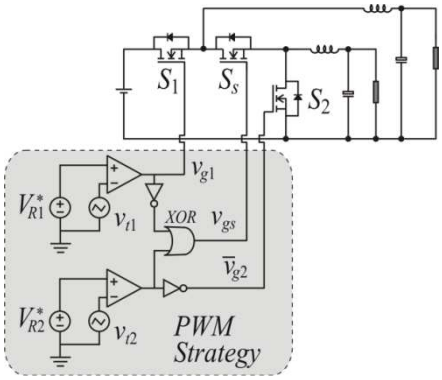
The state-space averaging model describing the voltage and current dynamics is given by (7) – (10)

$$L_1 \frac{di_{L1}}{dt} + v_{R1} = D_1 v_s \tag{7}$$

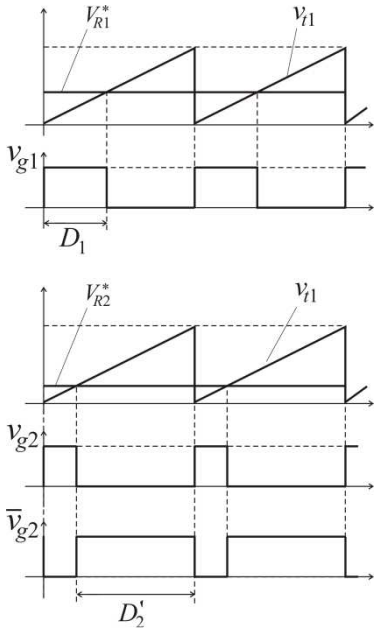
$$C_1 \frac{dv_{R1}}{dt} = i_{L1} - \frac{v_{R1}}{R_1} \tag{8}$$

$$L_2 \frac{di_{L2}}{dt} + v_{R2} = D_2' v_s \tag{9}$$

$$C_2 \frac{dv_{R2}}{dt} = i_{L2} - \frac{v_{R2}}{R_2} \tag{10}$$



(a)



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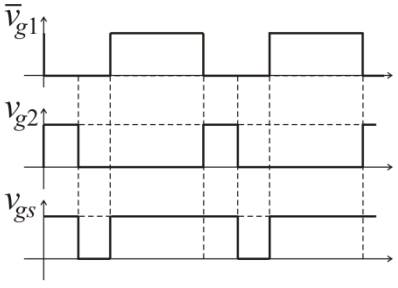
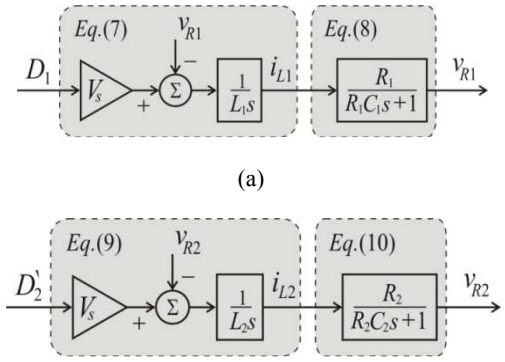


(c)

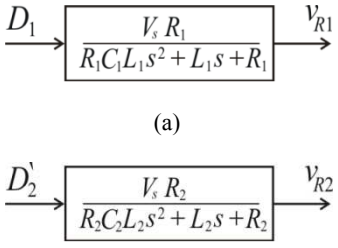
Fig. 5. (a) PWM approach. (b) Gating signal waveforms generation for switches S_1 and S_2. (c) Gating signal waveforms generation for switch S_s.



(a)

(b)

Fig. 6. Block diagram of the proposed system: (a) equations (7)-(8), (b) equations (9)-(10).



(a)

(b)

Fig. 7. Simplified block diagram of the proposed system: (a) output voltage 1, (b) output voltage 2.

The model is reasonably accurate for large-signal analysis under the continuous-conduction mode. From equations (7)-(10) it is possible to determine the block diagram of the single-input double-output buck converter, as observed in Figure 6. A simplified block diagram can be obtained from Figure 6, as observed in Figure 7. The block diagram presented in Figure 6 is useful for dual-loop control technique with the inner-inductor-current loop, since the inductor current is available.

To validate this model, a simulation in s-domain using *SIMULINK* software has been evaluated and compared with a dynamic simulation using PSIM. As observed in Figure 8, the waveforms obtained from both steady-state and dynamic simulations match completely. The simulation parameters used in these tests were: *i*) $V_s = 100V$, *ii*) $L_1 = L_2 = 1mH$, *iii*) $C_1 = C_2 = 120\mu F$, *iv*) $R_1 = R_2 = 10\Omega$ and *v*) $D_1 = 0.4$ and $D_2 = 0.2$.

VI. CONTROL STRATEGY

Normally, in a conventional dc-dc buck converter, either a *P* (proportional) or a *PI* (proportional plus integral) controllers are used to control the output voltage, since this kind of plant can be considered as a highly underdamped system. In this way, derivative actions are seldom used to avoid the differentiation of the switching actions. Fast speed of response can be obtained in sacrificing the steady-state errors when the *P* controller is used. On the other hand, steady-state errors can be removed with a *PI* controller,

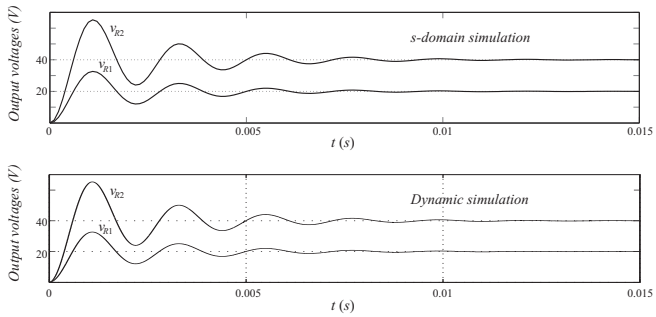
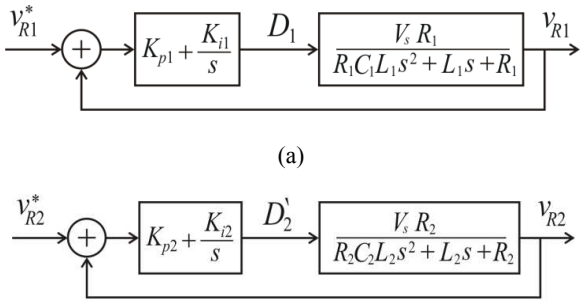


Fig. 8. Comparison of the step response for steady state (top) and dynamic simulation (bottom).



(a)

(b)

Fig. 9. Control block diagrams. Control of: (a) output 1, (b) output 2.

besides the slower response. In this text a *PI* controller has been used, since it turns out that there is no pole placed in zero for both transfer functions (block diagrams - see Figure 7), which means that a simple *P* controller cannot be used to guarantee zero steady-state error.

The control strategy applied to single-input double-output dc-dc converter must guarantee two controlled output voltages to desired levels, though the input voltage (V_s) and the output loads (R_1 and R_2) may fluctuate. As done in a conventional dc-dc converter [12], each output load of the proposed converter can be controlled by using either a simple single-loop voltage-mode control or a dual-loop control technique with the inner-inductor-current loop and the output-voltage loop. Due to simplicity the first approach will be considered, i.e., simple single-loop voltage-mode control. The control block diagrams with a *PI* controller are presented in Figure 9.

The transfer function of the *PI* controller can be written as

$$C(s) = K_{p\delta}\left(\frac{s+1/T_{i\delta}}{s}\right) \tag{11}$$

where δ=1,2 and $T_{i\delta} = K_{p\delta}/K_{i\delta}$.

The problem of setting the *PI* controller parameters of a second-order system can then be stated as follows: find a gain $K_{p\delta}$ and place the zero $-1/T_{i\delta}$ such that the feedback system satisfies some transient performance specification. The solution to this problem can be found with the help of the root-locus diagrams of Figure 10 for three different cases.

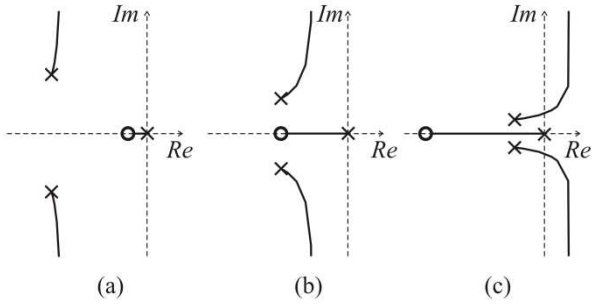


Fig. 10. Root-locus diagram for the design of *PI* controller: (a) case 1, (b) case 2, (c) case 3.

Three cases will be considered in terms of the zero's position of the controller $(-1/T_{i\delta})$:

- *Case* 1: When the zero of the controller $(-1/T_{i\delta})$ is placed between the origin and the real part of the plant double poles $-1/(2R_1C_1)$, i.e., $T_{i\delta} > 2R_1C_1$, the root-locus diagram with a *PI* controller is showed in Figure 10(a).
- *Case* 2: If the zero of the controller $(-1/T_{i\delta})$ is placed over the real part of the double poles i.e., $T_{i\delta} = 2R_1C_1$, the root-locus diagram is showed in Figure 10(b).
- *Case* 3: When the zero of the controller $(-1/T_{i\delta})$ is placed on the left side of the real part of the double poles, i.e., $T_{i\delta} < 2R_1C_1$, the system is stable for small values of $K_{p\delta}$ and instable for big values of $K_{p\delta}$, which could be undesirable.

Among the three cases presented before, the Case 2 will be employed in this work due to its interesting characteristics compared to the other ones, i.e., the step response of the closed-loop system may be monotonic or underdamped and there is no instability problem. In this sense, $K_{p\delta}$ can be set in such a way that the step response of the closed-loop system may be obtained without overshoot, as observed in Figure 11. The same behavior is obtained to both outputs v_{R1} and v_{R2}.

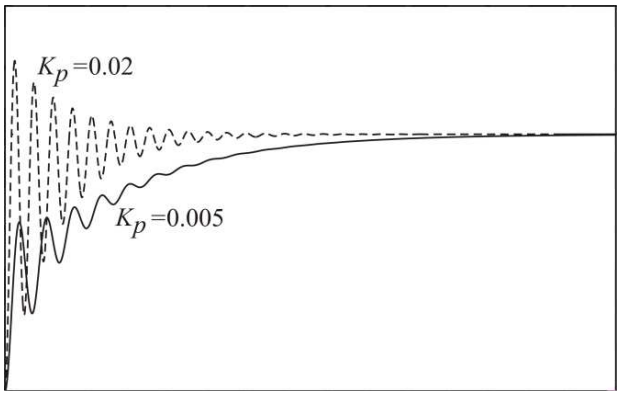


Fig. 11. Step response of the output voltage (v_{R1}) for the closed-loop system with K_I set as in case 2 and considering low values of K_P.

VII. DESIGN OF PASSIVE ELEMENTS

The proposed dual-output buck converter has been designed for continuous conduction mode. Some assumptions will be taken into account in the specification and design of passive elements, such as: all ripple component in $i_{L\delta}$ (δ=1,2) flows through the capacitors and average value of the currents go to loads.

A. Design of L_1 and C_1

Considering Figure 12(a) and the equation that governs the relationship between voltage and current in the inductor L_1, it is possible to write

$$v_{L1} = L_1 \frac{di_{L1}}{dt} \tag{11}$$

$$v_{L1} \approx L_1 \frac{\Delta i_{L1}}{\Delta t} \tag{12}$$

$$L_1 \approx \frac{v_{L1}\Delta t}{\Delta i_{L1}} \tag{13}$$

Applying (13) during $\Delta t = (1 - D_1)T_s$, means that

$$L_1 \approx \frac{V_{R1}}{\Delta i_{L1}}(1 - D_1)T_s \tag{14}$$

Figure 12(b) shows the values of L_1 in *mH* as a function of inductor current ripple Δi_{L1} for different values of switching frequency ($f_s = 1/T_s$). As expected, as far as the low values of ripples are demanded, higher values of inductors must be used or increasing in frequency is necessary.

The interval of time related to the capacitor charge is highlighted in Figure 13(a), i.e., when i_{C1} is positive in $T_S/2$. The amount of charge (ΔQ) stored by the capacitor C_1 is given by:

$$\Delta Q = C_1 \Delta V_{C1} \tag{15}$$

or

$$C_1 = \Delta Q/\Delta V_{C1} \tag{16}$$

$$C_1 = \frac{\Delta i_{C1} T_s}{8\Delta V_{C1}} \tag{17}$$

this equation was obtained using the same approach employed in [15] for conventional solution. Considering that $\Delta i_{C1} \approx \Delta i_{L1}$, it means that the capacitance C_1 could be obtained in terms of desired output voltage ripple and inductor current ripple, as in (18)

$$C_1 \approx \frac{\Delta i_{L1} T_s}{8\Delta V_{C1}} \tag{18}$$

Figure 13(b) shows the values of C_1 in μF as a function of capacitor voltage ripple Δv_{C1} for different values of switching frequency ($f_s = 1/T_s$). As expected, as far as the low values of ripples are demanded, higher values of capacitors must be used.

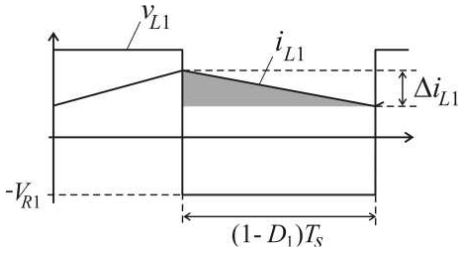
B. Design of L_2 and C_2

Following the same approach as employed for L_1 and C_1 it is possible to obtain:

$$L_2 \approx \frac{V_{R2}}{\Delta i_{L2}}(D_2')T_s \tag{19}$$

$$C_2 \approx \frac{\Delta i_{L2} T_s}{8\Delta V_{C2}} \tag{20}$$

The inductor and capacitor voltages obtained in Figs. 12(b) and 13(b) are valid for L_2 and C_2.



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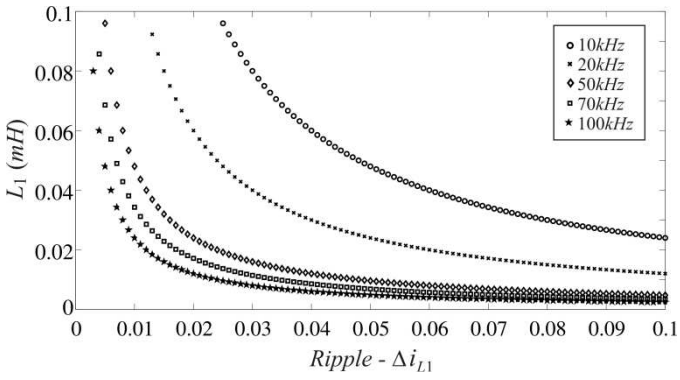

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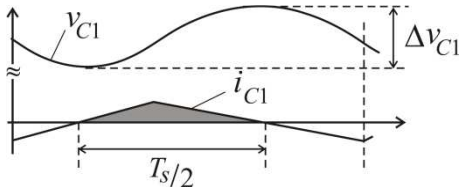
Fig. 12. (a) Variables associated with L_1 for design purposes. (b) Inductor value versus current ripple Δi_{L1}.



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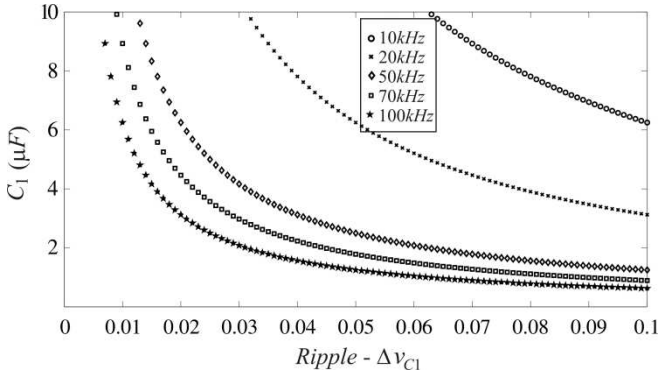


(b)

Fig. 13. (a) Variables associated with C_1 for design purposes. (b) Capacitor value versus current ripple Δv_{C1}.

VIII. COMPARISON WITH CONVENTIONAL SOLUTION

In this section will be presented a comparison in terms of the current rating of the switches used in both solutions, i.e., the proposed power converter with dual-output [Figure 2(b)] and that one considered as the conventional solution, as in Figure 2(a).

A direct comparison of those circuits reveals a reduction of one power switch as an advantage for the proposed converter, as well as the reduction of its drive circuitry to generate the gating signal. On the other hand, two power switches in the proposed solution must be redesigned in terms of current ratings, as observed in Table II, where t_δ is the time when the S_s is open (EC-2). In this table is presented the instantaneous values of current through each power switch as a function of the time in which the switches are conducting. Notice that, during EC-1 and EC-3 the switches S_1 and S_2 will deal with $i_{L1} + i_{L2}$, instead of i_{L1} or i_{L2} in the conventional solution.

The comparison in terms of losses in the power switches was also considered for both conventional and proposed converters showed in Figure 2. The evaluation of the converter losses is obtained through regression model presented in [16]. The switch loss model includes: a) IGBT and diode conduction losses, b) IGBT turn-on losses, c) IGBT turn-off losses, and d) diode turn-off energy. The same parameters employed in the simulated results (Section IX) were considered in the following results.

Figure 14(a) - left side - shows the conduction losses in the switches of the conventional converter, while Figure 14(a) - right side - shows the conduction losses in the diodes of the conventional converter. Figure 14(b) - left side - shows the conduction losses in the switches of the proposed converter, while Figure 14(b) - right side - shows the conduction losses in the diodes of the proposed converter. Figure 14(c) - left side - shows the switching losses in the switches of the conventional converter, while Figure 14(c) - right side - shows the switching losses in the diodes of the conventional converter. Figure 14(d) - left side - shows the switching losses in the switches of the proposed converter, while Figure 14(d) - right side - shows the switching losses in the diodes of the proposed converter. The proposed converter presents a reduction of 15% of the total losses compared to the conventional solution.

TABLE II
CURRENT RATINGS OF THE SWITCHES.

Proposed Converter	Conventional Converter
$i_{S1}(t_{on1} - t_\delta) = i_{L1} + i_{L2}$	$i_{S1a}(t_{on1}) = i_{L1}$
$i_{Ss}(t_{on1} - t_\delta) = i_{L2}$	$i_{S1b}(t_{on1}) = 0$
$i_{S2}(t_{on1} - t_\delta) = 0$	$i_{S1a}(T_s - t_{on1}) = 0$
	$i_{S1b}(T_s - t_{on1}) = -i_{L1}$
$i_{S1}(t_\delta) = i_{L1}$	
$i_{Ss}(t_\delta) = 0$	$i_{S2a}(t_{on2}) = i_{L2}$
$i_{S2}(t_\delta) = -i_{L2}$	$i_{S2b}(t_{on2}) = 0$
	$i_{S2a}(T_s - t_{on2}) = 0$
$i_{S1}(t_{on2} - t_\delta) = 0$	$i_{S2b}(T_s - t_{on2}) = -i_{L2}$
$i_{Ss}(t_{on2} - t_\delta) = -i_{L1}$	
$i_{S2}(t_{on2} - t_\delta) = -(i_{L1} + i_{L2})$	

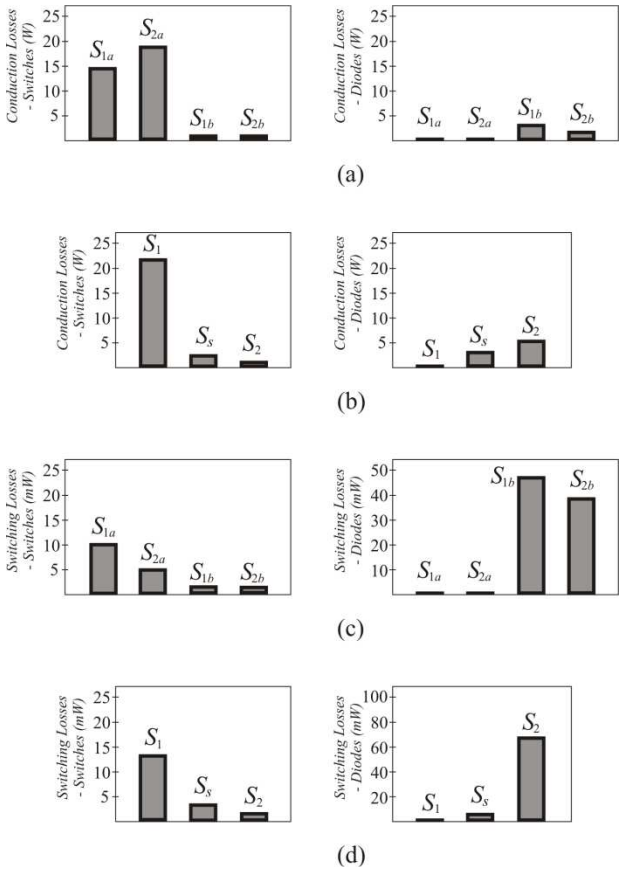


Fig. 14. (a) Conduction losses in the conventional converter: (left) losses in the switches and (right) losses in the diodes. (b) Conduction losses in the proposed converter: (left) losses in the switches and (right) losses in the diodes. (c) Switching losses in the conventional converter: (left) losses in the switches and (right) losses in the diodes. (d) Switching losses in the proposed converter: (left) losses in the switches and (right) losses in the diodes.

IX. SIMULATED AND EXPERIMENTAL RESULTS

The proposed converter has been implemented by dynamic simulation with PSIM software and in the laboratory. Steady-state and transient operation modes have been considered in the selected tests.

Two sets of simulated outcomes will be considered with the converter operating by using different parameters, i.e., the first set (presented in Figures 15 and 16) is obtained with: *i*) $V_s = 100V$, *ii*) $L_1 = L_2 = 1mH$, *iii*) $C_1 = C_2 = 120\mu F$, *iv*) $R_1 = R_2 = 10\Omega$, *v*) $f_s = 50KHz$ and *vi*) $V_{R1}^* = 40V$ and $V_{R2}^* = 20V$. On the other hand, the second set of results employs the following parameters: *i*) $V_s = 100V$, *ii*) $L_1 = L_2 = 2mH$, *iii*) $C_1 = C_2 = 2200\mu F$, *iv*) $R_1 = R_2 = 19.5\Omega$ and *v*) $D_1 = 0.4$ and $D_2 = 0.2$ (presented in Figs. 16 and 17).

Figure 15(a) shows the gating signals of the switches S_1, S_s and S_2, respectively. These simulated results follow the discussion presented in Section IV (Modulation Strategy). Figure 15(b) depicts the variables associated to each inductor of the proposed converter, which matches completely with the theoretical expectation presented in Section III (Steady-state Analysis). Figure 15(c) shows the control goal of the proposed converter including the start-up time. The design of the *PI* controllers is done as in Section VI (Control Strategy – see Figure 11). Comparing Figure 15(c) with Figure 11, it is possible to realize that the dynamic simulation results [Figure 15(c)] are quite similar to those ones obtained with steady-state simulation (Figure 11) for $K_P = 0.005$.

Figure 16 shows the behavior of the main variables of the converter under two hard transients, i.e., the first one at $t = 0.1s$ with a step transient in V_s from $100V$ to $120V$, and the other one at $t = 0.15s$ with a step transient in the value of R_1 from 10Ω to 5Ω.

Figures 17 and 18 show the comparison of simulated and experimental results for the second set of the outcomes. Notice that, both simulated and experimental results are quite close.

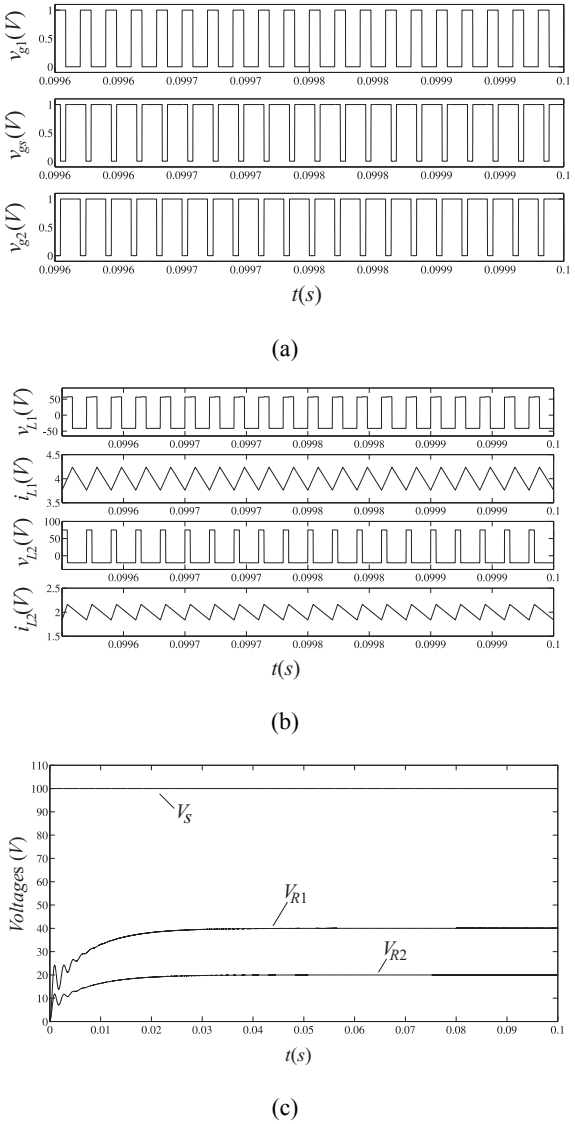


Fig. 15. Simulation results: (a) Gating signals of the switches, (b) variables associated to each inductor, and (c) input and output voltages.

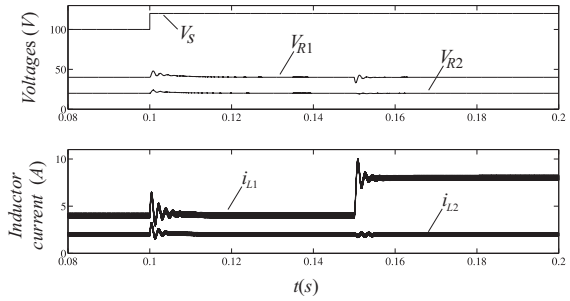
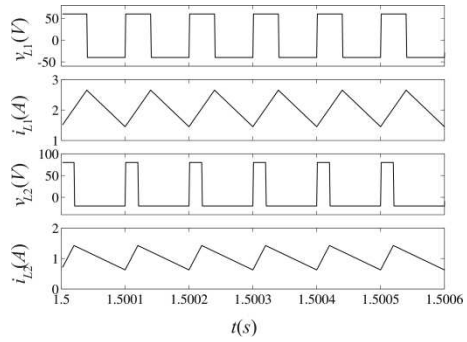
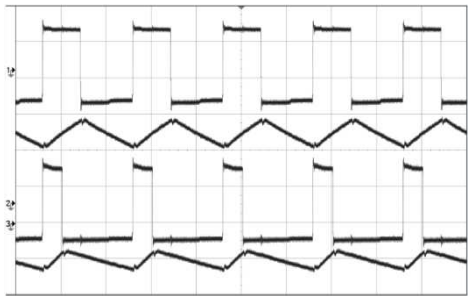


Fig. 16. Simulation results: (top) step transient in the voltage source, (bottom) step transient in the load R_1.



(a)

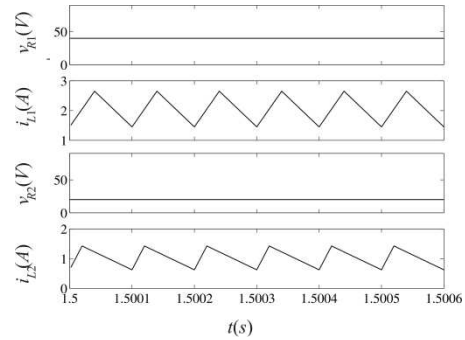


(b)

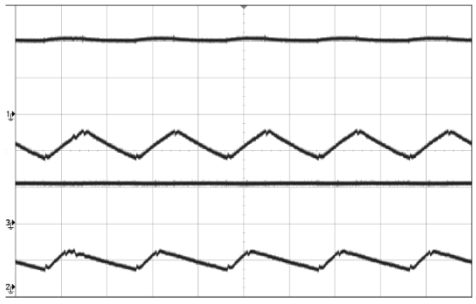
Fig. 17. Comparison of (a) simulation and (b) experimental results showing the variables of the inductors, (from top to bottom) v_{L1}, i_{L1}, v_{L2} and i_{L2} ($50V/div$ and $1A/div$).

X. CONCLUSION

This paper presented a dual-output dc-dc buck converter to be applied in single-input double-output synchronous dc-dc buck converter systems. Besides the proposal of the suitable power converter, this paper presents its model, control strategy, modulation approach, and design technique. As advantage of this converter, it is possible to sort: a single integrated converter with two outputs and elimination of one power switch and its drive circuitry. As disadvantage, the dual-output dc-dc buck converter needs power switches with current ratings higher than that observed in the conventional solution. Selected simulated and experimental results are presented to demonstrate the feasibility of the converter.



(a)



(b)

Fig. 18. Comparison of (a) simulation and (b) experimental results showing the output voltages and inductor currents, (from top to bottom) v_{L1}, i_{L1}, v_{L2} and i_{L2} ($20V/div$ and $500mA/div$).

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BIOGRAPHY

Euzeli Cipriano dos Santos Junior received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Federal University of Campina Grande, Campina Grande, Brazil, in 2004, 2005, and 2007, respectively. From 2006 to 2007, he was a Visiting Scholar with Electric Machines and Power Electronics Laboratory, Texas A&M University, College Station. From August 2006 to March 2009, he was a Professor at the Federal Center of Technological Education of Paraiba, Brazil. From December 2010 to March 2011, he was a Visiting Professor at the University of Siegen, Germany, sponsored by DAAD/CAPES. Since March 2009, he has been with the Department of Electrical Engineering, Federal University of Campina Grande, where he is currently Professor of Electrical Engineering. His research interests include power electronics and electrical drives.