SINGLE-STAGE CHARGE-PUMP VOLTAGE-SOURCE ELECTRONIC BALLAST FOR A 70 W HPS LAMP

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***Abstract* – In this paper a single-stage charge-pump voltage-source electronic ballast for a 70 W High Pressure Sodium [HPS] lamp is proposed. Although charge-pump ballasts have already been studied in fluorescent lamp applications, for HPS lamps this topology represents a new research topic. The proposed topology is a combination of a double charge-pump and a half-bridge inverter which share the same switches operating complementary. A microprocessor is used to generate the switching frequency, drive the ballast and to supervise and control the power at the lamp. The proposed ballast presents high power factor and energy efficiency, which is improved by the zero-voltage switching technique. Experimental results obtained on a 70 W high-pressure sodium lamp are discussed.**

***Keywords* – electronic ballast, high-pressure sodium lamp, Power Factor Correction - PFC.**

I. INTRODUCTION

High pressure sodium lamps cannot be connected directly to the utility line. Since they have a negative impedance characteristic in the desired operating region, these lamps require a ballast which provides a high voltage pulse to start-up and another voltage level to operate at. Moreover, the ballast needs to limit the lamp current to prevent its destruction.

Usually electromagnetic ballasts are applied to these lamps but they have some limitations like large size and weight, poor regulation, low power factor [1] and the stroboscopic effect, besides requiring an auxiliary circuit to generate the high voltage start-up pulse.

In order to obtain a compact electronic ballast and eliminate the stroboscopic effect and audible noise, the operating frequency must be raised [2]. Smaller magnetic components are used in this condition which reduces weight and size and the start-up circuit can be inserted into the topology. The main drawback of electronic ballasts is their initial cost with respect to magnetic ballasts, although the energy saving achieved with electronic ballasts make them more economic in the long run [1]. In the case of HPS lamps the energy may be saved considering the possibility of the electronic ballast to dimmer the lamp.

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The high-frequency electronic ballasts convert the utility line voltage and frequency into a high-frequency output voltage [3]. Usually they have two stages. The first stage consists of a full-bridge diode rectifier and a power factor correction [PFC] stage. The full-bridge diode rectifier without PFC will drain current with significant harmonics and, therefore, the electronic ballast will operate at a poor power factor. In order to provide a high power factor and generate a dc-link voltage, which is used in the second stage to generate a high frequency ac-voltage, a PFC circuit can be applied. This circuit can be a discontinuous current mode boost whose line current naturally follows the sinusoidal line voltage waveform. However, these two stages increase the cost and the number of components, reducing the efficiency of the electronic ballast. Besides, four power semiconductors devices are conducting current simultaneously. A smaller number of these devices are more desirable in terms of efficiency, reliability, and cost [2], [3].

To avoid these problems, single-stage topologies are more desirable and have been developed in [1-12]. In a single-stage topology, high power factor can be obtained by combining the PFC stage and the inverter stage into a single one with internal low frequency storage. The way to do this is to allow the two stages to share switches in order to simplify the circuit [1]. In this paper, a single-stage PFC ballast is presented and analyzed [13]. The presented electronic ballast employs a different charge-pump topology to correct the power factor. The main contribution of this paper is the use of charge-pump converters for HPS lamp electronic ballasts. This technology was first applied to fluorescent lamp ballasts but its use in HPS lamp electronic ballasts is a recent research topic. This PFC topology is a double charge-pump operating with two complementary switches and limiting input current inductors. This combination duplicates the input current frequency, reducing the magnetic components of the high frequency input filter. Charge-pump capacitors are on the input side and they are also used as a high frequency input filter. The switches are used by the half-bridge inverter. This inverter generates a square wave to supply the lamp located in a LC series resonant filter. The series resonant capacitor is used to eliminate the dc voltage level at the lamp and the series resonant inductor is used to limit the current through the lamp. The advantages of this ballast are that there are only three power semiconductor devices connected in the path from utility line to the ballast output and that all of the switches operate under the same conditions. In the other ballasts, one switch is demanded of more than the others for correcting the power factor [1], [4-8].

The proposed topology operates in steady state with a constant duty cycle D = 0.5 and controlled frequency. Soft-switching is necessary to reduce the power losses due to switching and to improve energy efficiency.

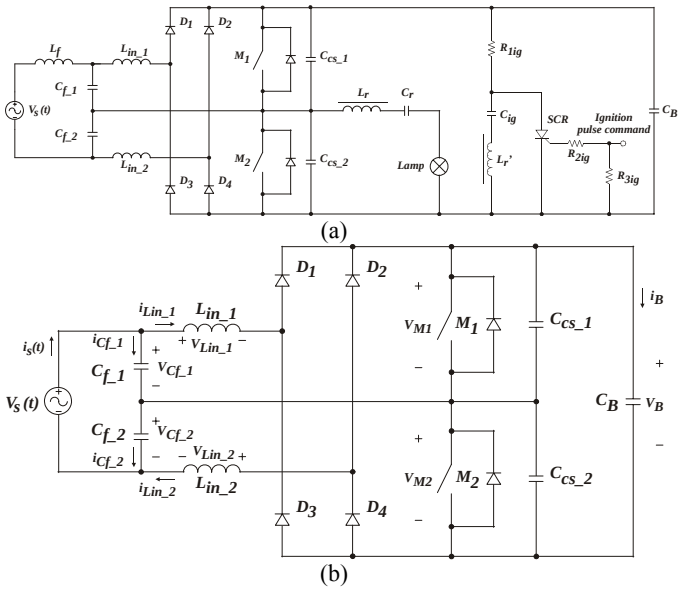

Fig. 1. Ballast topology. (a) Complete proposed Charge-Pump Voltage-Source. (b) Proposed PFC circuit.

II. ANALYSIS OF THE PFC STAGE

The proposed topology is presented in Fig. 1 (a), where the ignition circuit is also included. The ignition pulse is commanded by a microcontroller. The same microcontroller is used to control the output power in a closed loop manner. This structure integrates into one stage a PFC circuit and a half bridge inverter, which supplies the lamp. Although this topology is a single-stage ballast, the input and output functions can be studied separately. The input function is the PFC stage and the circuit that represents this stage is shown in Fig. 1 (b).

To proceed with the PFC analysis, capacitors C_{f_1} and C_{f_2} will be considered equal and large enough to neglect voltage oscillations over one switching period. In the same manner, C_B will be considered large enough to neglect oscillations in dc-link voltage V_B and voltage V_S will be considered constant during one switching period. In the PFC circuit of Fig. 1 (b), filter inductance L_f will be neglected to simplify the analysis and to show that its presence is important for filtering high frequency harmonic distortions in the input current.

The steady-state operation of the PFC circuit during one switching period includes eight stages shown in Fig. 2 whose theoretical waveforms are presented in Fig. 3. All of the components are considered ideal. To guarantee symmetrical operation of the PFC circuit, L_{in_1} and L_{in_2} need to be equal, as C_{f_1} and C_{f_2}. The design of the circuit is done in a way to guarantee that dc-link voltage V_B is larger than peak input voltage V_S, in order to avoid harmonic distortions in the input current.

In this topology, i_{Cf_1} and i_{Cf_2} are the currents flowing through capacitors C_{f_1} and C_{f_2}, respectively. L_{in_1} and L_{in_2} are the input inductors that limit the current of the PFC stage. C_{cs_1} and C_{cs_2} are soft-switching capacitors and C_B is the dc-link capacitor. M_1 and M_2 represent the switches of the circuit.

Stage 1 (t_0, t_1): Before t_0, switch M_2 is on and the current through L_{in_2} is increasing. At t_0, this switch is turned off and a soft-switching transition involving C_{cs_1} and C_{cs_2} occurs. This stage ends when the voltage across C_{cs_1} is equal to zero and the voltage across C_{cs_2} is equal to the dc-link voltage.

Stage 2 (t_1, t_2): Once the soft-switching stage is over, the body diode of M_1 takes over the current. Inductor L_{in_2} starts discharging on dc-link capacitor and inductor L_{in_1} starts charging due to the voltage across C_{f_1}. During this stage, M_1 is turned on in order to avoid switching losses.

Stage 3 (t_2, t_3): At the moment when i_{Lin_1} is equal to i_{Lin_2}, the current through switch M_1 inverts, however i_{Lin_1} is still increasing and i_{Lin_2} is still decreasing.

Stage 4 (t_3, t_4): This stage starts when i_{Lin_2} reaches zero. After this, there is only current through L_{in_1}, which is still increasing. This stage ends when M_1 is turned off. At t_4, i_{Lin_1} reaches its peak value i_{max}.

The stages "5 to 8" are symmetrical to stages "1 to 4". The difference between them is the charge of the inductor Lin_2 and the discharge of inductor Lin_1. For this reason this four stages will not be discussed at this point, but they are presented in Fig. 2.

As shown in stages "1" and "5", there are two soft-switching transitions in one switching period. Even so, these soft-switching transition intervals are presented in operating stages they can be neglected. Based on equation (2) it is possible to understand that these intervals are very short when compared to one switching period. Solving (1) for the dc-link voltage and half of i_{Lin_1} circulating through C_{cs_1}, equation (2) can be obtained. The transition interval is represented by T_t and capacitors $C_{cs\_1} = C_{cs\_2}$.

$$i_{Ccs\_1} = C_{cs\_1} \cdot \frac{\partial V_{Ccs\_1}}{\partial t} \tag{1}$$

$$T_t = \frac{V_B \cdot 2 \cdot C_{cs\_1}}{i_{max}} \tag{2}$$

At the first half of the period, current i_{Lin_1} is described by:

$$i_{Lin\_1} = \frac{V_S}{2 \cdot L_{in\_1}} \cdot (t - t_1) \tag{3}$$

When the switching interval is equal to half of the period the current is at its peak value. This value is represented by:

$$i_{max} = \frac{V_S}{2 \cdot L_{in\_1}} \cdot \frac{T_s}{2} = \frac{V_S \cdot T_s}{4 \cdot L_{in\_1}} \tag{4}$$

From "Kirchoff Current Law" [KCL] applied to Fig. 1 (b) it is possible to obtain:

$$i_S = i_{Lin\_1} + i_{Cf\_1} = i_{Lin\_2} + i_{Cf\_2} \tag{5}$$

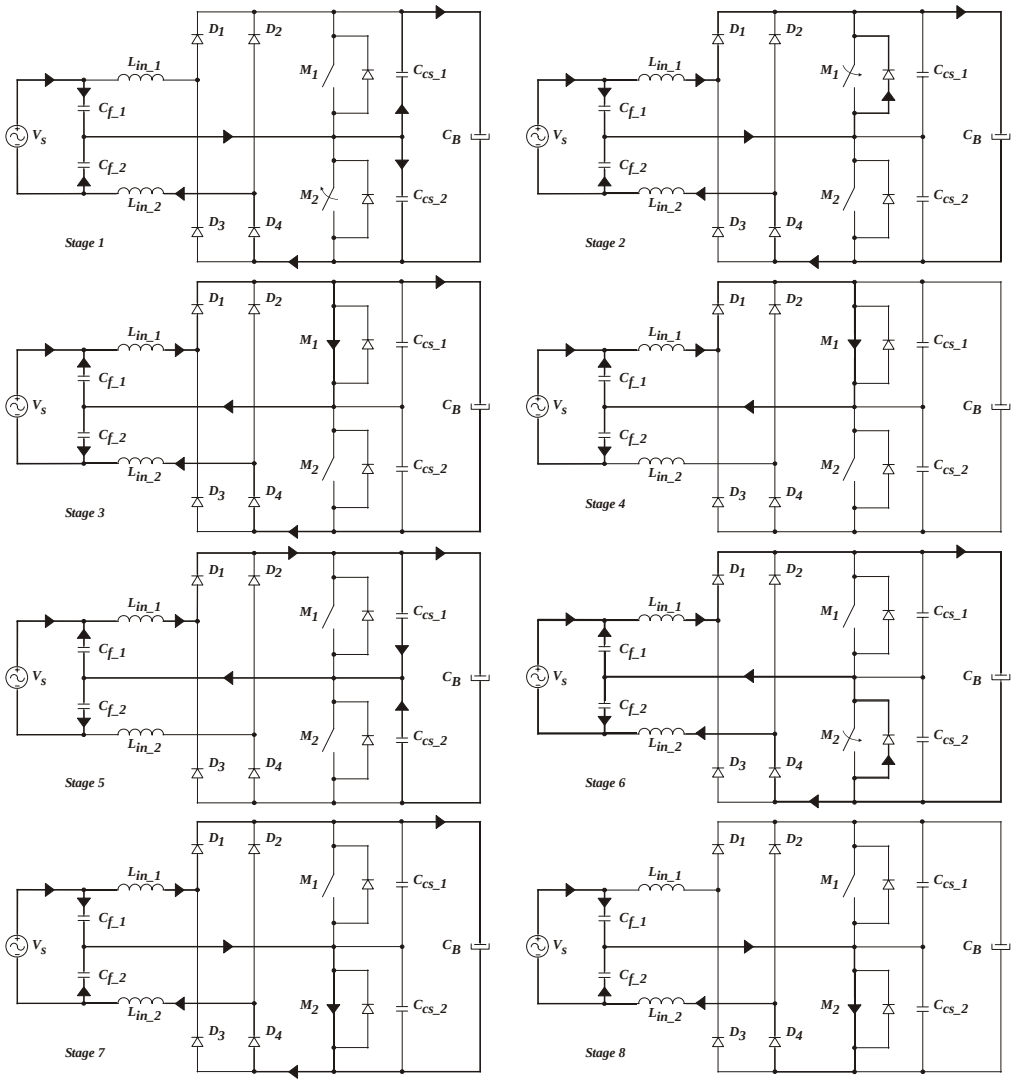

Fig. 2. Operating modes of PFC stage.

Analyzing i_{Cf_1} and i_{Cf_2} and the voltages across these capacitors in the first half of the period, the currents can be described as:

$$i_{Cf\_1} = C_{f\_1} \cdot \frac{\partial V_{Cf\_1}}{\partial t} = C_{f\_1} \cdot \frac{\partial \left(V_S - V_{Cf\_2} \right)}{\partial t} = -C_{f\_1} \cdot \frac{\partial V_{Cf\_2}}{\partial t} \tag{6}$$

Considering that these capacitors have the same value:

$$i_{Cf\_1} = -i_{Cf\_2} \tag{7}$$

From KCL and (6) it is possible to confirm that:

$$i_S = \frac{\left(i_{Lin\_1} + i_{Cf\_1} \right) + \left(i_{Lin\_2} + i_{Cf\_2} \right)}{2} \tag{8}$$

Substituting (7) into (8), the input current is described by:

$$i_S = \frac{i_{Lin\_1} + i_{Lin\_2}}{2} \tag{9}$$

Since the charging times of L_{in_1} and L_{in_2} are different from their discharging times, a high frequency oscillation in the input current appears. This oscillation can be seen in Fig. 3, however, to simplify the analysis, this high frequency oscillation will be neglected. For this reason, the maximum current in the source can be represented by:

$$i_m = i_{max} = i_{Lin\_1} + i_{Lin\_2} \tag{10}$$

And the input current can be approximated by:

$$i_S = \frac{i_m}{2} \tag{11}$$

The source is sinusoidal and is represented by:

$$V_S(t) = V_S \cdot sin\left(\omega \cdot t \right) \tag{12}$$

Substituting (4) and (12) into (11), the equation of the input current is:

$$i_S = \frac{T_s \cdot V_S}{8 \cdot L_{in\_1}} \cdot sin\left(\omega \cdot t \right) \tag{13}$$

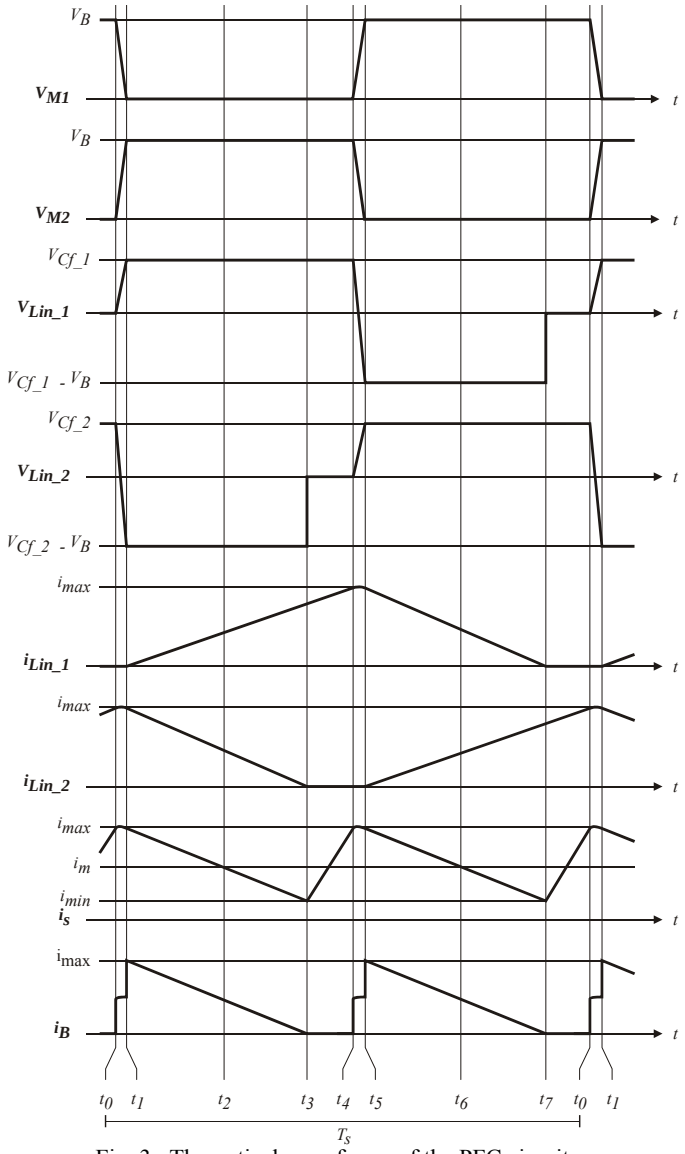

Fig. 3. Theoretical waveforms of the PFC circuit.

The average of the real input power P_{in} is determined by:

$$P_{in} = \frac{1}{\pi} \cdot \int_0^{\pi} \left(V_S \cdot i_S\right) \cdot \partial\left(\omega \cdot t\right) = \frac{T_s \cdot V_S^{\,2}}{16 \cdot L_{in\_1}} \qquad (14)$$

The power factor [*PF*] is given by:

$$PF = \frac{P_{in}}{V_{S\_rms} \cdot i_{S\_rms}} = \frac{\dfrac{T_s \cdot V_S^{\,2}}{16 \cdot L_{in\_1}}}{\dfrac{V_S}{\sqrt{2}} \cdot \dfrac{T_s \cdot V_S}{8 \cdot \sqrt{2} \cdot L_{in\_1}}} = 1 \qquad (15)$$

With this result it is possible to see that a high power factor can be obtained when the correct input filter is used to reduce the high frequency current harmonics. It is important to note that the high frequency oscillation in the input current occurs at twice the switching frequency, as shown in Fig. 3. This characteristic provides a smaller inductor for the input filter, reducing weight and size. Inductance L_{in_1} is designed to operate in PFC situations for the active input power desired at ballast, as follows:

$$L_{in\_1} = \frac{V_S^{\,2}}{16 \cdot f_s \cdot P_{in}} \qquad (16)$$

According to simulation results, if resonant frequency ω_0 is about three-tenths of the switching frequency, unity power factor is obtained. This relation is shown in (17) and input capacitor C_{f_1} is given by (18).

$$\alpha = \frac{\omega_0}{\omega_s} = 0.3 \qquad (17)$$

$$C_{f\_1} = \frac{4 \cdot P_{in}}{\pi^2 \cdot f_S \cdot V_r^{\,2} \cdot \alpha^2} \qquad (18)$$

III. HALF-BRIDGE INVERTER

Although the half-bridge inverter is a well known topology in the technical literature, this paper will approach this structure in a different focus. This study is done in a way to obtain some equations and curves that show the behavior of the power of the lamp during its life and that are able to justify the use of the feedback control system.

In high-frequency operation, the steady-state impedance of the HPS lamp can be considered a resistor, R_{Lamp}. The series resonant network, L_r, C_r and R_{Lamp}, operates as an inductive load in steady-state. The inverter stage operates above the resonant frequency, achieving zero voltage soft-switching turn-on.

Before the start-up of the lamp, its resistance is so high that it can be considered an open circuit. Immediately after start-up, this resistance falls to very low values, almost a short circuit, and starts increasing until reaching its steady-state value, which is obtained after several minutes.

Dc-link capacitor C_B is large enough to obtain dc-link voltage V_B. Dc-blocking capacitor C_r is used to block the dc component of the square-wave voltage and prevents the cataphoresis problem at the electrodes of the lamp.

The circuit that represents this inverter is presented in Fig. 4. Its operating stages are presented in Fig. 5 and the main waveforms are shown in Fig. 6, where V_{GM1} and V_{GM2} are the drive voltages of switches M_1 and M_2, respectively.

Stage 1 (t_0, t_1): Before t_0, M_2 is conducting the lamp current. At t_0 this switch is turned off. A commutation stage occurs during which the voltage across M_1 decreases to zero due to the discharge of C_{cs_1} and the voltage across M_2 increases to dc-link voltage V_B due to the charging of C_{cs_2}. At t_0 the current in the lamp is at its negative peak.

Stage 2 (t_1, t_2): After switching, the body diode of M_1 conducts the lamp current until it changes its direction. During this stage M_1 is turned on, avoiding switching losses.

Stage 3 (t_2, t_3): When the direction of the lamp current changes, M_1 takes over the current which increases until t_3 when M_1 is turned off. At t_3, the lamp current reaches its positive peak value.

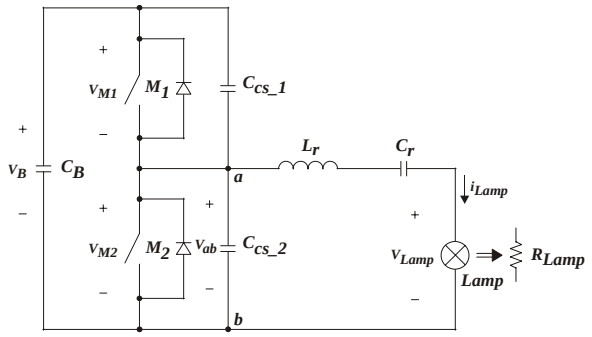

Fig. 4. Half-bridge inverter.

The behaviors of the stages "4 to 6" are symmetrical to the behavior of the stages "1 to 3". The difference between them is the current direction in the lamp, which make the switch M_2 assumes this current. For this reason these stages will not be described in this paper, but they are presented in Fig. 5.

From the waveform of V_{ab} in Fig. 6 it is possible to calculate the Fourier series of voltage VB_{ab}. This voltage is the one which is applied across the series resonant filter.

$$V_{ab}(t) = \frac{V_B}{2} + \frac{2 \cdot V_B}{\pi} \cdot \sum_{n=1}^{\infty} \frac{1-(-1)^n}{2 \cdot n} \cdot \sin(n \cdot \omega_s \cdot t) \qquad (19)$$

In this equation, variable ω_s is the angular switching frequency and the fundamental peak voltage is given by:

$$V_{ab-pk} = \frac{2 \cdot V_B}{\pi} \qquad (20)$$

To simplify the analysis of the circuit, only the RMS value of equation (19) will be considered. This value is indicated by:

$$V_{ab-rms} = \frac{V_B \cdot \sqrt{2}}{\pi} \qquad (21)$$

From Fig. 4, it is possible to obtain the value of the series resonant filter impedance.

$$Z = R_{Lamp} + j \cdot \left(\frac{-1 + \omega_s^{\,2} \cdot C_r \cdot L_r}{\omega_s \cdot C_r} \right) \qquad (22)$$

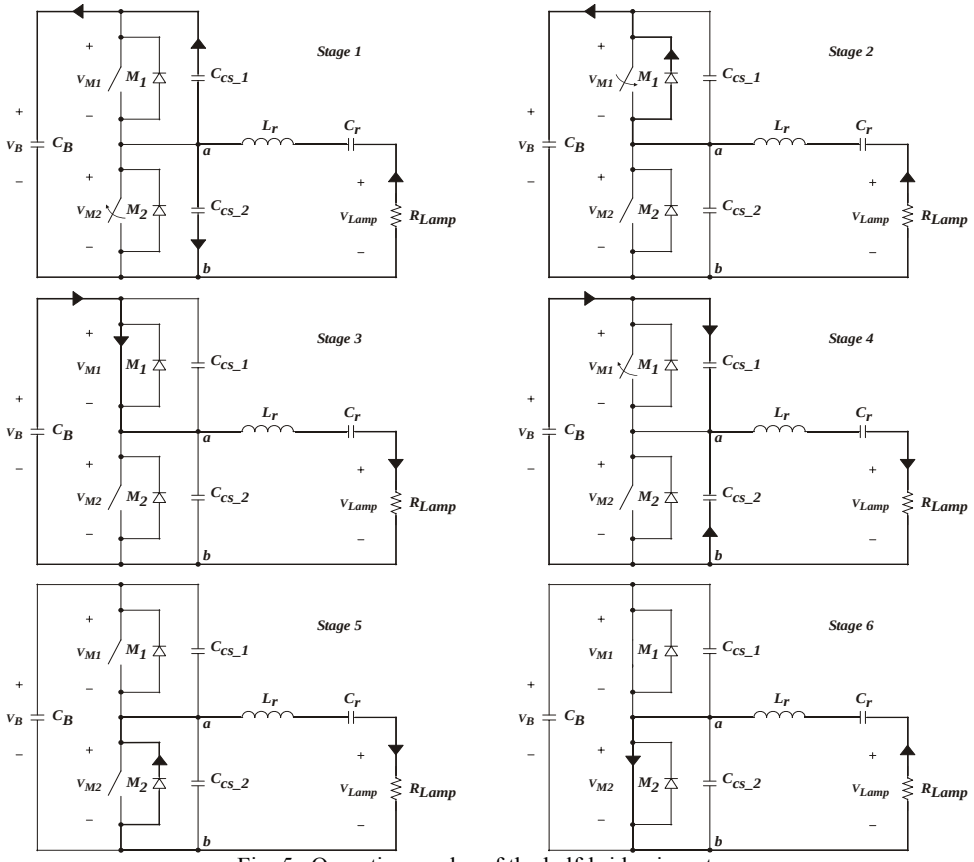

Fig. 5. Operating modes of the half-bridge inverter.

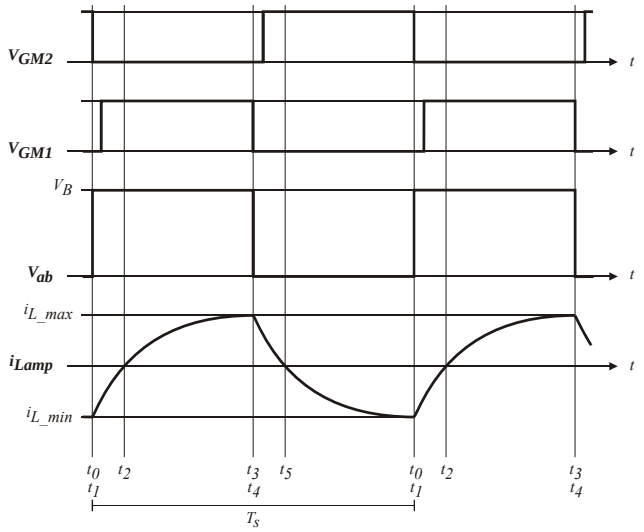

Fig. 6. Waveforms of the half-bridge inverter.

This impedance has a real part and an imaginary one. The phase between fundamental voltage V_{ab} and the current through the series resonant filter is given by:

$$\phi = \tan^{-1}\left(\frac{\mathrm{Im}(Z)}{\mathrm{Real}(Z)}\right) = \tan^{-1}\left(\frac{-1+\omega_s^{\,2}\cdot C_r\cdot L_r}{\omega_s\cdot C_r\cdot R_{Lamp}}\right) \quad (23)$$

Inductance L_r can be written as a function of R_{Lamp}, C_r and phase ϕ:

$$L_r = \frac{\omega_s\cdot C_r\cdot R_{Lamp}\cdot\tan(\phi)+1}{\omega_s^{\,2}\cdot C_r} \quad (24)$$

The current through the filter can be written as the ratio between voltage V_{ab} and the LC series resonant filter impedance:

$$I = \frac{V_{ab-rms}}{Z} \quad (25)$$

Substituting equations (21), (22) and (24) into (25), the current is determined.

$$I = \frac{V_B\cdot\sqrt{2}}{\pi\cdot R_{Lamp}\cdot\left(1+j\cdot\tan(\phi)\right)} \quad (26)$$

The power of the lamp is determined by:

$$P = R_{Lamp}\cdot I^2 \quad (27)$$

Replacing (26) in (27) the power equation of the lamp can be obtained as a function of the phase, the lamp resistance and the dc-link voltage:

$$P = R_{Lamp}\cdot\left|\frac{V_B\cdot\sqrt{2}}{\pi\cdot R_{Lamp}\cdot\left(1+j\cdot\tan(\phi)\right)}\right|^2 \quad (28)$$

Plotting the result of equation (23), the behavior of the phase angle as a function of the lamp's equivalent resistance can be seen. Fig. 7 (a) shows that, as the lamp ages and its impedance increases, the phase angle decreases.

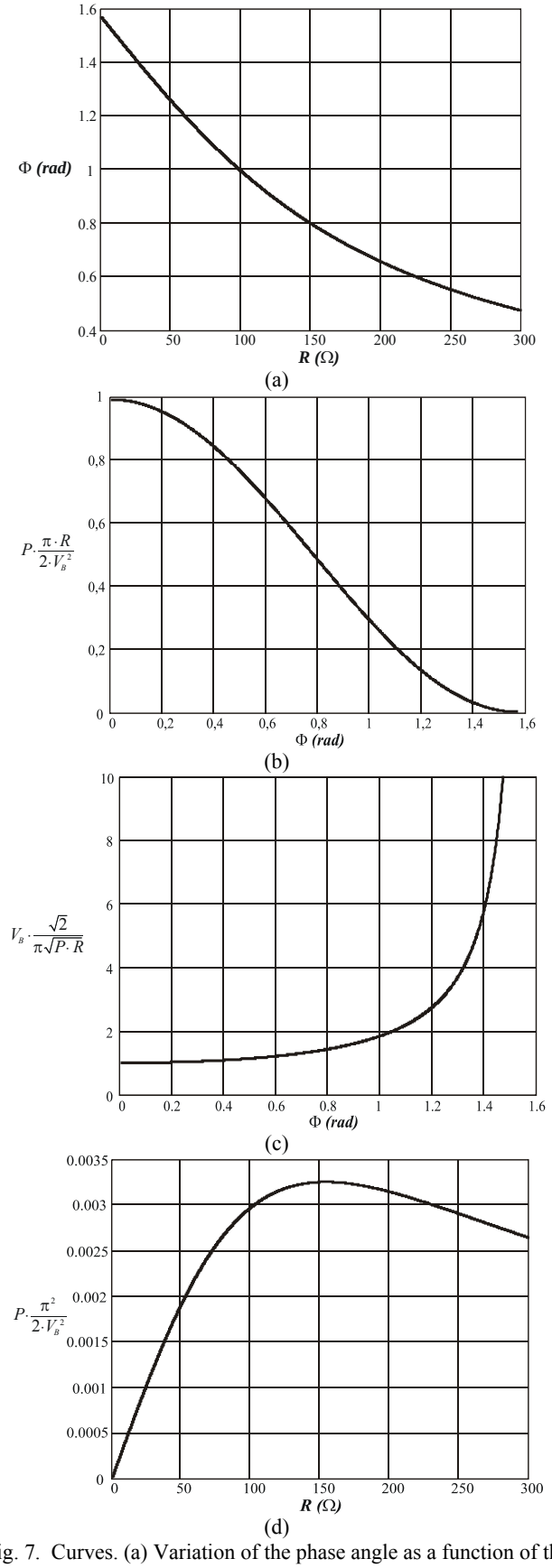

Fig. 7. Curves. (a) Variation of the phase angle as a function of the lamp's equivalent resistance. (b) Normalized power of the lamp as a function of the phase angle. (c) Normalized dc-link voltage as a function of the phase angle. (d) Normalized lamp power as a function of the lamp's resistance.

This result is important to understand Fig. 7 (b) which shows the behavior of the normalized power of the lamp as a function of the phase angle. This figure was obtained from equation (28) and shows that as the angle increases, the power of the lamp decreases. In this manner, as the lamp ages, the power of the lamp increases. This behavior shows that a power control system, not showed in this paper must be applied to avoid this effect and provide constant power to the lamp.

Another important result obtained from (28) is shown in Fig. 7 (c). This one presents the normalized behavior of the dc-link voltage as a function of the phase angle. As the lamp ages and the phase angle decreases, the dc-link voltage also decreases. If this voltage decreases and becomes lower than the peak of the input voltage, the power factor will decrease due to the high harmonic distortion in the input current.

To illustrate the power behavior of the lamp throughout its lifetime, Fig. 7 (d) presents the normalized power of the lamp as a function of the lamp's resistance, maintaining constant the switching frequency of the inverter. This curve confirms that if the ballast does not have a control system, the lamp will receive more power than desired throughout its lifetime and, consequently, its life will be reduced.

IV. EXPERIMENTAL RESULTS

The ballast topology proposed in Fig. 1 (a) was implemented in the laboratory and it was designed for a 70W high pressure sodium lamp. The electronic ballast is operated using a microcontroller to generate switch pulses and to control the output power. The feedback control system used hysteresis control, which measured the power of the lamp and regulated the frequency in order to obtain the correct power value.

The system parameters used for this experiment were:

$$V_S(t) = 220 \cdot \sqrt{2} \cdot sin(\omega \cdot t)\, V \qquad L_f = 3\ \text{mH}$$

$$C_{f\_1} = C_{f\_2} = 82\ \eta\text{F} \qquad L_{in\_1} = L_{in\_2} = 1.35\ \text{mH}$$

$$L_r = 950\ \mu\text{H} \qquad C_r = 22\ \eta\text{F}$$

$$C_B = 50\ \mu\text{F} \qquad D = 0.5$$

The initial design was done for a switching frequency equal to 50 *kHz*, but this value changes according to the lamp's equivalent resistance during its lifetime and due to variations in the input source voltage. The soft-switching capacitors used in this experiment were the internal drain-source capacitors of the MOSFETs.

Fig. 8 (a) shows input voltage $V_S(t)$ and input current $i_S(t)$. The measured power factor is 0.995. Fig. 8 (b) shows current i_{Lin_1} and current i_{Lin_2}. Fig. 8 (c) shows the voltage and the current waveforms of switch M_1 which were obtained at the peak of the input source voltage. The waveforms in Fig. 8 were obtained with a new lamp and illustrate the behavior of the PFC stage. It is possible to see that the switches commutate under the zero voltage condition, therefore, obtaining low switching losses.

To illustrate the behavior of the half-bridge inverter some waveforms are presented in Fig. 9. In Fig. 9 (a) voltage V_{Lamp} and current i_{Lamp} at the peak of input voltage $V_S(t)$ are presented showing that the lamp operates like a resistance at high frequency. Fig. 9 (b) presents the low frequency lamp current showing that the crest factor is 1.52. With the power measured in Fig. 8 (a) and Fig. 9 (b) the efficiency of the ballast results close to 96%. In order to improve the efficiency transistors with very low R_{DSon} (IRF27N60K) were used in this experiment.

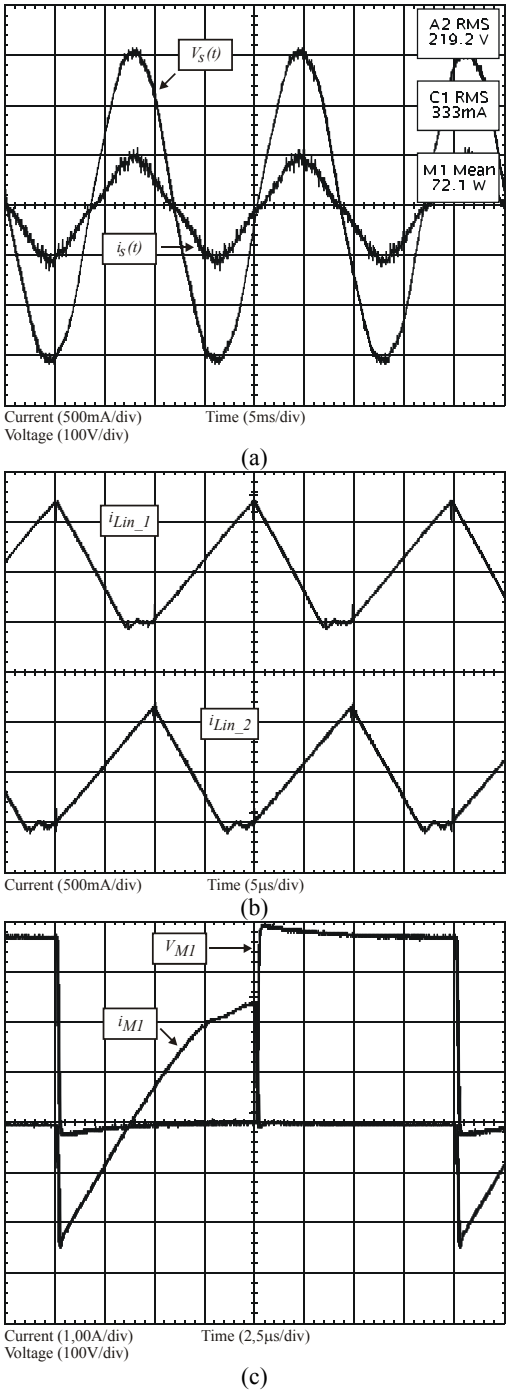

Fig. 8. Ballast waveforms for a new lamp. (a) Input source voltage and current. (b) Current $\boldsymbol{i_{Lin\_1}}$ and $\boldsymbol{i_{Lin\_2}}$. (c) Voltage and current of $\boldsymbol{M_1}$.

To show the behavior of the power control system applied to this ballast, Fig. 10 presents the waveforms for an old lamp operated by the same ballast. It is possible to note that the values of the voltage and current of the lamp

presented in Fig. 10 (a) are different from those shown in Fig. 9 (a) due to the higher equivalent resistance of the lamp. Moreover, the frequencies of these waveforms are different. In Fig. 10 (b) the low frequency current through the lamp is shown. In this case, the crest factor is 1.43 and proves that this value does not change significantly throughout the lamp's lifetime. Comparing the acquisition values of Fig. 9 (b) and Fig. 10 (b) it is possible to see that the measured power of the lamp is still close to the desired lamp power, validating the feedback control system applied to this ballast.

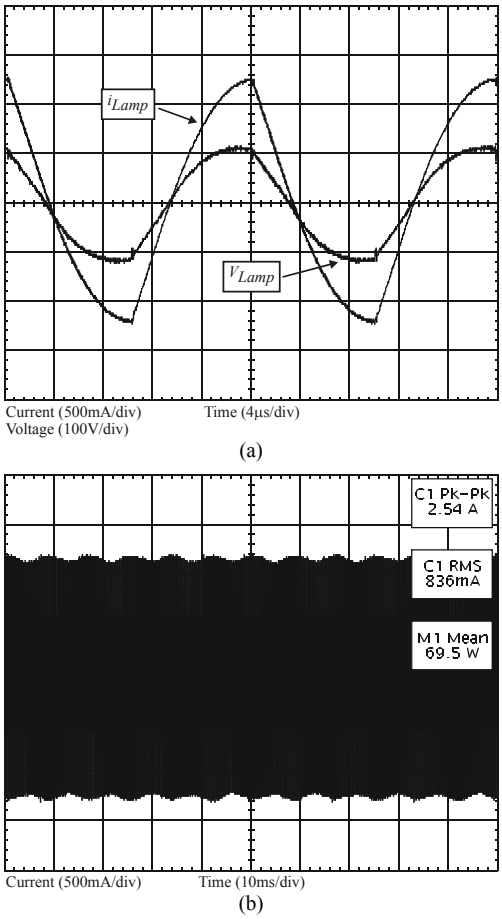

Fig. 9. Ballast waveforms for a new lamp. (a) Voltage and current of the lamp at high frequency. (b) Low frequency current through the lamp.

The measured line current harmonics are presented in Fig. 11. Each measured harmonic component meets the IEC 61000-3-2 Class C requirements.

As the feedback control law operates in the switching frequency some experimental were done to prove that these variations on the switching period do not change the power factor and the crest factor in a significant way.

Table 1 shows some acquisitions which were done with two new lamps and two older lamps. This table validates the good behavior of the output power control of the proposed topology. In this case, the transistors used in the experimentation have higher R_{DSon} (IRF22N60K) reducing the efficiency. The results showed in Fig. 8 and Fig. 9.

During the experimentations, the acoustic resonance was not detected mainly because the power control loop changes the switching frequency if the load changes, which is one of the consequences when the acoustic resonances occurs.

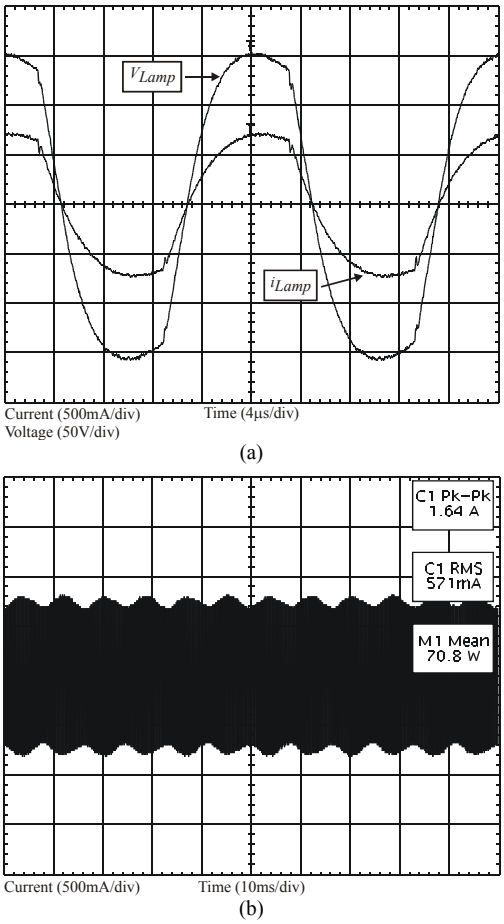

Fig. 10. Ballast waveforms for an old lamp. (a) Voltage and current of the lamp at high frequency. (b) Low frequency current through the lamp.

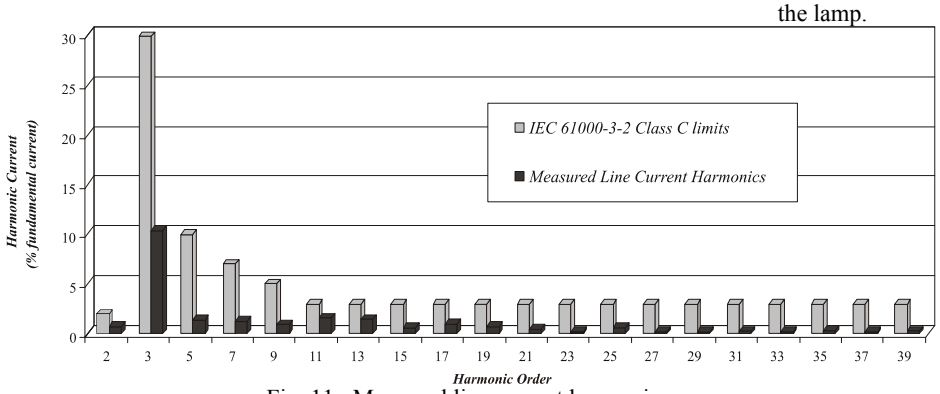

Fig. 11. Measured line current harmonics.

TABLE 1. Comparison between the operation of the ballast with new lamps and old lamps.

	New Lamp 1	New Lamp 2	Old Lamp 1	Old Lamp 2
Source Power	79.33 W	79.44 W	78.95 W	80.64 W
Lamp Power	70.94 W	71.89 W	72.26 W	73.22 W
Efficiency "η"	89.43 %	90.52 %	91.47 %	90.79 %
Lamp Voltage	71.67 V	88.21 V	108.7 V	122.3 V
Lamp Current	994.5 mA	820.8 mA	669.4 mA	606.5 mA
Crest Factor	1.552	1.524	1.583	1.572
Voltage THD	3.472 %	3.413 %	3.340 %	3.558 %
Current THD	11.996 %	13.075 %	13.009 %	14.080 %
Power Factor	0.990	0.990	0.989	0.989

V. CONCLUSION

A single-stage charge-pump voltage-source electronic ballast with unity power factor was presented. The proposed electronic ballast combines a PFC stage and an inverter stage in one topology to drive the HPS lamp. The topology was analyzed in detail. This analysis was done in two stages. The first stage analyzed the PFC stage. It was shown that with a proper high frequency input filter unity power factor can be achieved and that the input current is at twice the switching frequency, reducing the magnetic elements. In the second stage, the half bridge inverter was analyzed and a design methodology was presented. A microprocessor was used to generate the pulse signals that drive the switches and control the power of the lamp. This control system adjusts the switching frequency in a way to obtain constant output power. This control system guarantees constant lamp power, low THD and low crest factor when the lamp ages and when the input voltage oscillates. Therefore, this topology can be improved with special functions due to the microprocessor, which include lamp turn on at the beginning of the night and lamp turn off at the end of the night, dimmering the lamp at times when lower power is sufficient, thus saving electricity, and ballast protection in the case of a broken lamp or start-up failure. Additionally the proposed electronic ballast may provide high energy efficiency and low cost when compared to the conventional HPS electronic ballast.

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