DEVELOPMENT OF A DIDACTIC PLATFORM FOR FLEXIBLE POWER ELECTRONIC CONVERTERS

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***Abstract* – Power electronic converters are the subject of several studies and applications. Knowledge about those converters is essential for several technical and undergraduate courses in the field of Electrical Engineering and related areas. The presence of converter modules in laboratories can be beneficial for experimental validations in academic research and educational purposes, for allowing students to have practical contact with different converter topologies and applications. However, the commercially available power converters are generally manufactured for specific applications, with poor versatility and high cost, when applied for academic purposes. For this reason, several laboratories propose the design of versatile converters, mainly for multilevel converter research. Nevertheless, most of these projects present module designs based on half-bridge topology due to their low cost. Therefore, this project topology requires more modules to operate as topologies based on a full-bridge converter. Besides, modules based on full-bridge topology can also work in a half-bridge configuration. Thus, this work presents the design of full-bridge modules capable of operating as different types of converters, as well as the project of the dc-link voltage measurement, isolated power supply and bypass circuits. Moreover, this work addresses the heatsink choice, the thermal evaluation for the semiconductor devices and the realization of galvanic isolation between the signal and power circuits.**

***Keywords* – Converter, Galvanic Isolation, Multilevel Converter, Thermal Design, Versatile Modules.**

I. INTRODUCTION

Several applications use power electronic converters, such as photovoltaic systems, wind turbine systems, battery chargers and electric motor control systems. Furthermore, new studies and converter topologies are constantly emerging. However, simulations and features, such as hardware-in-the-loop (HIL) and software-in-the-loop (SIL), are used in most of the research validations [1]. Besides, research validations carried out through experimental setups highlight some physical characteristics, such as the parasitic effects, which can significantly affect the converter performance, depending on the context [2]. Thus, these effects are not easy to reproduce in HIL or simulations.

Another aspect is the teaching of Power Electronics challenges, such as relating and applying concepts of circuits, control, signals and systems and presenting standards about power quality and harmonic distortions. In addition, several authors discuss the benefits of practical activities in the academic training of new engineers. A power electronics course based on theoretical classes followed by practical classes related to different engineering applications has been recently presented in [3]. It also provides a questionnaire that highlights the opinion of students about the impacts of experimental activities on learning. The results reveal that most students agree that experiments help to link engineering applications to the basic circuits presented in textbooks.

Furthermore, reference [4] presents different experiments that can help the teaching of Power Electronics. They aim to expose the students to situations that demonstrate the significance of simulations, modeling and especially the applicability of this knowledge in electrical engineering problems. McShane et. al. [5] presents a teaching approach that provides a fundamental background in the different technical areas that constitute Power Electronics, aimed at undergraduate and graduate programs. A guide for teaching Power Electronics is presented in [6] to familiarize students with various applications and facilitate future practical activities. The authors in [7] present a teaching strategy where the students choose an electronic power converter application and implement the entire design during the course.

Besides, with the constant increase in the number of generation systems based on renewable energies, the presentation of experiments related to these applications for electrical engineering courses has been increasingly required. Reference [8] presents a laboratory course where renewable energy generation systems and tools, such as Simulink and dSPACE, are employed. In [9], the authors present a workbench to help the teaching of photovoltaic systems.

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The presented workbench consists of a real-time monitoring system and a double-stage photovoltaic system connected to the grid.

The aforementioned references show the importance of experimental activities in the teaching of Power Electronics. In addition, teaching strategies based on design-oriented projects, as presented in [7], can be costly and time-consuming, as new electronic components are needed each semester. In order to combine these facts with the hardware demand for experimental validations in research, the availability of power converters is essential for power electronics laboratories. However, commercial converters are not a viable option for this type of application, due to their low versatility and high cost. For this reason, several institutions assemble their own didactic converters.

The authors in [10] present a review of projects of multilevel converters from different laboratories used for academic purposes. In [11] it is designed a versatile teaching platform for the control of three-phase motor and inverter experiments. The authors in [12] present a design of robust, safe and cost-effective equipment for practical activities related to power electronics in technical and undergraduate levels. Finally, in [13], it is presented a modular power electronics protoboard for academic purposes that can perform experiments involving various converter topologies.

The project complexity and cost vary according to the voltage level and system topology. However, there are similarities between some of the converter circuits that make it possible to use the same modules for different topologies. This similarity is in the half-bridge (HB) circuit that appears in different topologies, as shown in Figure 1 [14].

Recently, [14] has proposed the design of a didactic platform based on HB converters. They affirm that the didactic platform can be arranged in several other converter topologies, using HB modules. However, the same topologies can be obtained with a smaller number of didactic platforms with a full-bridge (FB) configuration instead, since the FB module can operate as an HB module. Table I shows the possible switching states for a FB module configuration. It is possible to obtain an HB circuit performing the combinations of operations A and B (Figure 2), C and D, A and D, or B and C. In addition, the FB topology is used in several applications, such as dual-active bridge converters [15], dual-phase interleaved dc-dc converters [16] and isolated bidirectional series resonant converters [17].

TABLE I
Switching States for FB Submodule

Operation	S_1	S_2	S_3	S_4	V_{out}
A	On	Off	Off	On	V_{DC}
B	On	Off	On	Off	0
C	Off	On	On	Off	$-V_{DC}$
D	Off	On	Off	On	0

This work presents the design of a test platform based on a FB converter. Therefore, it is possible to operate as different converters with a smaller number of modules and external connections, which are frequently the source of problems in experimental setup commissioning. In addition, the modules

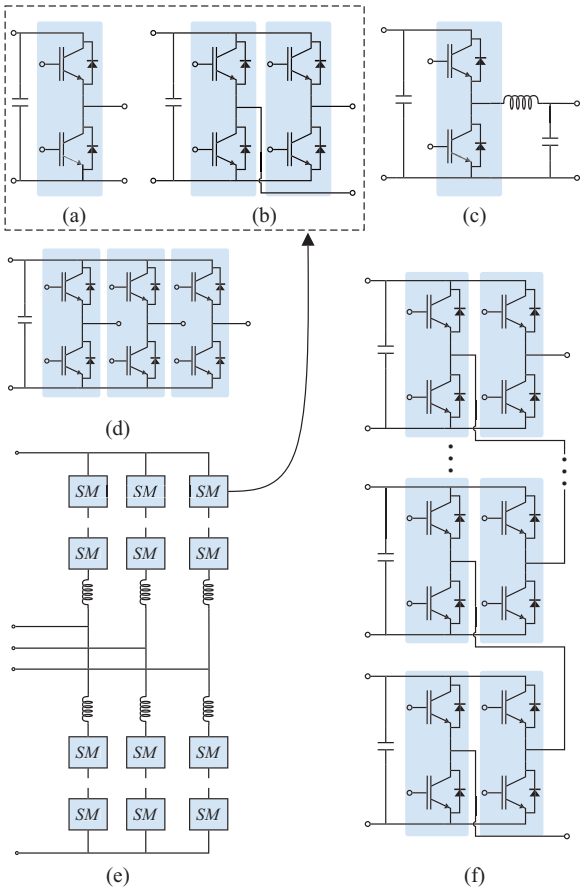


Fig. 1. Some power converter topologies which can be build based on half-bridge: (a) Half-brigde converter (b) Full-bridge converter (c) Bidirectional dc-dc converter (d) 3-phase converter (e) Modular multilevel converter (f) cascaded multilevel converter.

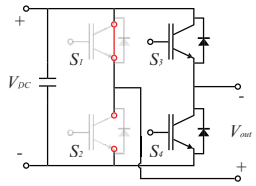


Fig. 2. Full-bridge circuit operating as half-bridge.

have a dc-link voltage measuring circuit, bypass circuit and galvanic isolation between the signal and the power parts of the boards. The experimental tests of the designed didactic platform validate the operation as a dc-dc converter, inverter and cascaded multilevel converter.

The rest of this paper is outlined as follows. Section II presents the module design overview and its technical aspects. Section III presents the cost analysis. Section IV presents the case study. Section V presents the results obtained from the experiments. The conclusions are presented in Section VI.

II. OVERVIEW OF THE DIDACTIC PLATFORM AND MODULE DESIGN

The developed prototype aims to offer researchers and students a cost-effective, robust, safe and versatile didactic platform based on an FB converter. For this reason, the FB didactic platforms are made in printed circuit boards (PCB) with four layers of copper, containing the bridge circuit,

gate-driver circuit, measuring dc-link voltage circuit and the bypass protection circuit. Figure 3 shows the structure of the modules.

Each module has two Pulse-Width Modulation (PWM) signals as input, one for each leg of the bridge, a bypass signal (BP) to short-circuit the module bridge midpoints, and a reset (RST) signal to turn off the Insulated Gate Bipolar Transistors (IGBT). All these signals are isolated from the power part of the board.

The designed modules have the black-start capability [18], due to the presence of an isolated power supply circuit, which supplies the gate-driver and the other integrated circuits (IC). The power supply circuit allows the modules to start switching even if the dc-link and the grid are not connected. However, they must be connected to an isolated 5 V dc source, which is available in most laboratory symmetrical dc power supplies. Thus, rectifier circuits and low-frequency transformers are not needed, which reduces cost and volume.

A. Didactic Platform Parameters and Full-Bridge Circuit

The selection of power parameters for each didactic platform considers the possible operating conditions of the laboratory. The output current chosen is 7 A RMS. This value is consistent with the available loads and considers a safety margin. In addition, the output voltage assumed is 220 V RMS, which is the value available in the laboratory. Finally, the maximum dc-link voltage is defined as 450 volts, considering the state of the art of single-phase photovoltaic inverters on the market. Table II presents the selected values.

TABLE II
Didactic Platform Parameters

Parameter	Symbology	Specification
Output current	$I_{out,rms}$	7 A
Output voltage (line)	$V_{out,rms}$	220 V
dc-link voltage	V_{dc}	450 V

Considering that the maximum dc-link voltage is 450 V, semiconductor devices with a blocking voltage of 600 V are selected [19], which results in a utilization factor of 75%. In addition, more cost-effective IGBTs are commercially available for this voltage rating. The devices with a forward current of 15 A are selected based on the thermal evaluation for a 20 kHz switching frequency. Therefore, the silicon IGBT IKP20N60H3 from the manufacturer Infineon is selected. Besides, Section V.B presents the thermal evaluation of the adopted IGBT and heatsink using simulations.

Didactic platforms FB are also presented in Figure 3. In this circuit, the electrolytic capacitors $C1$, $C2$, $C3$ and $C4$ are used for ripple attenuation in the dc-link, due to their higher energy density, in addition to the bleed resistor R_b, to realize their discharge when the converter shuts down. There are also decoupling capacitors, C_{y1} and C_{y2}, installed close to the IGBT legs to reduce the oscillations caused by IGBTs switching. Polyester capacitors are selected for C_{y1} and C_{y2}, due to their equivalent series inductance.

The sizing of electrolytic capacitors considers the single-phase inverter topology and the maximum tolerable dc-link voltage ripple. The total dc-link capacitance is [20]:

$$C_{total} = \frac{P_o}{2\pi f_0 \delta V_{DC}^2} \tag{1}$$

where P_o is the average power supplied, f_0 is the fundamental frequency, δ is the peak-to-peak per-unit capacitor ripple.

Considering the output voltage and current of Table II, P_o is 1540 VA. For 3% of ripple and a fundamental frequency of 60 Hz, the capacitance obtained is 672.42 μF. The commercial value selected is 680 μF. The design considers four dc-link capacitors in parallel, as shown in Figure 3. Therefore, it is possible to add or remove capacitors to obtain different total capacitances for the dc-link, if necessary in some other application.

In parallel with output terminals A and B, there is the varistor v, used to protect the module from voltage transients, and the bypass components: relay and thyristor. The presence of the bypass circuit is indispensable in modular multilevel or cascaded converter configurations. The bypass allows the system to remain in operation even if some submodules fail. The thyristor is used only in HB applications to guarantee a fast reaction time. However, an eventual dv/dt can trigger the thyristor in the FB configuration. Thus, in FB applications, the thyristor must not be used.

B. Heatsink Selection

The thermal design assumes the maximum current and switching frequency that the devices should support (9.89 A peak current and 20 kHz). The maximum thermal heatsink impedance is given by:

$$R_{sA,max} = \frac{T_C - T_A}{P_{dissipated}} - R_{cH} \tag{2}$$

where T_C is the maximum case temperature in °C of the device, as indicated by the manufacturer, T_A is the ambient temperature in °C, $P_{dissipated}$ is the maximum power rating of the device in Watts and R_{cH} - thermal resistance between the heatsink and IGBT.

R_{cH} is considered equal to the thermal resistance of the mica wafer (used to electrically isolates the IGBT from the heatsink) for the selection of the heatsink. The resistance employed is R_{cH} = 0.40°C/W, and the ambient temperature is considered 40°C. The heatsink model selected is HS4225, from HS *dissipadores*.

C. Power Supply Scheme

The objective of the power supply scheme, illustrated in Figure 4, is to provide isolated voltage supply to the IC and filtered voltage to the measurement circuit from a 5 V dc input. In addition, this circuit eliminates the need for pre-loading to start switching, since the components are not powered by the dc-link. Isolated supplies are necessary, since the same Digital Signal Processor (DSP) can be used to control different FB platforms. Therefore, a single DSP can measure several dc-link voltages that are in reference to different electrical potentials. In this context, galvanic isolation is essential to prevent possible short-circuits.

The π filter improves the electromagnetic compatibility, since the noise produced by the digital circuits does not reach the analog circuits [21]. This filter is composed of

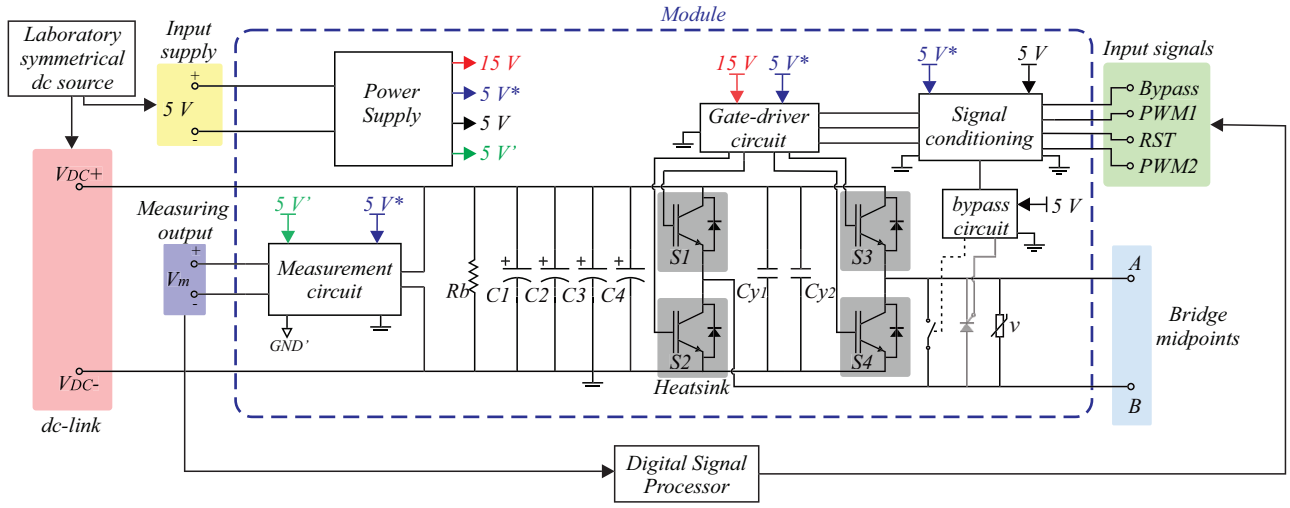


Fig. 3. Proposed scheme for the test platform converter modules.

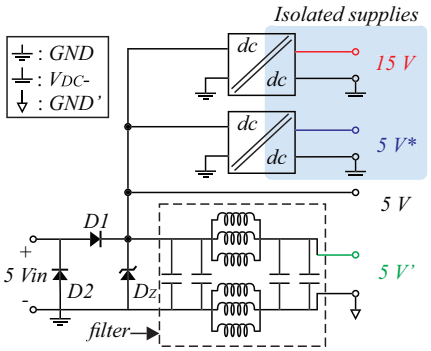


Fig. 4. Isolated dc-dc circuit.

100 nF ceramic capacitors and choke inductors. Moreover, a protection circuit is employed in the voltage input to prevent polarity inversion, fluctuations and over-voltage of the external power supply.

Figure 4 shows three different ground symbologies. The first one, called *GND*, is the digital circuit reference. The second, V_{DC-}, is the power circuit reference, and the third, GND', is the measurement circuit reference. For the generated voltage levels, 5 V* refers to the isolated 5 V for the power circuit, and 5 V' refers to the filtered 5 V for the dc-link voltage measurement circuit.

In Figure 4, D_1 and D_2 are Schottky diodes that ensure protection against reverse polarity. D_Z is a 5.6 V Zener diode that protects the circuit against voltages higher than 5 V.

The first output level follows the protection scheme and supplies the isolated dc-dc converters, bypass circuits, LEDs, buffers and the optocoupler from the signal circuit. After the π filter, the filtered voltage (5 V') supplies the voltage measurement circuit. The other two isolated voltage outputs (5 V* and 15 V), obtained by the dc-dc converters, supply the gate-driver, signal conditioning and measurement circuits. The Traco power part number TBA 1-0511 and TBA 2-0513 are the dc-dc converters employed.

D. Digital Signals Conditioning

This circuit is responsible for receiving the signals coming from the DSP and generating the $PWM1^*$, $PWM2^*$, RST^*, and bypass signals. Figure 5 shows the circuit.

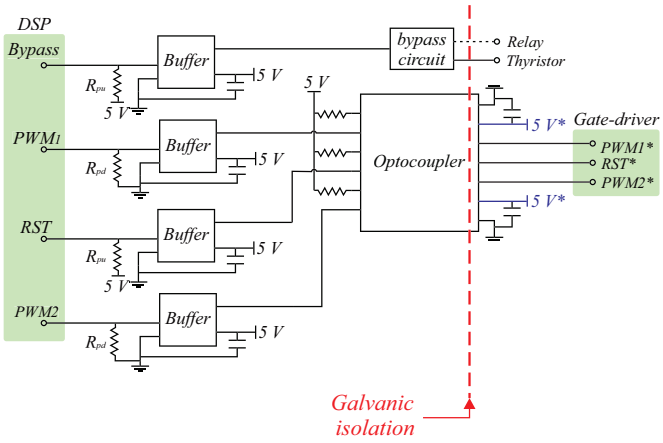


Fig. 5. Signal isolation circuit.

The employed buffers increase the impedance between the DSP and the modules. The SN74LV1T34 IC is employed. Even if the signals from the Texas Instruments F2837x DSP family are 0 or 3.3 V, the buffer output will be 0 or 5 V since it is based in the IC supply value. In the case of PWM and reset signals, there is an optocoupler to perform the galvanic isolation between this part of the board and the power part (gate-driver and full-bridge circuit). It was employed the ACSL-6400 optocoupler.

Pull-up (PU) resistors are used for the bypass and reset signals at the input of the buffers, while pull-down (PD) resistors are used for PWM signals. Thus, in case of signal losses, the pull-up resistors will ensure that the bypass and reset signals remain at a high logic level. This configuration makes the bypass and resets remain active. On the other hand, PWM signals would be at a low logic level due to the pull-down resistors. This configuration ensures the module protection in case of signal losses between DSP and the didactic platform. Both the pull-up and pull-down resistors used are 22 kΩ.

E. Gate-Driver Circuit

Figure 6 presents the gate-driver circuit. Some aspects must be considered in the choice of a gate driver IC: the half-bridge driving capability, easy dead-time implementation and driver disable function. Bootstrap drives are used in this project, since they are a cost-effective option for the chosen full-bridge converter parameters.

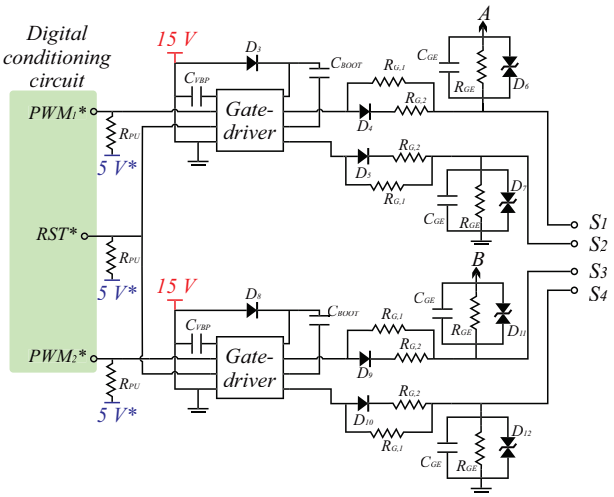


Fig. 6. Gate-driver circuit configuration.

The IR2104 IC is selected based on the designed gate-driver circuit. The floating channel is for bootstrap operation and can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration. It can support up to 600 V between driving outputs.

The bootstrap circuit design depends on the switching frequency and the IGBT gate charge. The switching frequency (f_{sw}) is 20 kHz. Considering the IGBT switch IKP20N65F5, the total gate charge is Q_G = 48 nC. Moreover, a maximum allowed voltage drop for the driving circuit selected is ΔV_{BOOT} = 0.02 V [22]. The minimum bootstrap capacitor is:

$$C_{BOOT} = \frac{Q_G + I_{Q,BOOT}\frac{D_{max}}{f_{sw}}}{\Delta V_{BOOT}} \tag{3}$$

where $I_{Q,BOOT}$ is the quiescent current of the bootstrap circuit and D_{max} is the maximum duty cycle.

The rule of thumb is used to select a high-quality oversized capacitor (usually twice the size is a good practice). For this circuit, the bootstrap capacitor is a polyester capacitor. For the bootstrap diode, the ultrafast recovery MUR160 diode is employed.

The driving circuit must load the IGBT gate charge to open it. Besides, the gate resistance needs to be present to limit the current. The gate resistance is calculated based on the gate charge, turn-on delay time and turn-on rise time. Thus, considering the supply voltage (V_{DD}) as 15 V and the gate voltage for the nominal current ($V_{GS(th)}$), the turn-on and turn-off gate resistance rates are obtained as shown in [23].

According to [24], the value of an optimized gate resistor will be somewhere between the calculated turn-on and turn-off gate resistance and the gate resistance value indicated in the IGBT datasheet. Moreover, in most applications, the turn-on gate resistance $R_{G,on}$ is smaller than the turn-off gate resistance $R_{G,off}$. Depending on the individual parameters, $R_{G,off}$ can be roughly twice the $R_{G,on}$ value. Therefore, the gate resistors R_{G1} and R_{G2} are chosen to be equal to $R_{G,off}$.

The gate-driver connection is based on the Semikron application note [25]. The application note recommends placing a 10 kΩ resistor (R_{GE}) and a suppressor diode (back-to-back Zener diode) between the gate and the emitter. Furthermore, a capacitor (C_{GE}) between the gate and the emitter can be advantageous, even for high-power IGBT modules and parallel operation. The C_{GE} should be approximately 10% of the gate-emitter capacitance of the IGBT used. Those components must be placed very close to the IGBT module.

Finally, based on commercial values and the margins in the evaluated values, the gate-driver circuit main parameters are shown in Table III.

TABLE III
Parameters Used in the Gate-Driver Circuit

R_{G1}	R_{G2}	C_{BOOT}	C_{VBP}	C_{GE}
32 Ω	32 Ω	4.7 μF	100 nF	150 pF

F. Dc-Link Voltage Measurement Circuit

Figure 7 presents the dc-link voltage measurement circuit. The dc-link voltage is reduced to smaller values by a voltage divider. Besides, an optical isolator amplifier galvanically isolates the measurement circuit and the dc-link. The HCPL-7520 is the IC selected. The voltage divider output will be from 0 V to 200 mV, considering a dc-link range from 0 V to 450 V. Under the previous voltage considerations, the output of the HCPL-7520 ranges between 2.5 V and 4.45 V and can exceed the DSP limit. Thus, a differential operational amplifier (op-amp) circuit with a single supply adjusts the voltage to a range supported by the DSP (0 V to 3 V). The TLV247X is the op-amp selected. The transfer function of the differential op-amp circuit is:

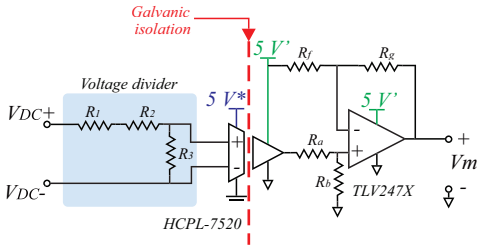


Fig. 7. Dc-link voltage measurement circuit.

$$V_m = V_{in}\left(\frac{R_b}{R_a + R_b}\frac{R_f + R_g}{R_g}\right) - V_{ref}\frac{R_f}{R_g} \tag{4}$$

where V_{in} is the HCPL-7520 output voltage, and V_{ref} is the filtered 5 V.

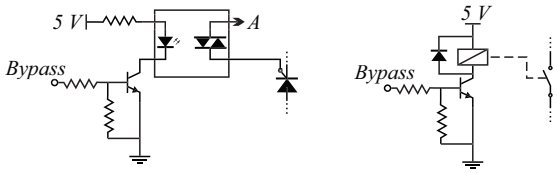
The resistance values of the differential op-amp circuit are obtained solving (4) for the HCPL-7520 output voltages and the desired measurement circuit output voltage V_m range limits, as shown in [26]. Based on commercial values, the selected values of the resistors are shown in Table IV.

TABLE IV
Measurement Circuit Resistance Values

R_f	R_g	R_a
7.68 kΩ	10 kΩ	7.68 kΩ
R_b	R_1, R_2	R_3
51.1 kΩ	1.3 MΩ	1.1 kΩ

G. Bypass Circuit

The bypass circuit is composed of two activation circuits: the thyristor and the relay, shown in Figures 8.a and 8.b.



(a) (b)

Fig. 8. Bypass circuits: (a) thyristor (b) relay.

The driver MOC3041 triggers the bypass thyristor, which isolates the signal from the full-bridge circuit. Besides, a transistor in a common-emitter configuration provides a current gain in the circuit activation signal, due to the thyristor current requirements. A pull-down resistor is used at the base of the transistor to avoid being turned on by electromagnetic interferences.

The relay drive circuit uses a transistor for the same reason as the thyristor circuit. The freewheeling diode parallel to the relay protects the transistor from currents that can appear at the turn-off of the relay. A pull-down resistor avoids accidental turn-on of the bypass circuit.

H. PCB Design

The modules are designed in four copper layer PCBs. The PCB is composed of two fiberglass cores isolated by prepreg. The positive and negative references are separated from the cores, to ensure higher electrical isolation. The negative references and grounds are in the outermost layers. The positive voltage references are in both inner copper layers of the PCB. Figure 9 presents the distribution of voltage references per copper layer. Figure 10 shows the top view of the finished modules. The board dimensions are 272 mm x 127 mm.

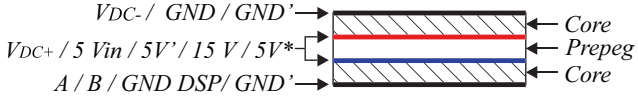


Fig. 9. Voltage reference distribution across the PCB copper layers.

III. COST ANALYSIS

The component choices aim at the best cost-benefit. The PCB manufacturer is JLCPCB. The modules were soldered and tested in the Gerência de Especialistas em Sistemas Elétricos de Potência (GESEP) Power Electronics Laboratory. In this first version, five PCBs were assembled. Table V shows a cost estimate for a single module for July/2022. The component prices were obtained from Digikey, Mouser and HS *Dissipadores*.

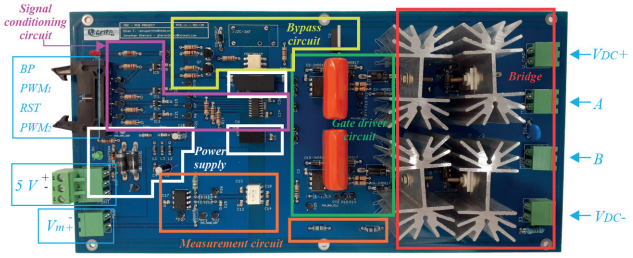


Fig. 10. Board top view.

TABLE V
Cost Estimate for a Single Module

Item	Cost
Electronic components and heatsinks	$ 125.40
PCB	$ 10.96
Total	$ 136.36

The graph in Figure 11 shows the cost distribution for the module components. The most expensive are the dc-link electrolytic capacitors, followed by the PCBs, optocoupler, IGBTs and dc-dc converters.

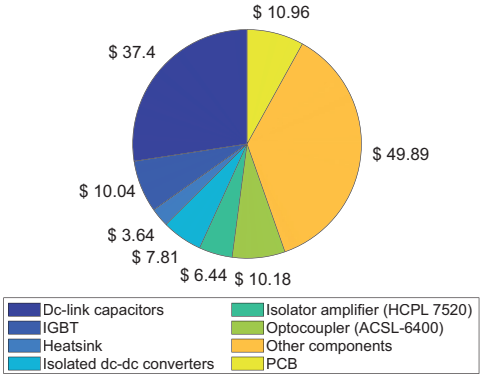
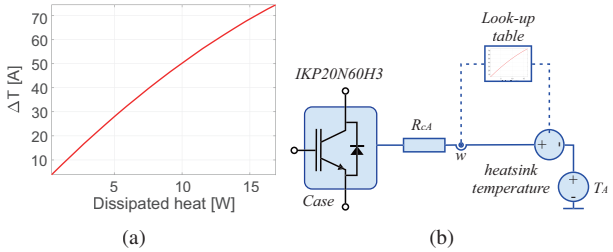


Fig. 11. Cost distribution of modules by component.

IV. CASE STUDY

A simulation of the equivalent thermal circuit of the IGBTs and heatsinks in the PLECS software is used for thermal evaluation. The platform operates as a single-phase FB inverter, with a 20 kHz switching frequency, 450 V dc-link voltage and 7 A (rms) output current. The heatsink-to-ambient thermal resistance temperature dependence is considered in the simulation, following the information provided in Figure 12.a. In this case, a controlled temperature source is used instead of a constant thermal resistor, as shown in Figure 12.b.

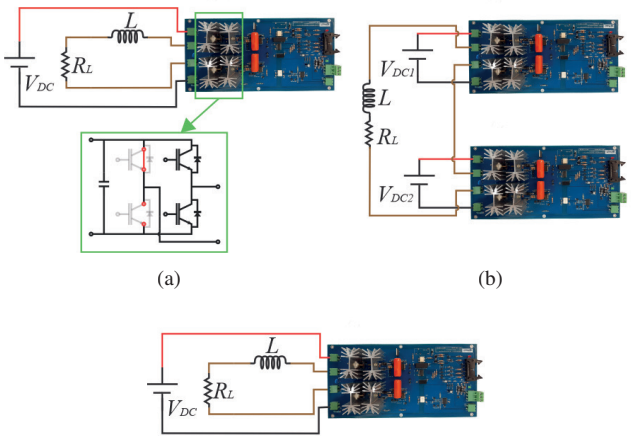
Then, tests are performed as different converter topologies to ensure the versatility of the didactic platforms in both simulation and experiments. Three topologies were selected: Step-down converter with half-bridge configuration, shown in Figure 13.a; 5-level cascaded H-bridge converter, shown in Figure 13.b; Single-phase full-bridge inverter, shown in Figure 13.c. The Tektronix DPO2014B and TDS1001B



(a) (b)

Fig. 12. (a) Temperature variation vs. heat dissipated for heatsink HS4225. (b) IGBT-Heatsink thermal circuit.

oscilloscopes and the A622 current probe are used in the tests. The input signals are generated through the DSP TMS320F28379D from Texas Instruments and programmed by the Matlab Simulink. The parameters used in each experimental setup are shown in Table VI.



(a) (b)

(c)

Fig. 13. Proposed module evaluation experiments: (a) Step-down converter; (b) 5-level cascaded H-bridge converter; (c) Single-phase full-bridge inverter.

V. RESULTS

A. Thermal Simulation

From the thermal simulation, the total losses for each switch are 8.03 W. Figure 14 shows the steady-state IGBT junction temperature. The junction temperature does not exceed the limit of 125°C, given by the IGBT datasheet, which demonstrates that the chosen heatsink is adequate for the circuit specification of switching frequency, voltage and current.

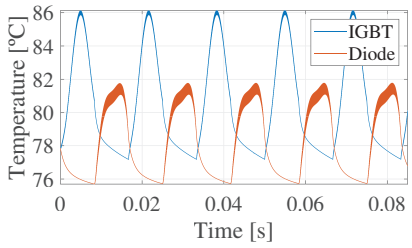


Fig. 14. Steady-state of the diode and IGBT junction temperature from simulation.

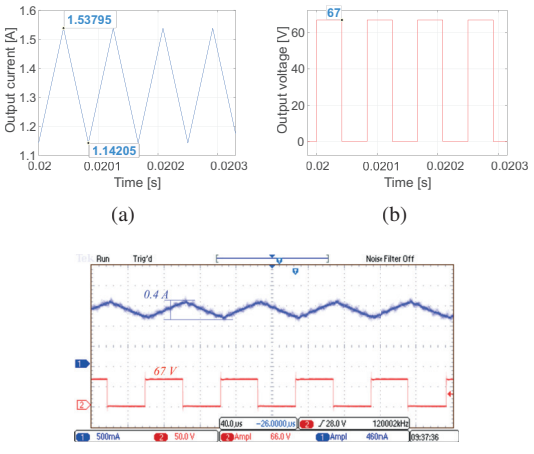
TABLE VI
Experimental Setup Parameters

Parameter	Step-down converter	Inverter	Cascaded converter
R_L	25 Ω	50 Ω	16 Ω
L	3.5 mH	5 mH	3.5 mH
V_{DC}	67 V	400 V	-
V_{DC1}	-	-	28 V
V_{DC2}	-	-	28 V
Switching frequency	12 kHz	12 kHz	10 kHz
Modulation index	0.5	0.6	0.8

Figure 14 also shows the temperature short-term cycling. It has a frequency of 60 Hz, as expected for an inverter. The IGBT and diode have an amplitude of 8.95°C and 6.04°C, respectively. In addition, the IGBT operates at a higher temperature compared to the diode, since the IGBT has a greater current effort in the inverter operation with a unity power factor.

B. Step-Down Converter Operation

The didactic platform operates as HB, as shown in Figure 2. Figure 15 shows the obtained experimental and simulation output voltage and current waveforms. The voltage and current waveforms are similar to the expected for the step-down converter [27]. The average output voltage is 33.5 V, both for experiment and simulation. The mean output currents are 1.34 A and 1.35 A, with a current ripple of 395.9 mA and 400.0 mA for simulation and experiment, respectively. The errors between the simulation and the experiment are lower than 1.5%.



(a) (b)

(c)

Fig. 15. Step-down converter: (a) output current simulation; (b) output voltage simulation; (c) experimental waveforms. CH1 - Output current. CH2 - Output voltage.

C. Single-Phase Full-Bridge Inverter Operation

The didactic platform is operating as a FB single-phase inverter. Figures 16.a and 16.c show the simulated and experimental output voltage and current waveforms. In addition, Figures 16.b and 16.d present the output voltage

spectrum of the simulation and the experiment.

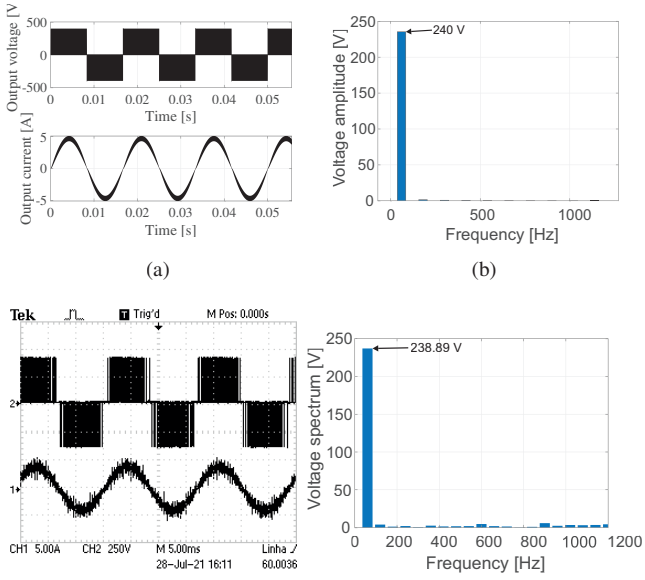


Fig. 16. Single-phase full-bridge inverter operation: (a) simulation output waveforms (b) simulation output voltage spectrum (c) Experimental output waveforms (d) Experimental output voltage spectrum. CH1 - Output current. CH2 - Output voltage.

In Figure 16.b, the inverter produces the expected fundamental voltage component, obtained by the input voltage multiplied by the modulation index [28]. The value obtained in the experiment is 238.89 V, which resulted in an error of 0.46%. The difference between the experimental and simulation results is related to the dead time and the IGBT voltage drop.

D. 5-Level Cascaded Converter Operation

This experiment has two main objectives: to validate the operation of the didactic platform as a cascaded converter and to test the galvanic isolation. The modules can only operate correctly as a cascaded converter if the galvanic isolation is well designed. Figure 17. shows the experimental and simulation output voltage, current and voltage spectrum.

The voltage and current waveforms are similar to the expected for the 5-level cascaded converter [28]. The fundamental voltage is 44.8 V for the parameters in Table VI [28]. However, in the simulation and experiment, 44.61 V and 42.93 V, are obtained respectively. The error of 4.17% in the experimental value is mainly associated with a voltage drop of the devices and dead-time. This effect is more significant in this experiment than in Section V.C, due to the lower dc-link voltage.

E. Experimental Validation of the Dc-Link Measurement Circuit

The single-phase full-bridge inverter configuration is used to test the dc-link measurement circuit. In this experiment, the dc-link measurement starts with no switching. Then, the module starts to switch. Thus, it is possible to observe if the converter switching affects the measurement. Figure 18.a shows the obtained result. Even when the switching and

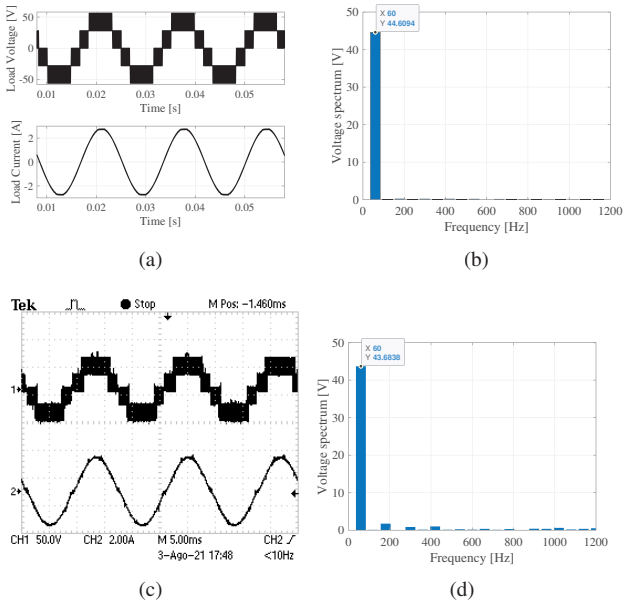


Fig. 17. 5-level cascaded converter operation: (a) simulation output waveforms (b) simulation output voltage spectrum (c) Experimental output waveforms (d) Experimental output voltage spectrum. CH1 - Output voltage. CH2 - Output current.

current circulation start in the inverter, the waveform of the voltage measurement does not change, thus validating the measurement circuit isolation.

Besides, the linearity of the measurement voltage circuit is verified by varying the dc-link voltage and measuring the output voltage V_m. Figure 18.b shows the obtained result. The theoretical curve obtained by (4) and the collected experimental points are very similar, with errors lower than 6%.

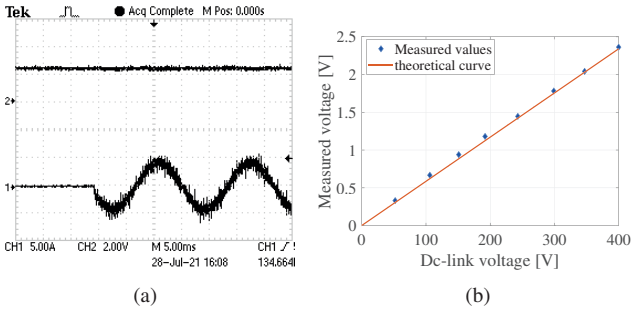


Fig. 18. (a) Voltage measurement output before and after the inverter starts the switching (b) Dc-link voltage vs. voltage measurement output. CH1 - Output current. CH2 - Measurement output voltage.

F. Experimental Validation of the Bypass Circuit

The bypass circuit validation uses the 5-level cascaded converter configuration. This experiment simulates a fault in a submodule of a converter of a multilevel system. Thus, a DSP signal connected to the reset input turns off one of the didactic platform modules. The same DSP signal is also connected to the bypass input and activates it. Figure 19 shows the output voltage, current and the bypass test signal.

Initially, in Figure 19, the modules are operating normally as the 5-level cascaded converter. One of the converters stops

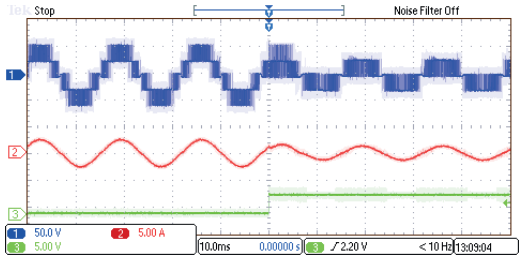


Fig. 19. Bypass experimental test wave forms. CH1 - Load voltage. CH2 - Load current. CH3 - test activation signal

switching when the test activation signal turns on. Then, the bypass signal turns on the relay. The time difference between the module shutdown and bypass activation is related to the time the relay needs to close its contact. When the relay is finally on, the module that stopped switching is short-circuited, and the system starts operating again, thus losing two voltage levels.

VI. CONCLUSIONS

This work presented the didactic platform design stages, including the design of the full-bridge cell, gate-driver, signals circuit, voltage measurement circuit and bypass circuit. The design focused on ensuring the galvanic isolation between the signal and power circuits, thus preventing interferences and protecting the DSP. Besides, a power supply circuit was designed to supply the modules independently from the dc-link and grid. A thermal evaluation of the heatsinks and IGBTs through simulation was also presented.

The didactic platform design validation was carried out through experiments involving some converter topologies: step-down converter, single phase inverter and cascaded converter. The didactic platform and the simulations presented similar results. Besides, the didactic platform can also be arranged in many other topologies. The tests with multilevel converters were limited to a 5-level cascaded converter, due to the number of assembled modules. Additional topology operation tests, as well as the expansion of more cells for the applications of multilevel converters, will be developed in the next steps of this work.

Furthermore, tests were performed on the dc-link measurement and bypass circuits. The dc-link measuring circuit proved to be well isolated by rejecting interferences even with the IGBT switching in high frequencies. In addition, the measurement presented linear behavior between its output and the dc-link voltage. Besides, the bypass circuit was able to short-circuit the disabled module, which allowed the system to continue operating at lower voltage levels, as expected for multilevel converter modules.

Finally, the didactic platform in the GESEP laboratory was successfully used. Components and PCBs for ten more didactic platform modules were ordered. They will assist in Power Electronics classes for undergraduate and graduate programs at the Federal University of Viçosa, the Federal Center for Technological Education of Minas Gerais (CEFET-MG) and in the research projects of the GESEP group. The complete design of the didactic modules and the PCB schematics is available for download on the GESEP website [29].

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