# **ON THE STUDY OF THE DYNAMICS OF THE ZVS THREE-PHASE DC/DC CONVERTER**

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*Abstract –* **This paper presents the theoretical analysis concerning the operating stages of the three-phase dc/dc converter associated with the hybridge rectifier, in order to obtain its dynamic model. The nonlinear instant model in state space form is obtained by the definition of a switching function** *q(t)***. From this model, an average nonlinear model is proposed, as well as a linearized model. The dynamic model, the controller design, and also experimental results obtained from a prototype of 6kW are presented.** 

*Keywords - Asymmetrical duty cycle, hybridge rectifier, three-phase dc/dc converter***.** 

# NOMENCLATURE



# I. INTRODUCTION

Nowadays, the main topology used in high power dc/dc conversion is the ZVS PWM Full Bridge converter [1] [2]. It

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is characterized by four switches operating in high frequency. Soft commutation can be obtained by using phase shift modulation or asymmetrical modulation, which preserves the simplicity and achieves high power density.

However, for higher power levels, the components face several stresses. As possible solutions, the parallelism of components or even converters can be applied. The parallelism of components increases the complexity of the compromise between the layout circuit and the thermal design. Besides that, one should consider that the dynamic and static current sharing problem limits its application. The parallelism of converters causes redundancy in the control circuits as well as in the number of power components and drivers, increasing global cost and size of the equipment.

A prominent alternative was proposed by Ziogas [3]. It uses a three-phase inverter coupled to a three-phase high frequency transformer and to a three-phase high frequency rectifier. The resulting advantages consist in the increase of the input and output current frequency, by a factor of three compared to the Full Bridge converter, lower rms current through power components and reduction of the cores.

Although it presents satisfactory advantages, soft commutation has not been achieved, which limits the switching frequency and the power density. Then, the use of the asymmetrical duty cycle [4] in the three-phase dc/dc converter was proposed [5], in order to provide the ZVS commutation of all switches for a wide load range. Nevertheless, the resulting topology suffers high conduction losses, since two series diodes conduct the load current.

It was stated in [6] that the use of the three-phase version of the hybridge rectifier, associated with the three-phase dc/dc converter employing asymmetrical duty cycle, improves the efficiency obtained with the same converter associated with the six-diode rectifier. Within this context, this paper fulfills the theoretical development of the proposed converter, focusing on its dynamic behavior.

## II. TOPOLOGY DESCRIPTION

The circuit of the three-phase dc/dc converter associated with the hybridge rectifier is shown in figure 1. According to the operating stages described in [6], three operational modes DMIN, DMED and DMAX are possible, in continuous conduction mode, as shown in figure 2, where  $I_0$ ' is the normalized output current. It must be mentioned that this converter must be designed to operate in mode DMIN only, or mode DMAX only, or modes DMIN and DMED.

 $\overline{a}$ 

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Fig. 2. Definition of modes DMIN, DMED and DMAX.

The equivalent circuits of stages 1, 2 and 3 for mode DMIN are shown in figures 3, 4 and 5, respectively.



Fig. 3. Equivalent circuit of the first stage in mode DMIN.



Fig. 4. Equivalent circuit of the second stage in mode DMIN.



Fig. 5. Equivalent circuit of the third stage in mode DMIN.

The equivalent circuits of stages 1, 2 and 3 in mode DMIN are shown in figures 6, 7 and 8, respectively.



Fig. 6. Equivalent circuit of the first stage in mode DMED.



Fig. 7. Equivalent circuit of the second stage in mode DMED.



Fig. 8. Equivalent circuit of the third stage in mode DMED.

The equivalent circuits in stages 1, 2 and 3 in mode DMAX are shown in figures 9, 10 and 11, respectively.



Fig. 9. Equivalent circuit of the first stage in mode DMAX.



Fig. 10. Equivalent circuit of the second stage in mode DMAX.



Fig. 11. Equivalent circuit of the third stage in mode DMAX.

The simplified equivalent circuits for each stage, considering unity transformer ratio, are shown in figure 12. Figures 12 (a), (b) and (c) represent the three operating stages of the converter for mode DMIN, as DMIN occurs when duty cycle is less than 0.33 and greater than zero. Figures 12 (d), (e) and (f) correspond to the operating stages of the converter for mode DMED, where DMED occurs when duty cycle is less than 0.66 and greater than 0.33. Figures 12 (g), (h) and (i) are the three operating stages of the converter for mode DMAX, where DMAX occurs when duty cycle is less than unity and greater than 0.66.



Fig. 12. (a),(b) and (c) equivalent operating stages in mode DMIN, (d), (e) and (f) equivalent operating stages in mode DMED and (g), (h) and (i) equivalent operating stages in mode DMAX.

Although they represent different stages in distinct operational modes, Figures 12 (a), (c) and (g) are the same because they represent a freewheeling or a transition stage

where there is no energy transference between source and load. Figures 12 (b), (f) and (d), (h) are similar because they represent energy transference or a transition stage where there is maximum or partial energy transference involving a single inductor. Figures 12 (e) and (i) are stages where there is full energy transference involving two output inductors.

### III. DYNAMIC ANALYSIS

Firstly, some variables used in this section must be defined as follows:  $L = L_1/3$  is the equivalent output filter inductance,  $i_l$  is the sum of the currents through the output inductances,  $C$  is the output filter capacitance,  $r_{SE}$  is the series resistance of the output capacitor,  $V_C$  is the voltage across capacitor *C*, *R* represents the load and  $V_{in}$  is the input voltage. In addition to this, *X* is defined as the vector representing the state variables and  $\overline{X}$  corresponds to the equilibrium point.

#### *A. Mode DMIN*

From the simplified equivalent circuits in figures 12 (a), (b) and (c), one can obtain the state space equation (1), valid for each stage in mode DMIN.

$$
\begin{bmatrix} i_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} \cdot \frac{R \cdot r_{SE}}{R + r_{SE}} & -\frac{1}{L} \cdot \frac{R}{R + r_{SE}} \\ \frac{1}{C} \cdot \frac{R}{R + r_{SE}} & -\frac{1}{C} \cdot \frac{1}{R + r_{SE}} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1+3q(t)}{6L} \\ 0 \end{bmatrix} V_{in} \quad (1)
$$

where the switching function  $q(t)$  is defined as follows:

$$
q(t) = \begin{cases} 1, & \text{if stage 2} \\ 0, & \text{if stage 1 or 3} \end{cases}
$$
 (2)

The equilibrium points are given by (3), and the eigenvalues can be real or complex, depending on the parameters of the circuit.

$$
\overline{X}^t = \left[\frac{1}{3R} \quad \frac{1}{3}\right] V_{in} q(t) \tag{3}
$$

A slight variation in currents and voltages results in a switching period. From the static gain, defining the average effective duty cycle  $d=D_{ef}(t)$  in (4), where  $R_d$  is related to the duty cycle loss caused by the series inductance  $L_d = L_{da} = L_{db} = L_{dc}$  (5), the nonlinear model in the average state space can be obtained in (6). The nonlinear nature of this expression is due to dependence of the effective duty cycle on the inductor current.

$$
d = D_{ef}(t) = \langle q(t) \rangle_{T_s} - \frac{R_d}{V_{in}} \langle i_L(t) \rangle_{T_s}
$$
 (4)

$$
R_d = f_s L_d \tag{5}
$$

$$
\begin{bmatrix} i_L \\ i_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} \cdot \frac{R \cdot r_{SE}}{R + r_{SE}} & -\frac{1}{L} \cdot \frac{R}{R + r_{SE}} \\ \frac{1}{C} \cdot \frac{R}{R + r_{SE}} & -\frac{1}{C} \cdot \frac{1}{R + r_{SE}} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{d}{L} \\ 0 \end{bmatrix} V_{in}
$$
 (6)

By equaling its derivative to zero, the equilibrium points of the nonlinear model are:

$$
\overline{X}^t = \left[\frac{1}{R + R_d} \quad \frac{R}{R + R_d}\right] d \cdot V_{in} \tag{7}
$$

#### *B. Mode DMED*

From the simplified equivalent circuits in figures 12 (d), (e) and (f), one can obtain the same state space equation obtained in (1), valid for mode DMED. However, the switching function  $q(t)$  is defined as follows:

$$
q(t) = \begin{cases} 1, & \text{if stage 1} \\ 0, & \text{if stage 2 or 3} \end{cases}
$$
 (8)

The equilibrium points are given by (9), and the eigenvalues can be real or complex, depending on the parameters of the circuit.

$$
\overline{X} = \frac{\left[\frac{V_{in}(1+3q(t))}{6R}\right]}{\frac{V_{in}(1+3q(t))}{6}}
$$
\n(9)

Using the average effective duty cycle (4), where  $R_d$  is related to the duty cycle loss caused by the series inductance  $L_d = L_{da} = L_{db} = L_{dc}$  (10), the nonlinear model in the average state space can be obtained  $(11)$ .

$$
R_d = 3f_s L_d \tag{10}
$$

$$
\begin{bmatrix} i_L \\ i_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} \cdot \frac{R \cdot r_{SE}}{R + r_{SE}} & -\frac{1}{L} \cdot \frac{R}{R + r_{SE}} \\ \frac{1}{C} \cdot \frac{R}{R + r_{SE}} & -\frac{1}{C} \cdot \frac{1}{R + r_{SE}} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{d}{L} \\ 0 \end{bmatrix} V_{in} \qquad (11)
$$

By equaling its derivative to zero, the equilibrium points of the nonlinear model are:

$$
\overline{X}^t = \left[\frac{1}{R + R_d} \quad \frac{R}{R + R_d}\right] d \cdot V_{in}
$$
\n(12)

*C. Mode DMAX* 

From the simplified equivalent circuits in figures 12 (g), (h) and (i), one can obtain the state space equation (13).

$$
\begin{bmatrix} i_L \\ i_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} \cdot \frac{R \cdot r_{SE}}{R + r_{SE}} & -\frac{1}{L} \cdot \frac{R}{R + r_{SE}} \\ \frac{1}{C} \cdot \frac{R}{R + r_{SE}} & -\frac{1}{C} \cdot \frac{1}{R + r_{SE}} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{q(t)}{1.5L} \\ 0 \end{bmatrix} V_{in} \quad (13)
$$

The switching function  $q(t)$  is defined as follows:

$$
q(t) = \begin{cases} 0, \text{ if stage 1} \\ 1/4, \text{ if stage 2} \\ 1, \text{ if stage 3} \end{cases}
$$
 (14)

The equilibrium points are given by (15), and the eigenvalues can be real or complex.

$$
\overline{X}^t = \begin{bmatrix} \frac{2}{3R} & \frac{2}{3} \end{bmatrix} V_{in} q(t) \tag{15}
$$

Using the average effective duty cycle in (4), where  $R_d$  is related to the duty cycle loss caused by the series inductance  $L_d = L_{da} = L_{db} = L_{dc}$  (16), the nonlinear model in the average state space can be obtained in (17).

$$
R_d = 3f_s L_d \tag{16}
$$

$$
\begin{bmatrix} i_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} \cdot \frac{R \cdot r_{SE}}{R + r_{SE}} & -\frac{1}{L} \cdot \frac{R}{R + r_{SE}} \\ \frac{1}{C} \cdot \frac{R}{R + r_{SE}} & -\frac{1}{C} \cdot \frac{1}{R + r_{SE}} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{d}{L} \\ 0 \end{bmatrix} V_{in} \qquad (17)
$$

By equaling its derivative to zero, the equilibrium points of the nonlinear average model can be obtained.

$$
\overline{X}^t = \begin{bmatrix} \frac{1}{R + R_d} & \frac{R}{R + R_d} \end{bmatrix} 2(1 - d) \cdot V_{in} \tag{18}
$$

#### *D. Linearization*

Defining the equilibrium points  $I_L$ ,  $V_C$  for a given *D*,  $V_{in}$ and *R*, and using the Jacobian concept, the linearized average state space equation can be found as (19).

$$
\begin{bmatrix}\n\dot{i}_L \\
\dot{v}_C\n\end{bmatrix} = \begin{bmatrix}\n-\frac{1}{L} \cdot \frac{R \cdot r_{SE}}{R + r_{SE}} & -\frac{1}{L} \cdot \frac{R}{R + r_{SE}} \\
\frac{1}{C} \cdot \frac{R}{R + r_{SE}} & -\frac{1}{C} \cdot \frac{1}{R + r_{SE}}\n\end{bmatrix} \begin{bmatrix}\n\dot{i}_L \\
\dot{v}_C\n\end{bmatrix} + \begin{bmatrix}\n\frac{V_m}{L} & \frac{D}{L} & \frac{-dV_m r_{SE}}{(R + r_{SE})(R + r_{SE})}\n\end{bmatrix} \cdot \begin{bmatrix}\n\Delta d \\
\Delta v_m \\
0\n\end{bmatrix}
$$
\n(19)

Solving the transference matrix, one can obtain the complete dynamic transfer functions of the three-phase dc/dc converter operating in mode DMIN.

$$
\frac{I_L(s)}{D(s)} = \frac{V_{in}}{R} \frac{(r_{SE} + R)C \cdot s + 1}{den(s)}
$$
(20)

$$
\frac{I_L(s)}{V_{in}(s)} = \frac{D}{R} \frac{(r_{SE} + R)C \cdot s + 1}{den(s)}
$$
(21)

$$
\frac{I_L(s)}{R(s)} = -D \frac{V_m}{R(R+R_d)} \frac{r_{SE}C \cdot s + 1}{den(s)}
$$
(22)

$$
\frac{V_0(s)}{D(s)} = V_{in} \frac{r_{SE}C \cdot s + 1}{den(s)}
$$
\n(23)

$$
\frac{V_0(s)}{V_{in}(s)} = D \frac{r_{se}C \cdot s + 1}{den(s)}
$$
\n(24)

$$
\frac{V_0(s)}{R(s)} = -DV_{in}\frac{(L - r_{SE}^2C) \cdot s + R_d - r_{SE}}{(R + R_d)(R + r_{SE})den(s)}
$$
(25)

where:

$$
den(s) = \left[ LC\left(\frac{r_{SE}}{R} + 1\right)s^2 + \left[r_{SE} + R_d\left(\frac{r_{SE}}{R} + 1\right)C + \frac{L}{R}\right]s \right]
$$
(26)

Following the same procedure used in mode DMED, one can obtain the same previous equations (20) to (26), except for *Rd*. Hence, a unified approach was defined for the converter operating in modes DMIN and DMED.

$$
R_d = \begin{cases} f_s L_d & \text{if DMIN} \\ 3f_s L_d & \text{if DMED} \end{cases}
$$
 (27)

As the converter presents an improved performance in modes DMIN and DMED [6], the linearization of DMAX is not analyzed here. However, for mode DMAX, the same procedure can be used, but the equations can not be described in a unified way.



Fig. 15. Duty cycle response in the nonlinear average state space (voltage: 10V/div; current: 10A/div; time: 500μs/div).

The developed linear model is valid only around a small neighborhood of the equilibrium points, since high order terms of the Taylor series were disregarded. However, the obtained model is useful in the design of an adequate controller.

## *E. Model Validation*

In order to prove the validity of the developed nonlinear model, some simulation tests were performed, using *Vin*=200V and load step from *R*=0.6Ω to *R*=0.38Ω. Figures 13 and 14 show the dynamic responses obtained from PSpice and from the nonlinear average model, under the same conditions and for the same load step, respectively. Figures 15 and 16 establish a comparison between simulation and experimental results of the dynamic response obtained with a duty cycle step (0.51 to 0.57), with  $V_{in}$ =300V and  $R=1\Omega$ . One can see that the obtained responses are almost the same, validating the accuracy of the developed model.

# IV. CONTROLLER DESIGN

As it can be seen, the resulting linearized model is analogous to the expressions of the Buck converter, as a similar controller can be used. Figures 17 shows the Bode diagram of the system, calculated from expressions (28) to (32), in modes DMIN and DMED, where there is a slight variation in the curves. Therefore only one controller can be used to control the system in regions 1 and 2. The parameters used in the tests are presented in table I.



Fig. 14. Load step response in the nonlinear average state space



Fig. 16. Duty cycle response in the nonlinear average state space (voltage: 10V/div; current: 10A/div; time: 500μs/div).

$$
G(s) = k_d \frac{\left(1 + \frac{s}{\omega_{za}}\right)}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}}
$$
(28)

$$
k_d = V_{in} \frac{R}{R + R_d} \tag{29}
$$

$$
\omega_{za} = \frac{1}{r_{SE}C} \tag{30}
$$

$$
\omega_0 = \sqrt{\frac{1}{LC} \frac{R + R_d}{R + r_{SE}}} \tag{31}
$$

$$
Q = \frac{R + R_d}{L + (R + r_{SE})R_dC + r_{SE}RC} \frac{1}{\omega_0}
$$
(32)

# **TABLE I Parameters used in the prototype.**



In order to maintain the output voltage constant under load variations, the following controller was designed and implemented: 2

$$
G_c(s) = \frac{\left(1 + \frac{s}{\omega_1}\right)^2}{\left(1 + \frac{s}{\omega_G}\right)\left(1 + \frac{s}{\omega_{2a}}\right)}
$$
(33)



where  $\omega_l$  is slightly smaller than  $\omega_0$  (natural resonant frequency of the system),  $\omega_{z}$  is the frequency of the zero generated by  $r_{SE}$ , and  $\omega_G$  is the pole frequency necessary to obtain the required crossover frequency  $(f_c < f_s/5)$ . Table II shows the parameters set of the controller. Figures 18 and 19 are the controller response and the open loop response of the system, respectively.

**TABLE II Controller parameters** 





## V. EXPERIMENTAL AND SIMULATION RESULTS

Using the experimental prototype developed with the parameters in table I, some results were obtained in order to verify the closed loop response of the converter.

Figures 20 and 21 represent simulation results obtained from the closed loop controller developed above, associated with the nonlinear average model of the converter. As it can be seen, an optimum voltage regulation is obtained from a 50% load step  $(I_0=3x20A$  to  $I_0=3x10A)$ . Figure 22 corresponds to simulation results obtained from an input voltage step  $(V_{in} = 400V)$  to  $V_{in} = 421V$ ). It can be seen that a satisfactory voltage regulation is verified. Since the input voltage transients are not so abrupt in practice, the controller is supposed to present adequate response.



Fig. 20. Load step response of the closed loop system obtained by simulation of the nonlinear average model (current through inductor  $L_1$ ).



Fig. 21. Load step response of the closed loop system obtained by simulation of the nonlinear average model (output voltage).



Fig. 22. Input voltage step response of the closed loop system obtained by simulation of the nonlinear average model (output voltage and current through  $I_1$ <sub>2</sub>).

Figure 23 shows experimental results on the dynamic behavior of the output inductor current during a load step near to rated condition ( $V_0$ =60V and  $I_0$ =3x20A to  $I_0$ =3x30A). The dynamic response is satisfactory, since current overshoot is low and the transient time is short, implying reduced stresses in semiconductors during large transients.

#### VI. CONCLUSION

This paper has presented a dynamic analysis of the threephase dc/dc converter with asymmetrical duty cycle. As expected, the obtained dynamic model is equivalent to the Buck converter model, although it includes some real characteristics such as the presence of leakage inductances and the use of three output inductors.

The developed model was studied by simulation and step response under load variations. A linearized model was obtained, so that a conventional controller can be implemented.

Using a prototype of 6kW, experimental closed loop responses were obtained. The results have shown satisfactory agreement with the mathematical model, validating the adopted design procedure.



Fig. 23. Closed loop system response (Current through inductor  $L_1 - 10A/div$ ; 10ms/div, Output Voltage – 20V/div; 10ms/div).

 The proposed method can be easily extended to the study of the dynamic behavior of the three-phase dc/dc converter associated with other rectifier topologies [5] [7].

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#### **REFERENCES**

- [1] I. Barbi, W.A. Filho, "A Non-Resonant Zero Voltage Switching Pulse Width Modulated Full-Bridge DC/DC Converter," *in Proc. IECON*, pp 1051-1056, 1990.
- [2] R.L. Steiengerwald, K.D.T. Ngo, "Full-Bridge Lossless Switching Converter," *U.S. Patent 4864479*, Sept 5, 1989.
- [3] P.D. Ziogas, A.R. Prasad, S. Manias, "Analysis and Design of A Three Phase Off-Line DC-DC Converter with High Frequency Isolation," *in Proc. IAS*, pp. 813- 820, 1988.
- [4] N. Mohan, P. Imbertson, "Asymmetrical Duty Cycle Permits Zero Switching Loss in PWM Circuits with No Conduction Loss Penalty," *IEEE Transactions on Industry Applications*, vol. 29, no 1, pp. 121-125, Jan/Feb 1993.
- [5] D.S. Oliveira Jr, I. Barbi, "A Three-Phase ZVS PWM DC/DC Converter with Asymmetrical Duty Cycle for High Power Applications", *IEEE Transactions on Power Electronics*, pp. 354-360, Mar/Apr 2005.
- [6] D.S. Oliveira Jr., I. Barbi, "A Three-Phase ZVS PWM DC/DC Converter with Asymmetrical Duty Cycle Associated with A Three-Phase Version of the Hybridge Rectifier", *IEEE Transactions on Power Electronics*, pp. 370-377, Mar/Apr 2005.
- [7] D.S. Oliveira Jr., F.L.M. Antunes, "A Novel Modulation Technique Applied to The Three-Phase ZVS PWM DC/DC Converter Associated with A Double-Wye Connected Rectifier, Delta Primary" *in International Conference on Industrial Applications*, Joinville, Brazil, pp. 852-856, 2004.

## **BIOGRAPHIES**

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