

# A LOW POWER VOLTAGE SAG COMPENSATOR

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**Abstract** – The increasing use of voltage variation sensitive loads in industrial applications nowadays has brought a real concern about interruption costs and damages in complex production lines. This paper presents a power-electronic-based device which compensates voltage sags, restoring the load voltage to acceptable values through a series connected injection transformer. The ratings and power requirements of a low-power voltage sag compensator, also known as Dynamic Voltage Restorer (DVR) are derived, as well as its deadbeat control algorithm implemented in a Digital Signal Processor (DSP). Finally, simulation and experimental results of a 5-kVA prototype are presented.

**Keywords** - DSP controlled converter, Dynamic Voltage Restorer (DVR), Power Quality, Voltage Sags.

## I. INTRODUCTION

Disturbances within the power systems can affect sensitive devices present in most of the production lines. According to [1], a Voltage Sag is defined as a decrease in the rms voltage magnitude at the fundamental frequency and duration from 0.5 cycles to 1 min. Voltage sags are commonly caused by faults on adjacent lines of the power system or by large motors startup, and may cause misoperation or fails. Typical magnitudes are between 0.1–0.9 per unit (p.u.). A Voltage Swell is defined as an increase in the rms voltage magnitude at the fundamental frequency and duration from 0.5 cycles to 1 min, which may lead sensitive devices to be permanently damaged. Typical magnitudes are between 1.1 and 1.8 p.u.

The interruption costs of industrial processes depend on the load sensibility and on the process itself. Typically a four-hour outage costs US\$74,835.00, while a voltage sag of 0.1 p.u. or 0.2 p.u. which lasts only 15 cycles may cost US\$7,694.00 [2], proving that these power quality phenomena are real concerns nowadays in industrial facilities.

In order to mitigate these problems, a possible solution [10], based on power-electronic devices is the Dynamic Voltage Restorer (DVR), which is series connected to the load by means of injection transformers and restores the load voltage magnitude during voltage sags. DVRs add to the

mains voltage a pre-defined voltage synthesized by a power inverter in order to keep the load voltage within acceptable values. The first DVR was installed by Westinghouse in 1996 and since then a lot of industrial installations employ this power quality device to mitigate voltage sags [12].

The main advantage of a DVR is the needless of storing the energy to supply full load, which is the case for Uninterruptible Power Supplies (UPSs). A DVR injects only the difference between the remaining mains voltage and the reference voltage during voltage sags or swells. However, DVRs are not designed to work when an outage occurs, as UPSs devices do, which is the major disadvantage of the adopted solution.

This paper describes the design of a DVR that compensates voltage sags. The control technique, phase-locked-loop (PLL) algorithm, voltage reference generation and power converter modeling are discussed. Simulations results of the device in a power utility are also presented. Finally, the proposed approach is implemented in a 5-kVA/220V prototype with a Digital Signal Processor (DSP) based control, and its validity is evaluated through experimental results. Preliminary results of voltage harmonic compensation are also presented.

## II. TOPOLOGY

The single-phase diagram of the DVR is shown in Fig. 1. A pulse-width-modulated (PWM) full bridge single-phase inverter is connected to a LC filter and a single-phase series transformer. Three equal arrangements allow zero sequence voltage injection.

It is important to note that the energy required to charge DC-link capacitors comes from the mains where the device is installed [11], by means of a non-controlled three-phase bridge rectifier and a delta-ye transformer. As a consequence, in order to avoid voltage collapse during voltage sags, charging limitation is introduced through resistors in the output of the AC/DC converter. On the other hand, during voltage swells, a DC/DC converter and discharging resistors are operated to limit DC-link voltage and to satisfy load voltage specifications.

It is well known that the DVR shall not interfere in the protection coordination of the considered load. Moreover, when faults as short-circuits occur inside the load, the DVR must be isolated from the mains circuit in order to protect its power electronics and other internal sensitive devices. Thus, fast solid-state switches and normally closed contactors are

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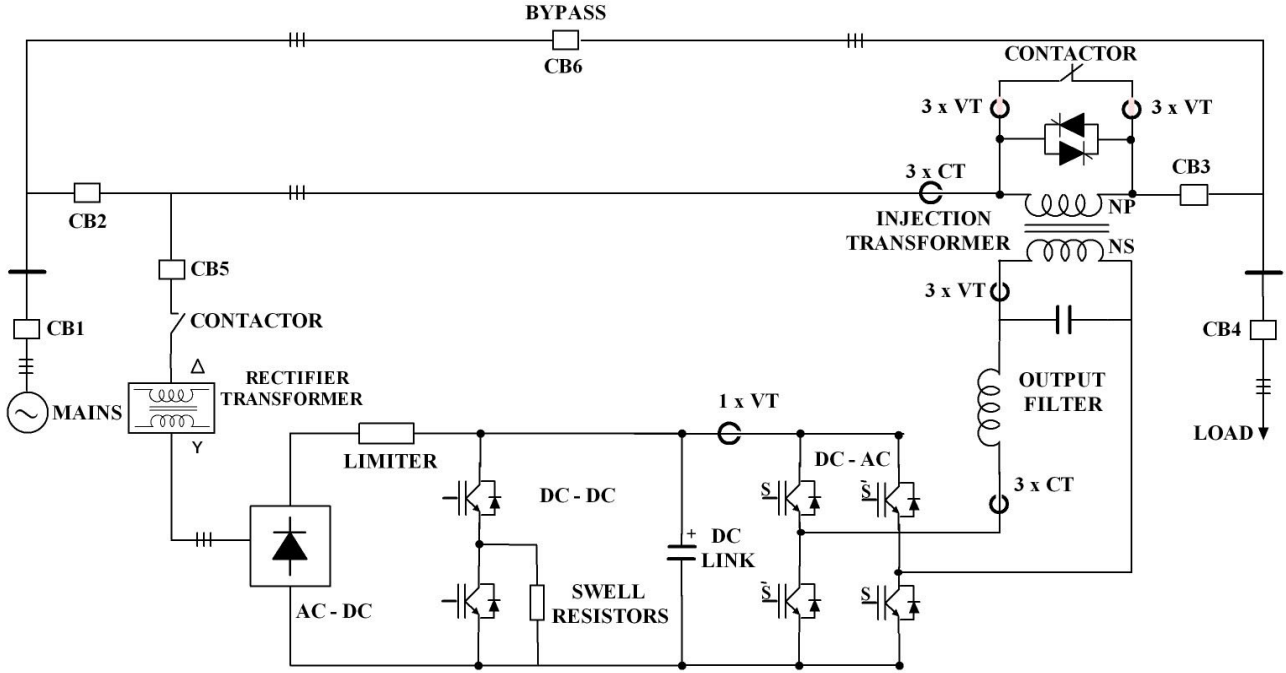


Fig. 1. Single-phase diagram of the DVR

placed in parallel with the injection transformer's load side windings. It was foreseen the inclusion of auxiliary circuit breakers in order to allow DVR replacement or maintenance without interrupting the load.

Fig. 1 also shows Current and Voltage Hall-Effect transducers (CT and VT, respectively) for control and monitoring purposes.

### III. DVR DESIGN [3]

#### A. DVR Performance Specification

The proposed DVR can compensate a maximum single-phase voltage sag magnitude  $v_{sag1\phi} = 0.5pu$ , maximum three-phase voltage sag magnitude  $v_{sag3\phi} = 0.65pu$ , maximum voltage sag duration  $\Delta t = 500ms$  for a maximum three-phase load apparent power  $S_{3\phi load} = 10 kVA$  and nominal line-to-line rms voltage  $v_{L-L} = 220V$ .

Assuming the load power factor equal to unity and that the injected voltage is in phase with the mains voltage, the maximum power transfer from the DVR to the load occurs for the maximum three-phase voltage sag specification, where the relation between the DVR apparent power and load apparent power is  $S_{DVR} / S_{3\phi load} = 0.35$ .

#### B. Transformer and Inverter Ratings

Taking the load side as the primary and the inverter side as the secondary of the injection transformer, its turns ratio is derived from the relationship between the peak values of the minimum inverter voltage, that is approximately equal to the minimum DC-link voltage  $v_{CCMIN}$ , and the maximum rms primary voltage of the DVR  $v_{DVR}$ :

$$\frac{N_S}{N_P} \cong \frac{v_{CCMIN}}{(1+k_L) \cdot \sqrt{2} \cdot v_{DVR}} \quad (1)$$

where  $k_L$  is the inductor voltage drop in p.u. assuming the inverter voltage as base,  $N_P$  is the primary turns number and  $N_S$  is the secondary turns number. Writing  $v_{DVR}$  as a function of the maximum single-phase voltage dip  $\alpha_{1\phi}$ :

$$\frac{N_S}{N_P} = \frac{v_{CCMIN}}{0.8165 \cdot v_{L-L} \cdot \alpha_{1\phi} \cdot (1+k_L)} \quad (2)$$

The inverter current is equal to the secondary current of the injection transformer plus the filter capacitor current:

$$i_{inv} = \frac{0.8165 \cdot (1+k_C) \cdot (1+k_L) \cdot v_{L-L} \cdot i_{LOAD} \cdot \alpha_{1\phi}}{v_{CCMIN}} \quad (3)$$

where  $k_C$  is the capacitor current in p.u. considering the inverter current as base and  $i_{LOAD}$  is the load current. Multiplying the inverter current by the inverter single-phase voltage, the three-phase inverter apparent power may be written as:

$$S_{inv3\phi} = \frac{S_{3\phi load} \cdot \alpha_{1\phi} \cdot (1+k_C) \cdot (1+k_L)}{\gamma} \quad (4)$$

$$\gamma = \frac{v_{CCMIN}}{v_{CCMAX}}, \quad 0 \leq \gamma \leq 1 \quad (5)$$

where  $\gamma$  is the maximum DC link voltage dip and  $v_{CCMAX}$  is the maximum DC-link voltage.

#### C. DC-Link Capacitor Derivation

The DC-link capacitor bank energy is given by:

$$\varepsilon = 1/2 \cdot C \cdot \Delta v_{CC}^2 \quad (6)$$

$$\varepsilon = 1/2 \cdot C \cdot v_{CCMAX}^2 \cdot (1-\gamma^2) \quad (7)$$

The capacitor dimensioning is based on the maximum injected active power of the DVR that occurs for the three-phase voltage sag case:

$$\varepsilon = P_{load} \cdot \alpha_{3\phi} \cdot \Delta t \quad (8)$$

where  $P_{load}$  is the load active power and  $\alpha_{3\phi}$  is the maximum three-phase voltage dip. Substituting (7) into (8):

$$C = \frac{2 \cdot P_{load} \cdot \alpha_{3\phi} \cdot \Delta t}{v_{CCMAX}^2 (1 - \gamma^2)} \quad (9)$$

#### D. Output Filter Design

The inverter PWM filter is designed as a second order LC-low-pass filter whose resonance frequency is approximately one decade below the switching frequency and one decade above the fundamental frequency. Setting  $k_L = 0.1$ ,  $k_C = 0.1$ , the fundamental frequency  $f = 60\text{Hz}$  and the resonance frequency of the filter  $f_r = 1\text{kHz}$ , the filter inductance is  $L_F = 3.947\text{mH}$ . Consequently, the PWM filter capacitance is equal to  $C_F = 6.417\mu\text{F}$ .

#### E. Final Dimensioning Considerations

As can be noted from (1), (4) and (9), the injection transformer turns ratio, the inverter apparent power and the DC-link capacitor are strictly related to  $\gamma$ . For instance, fig. 2 shows that a small value of  $\gamma$  implies smaller DC-link capacitor size and higher inverter KVA ratings. Thus, there must be a compromise solution considering these three variables.

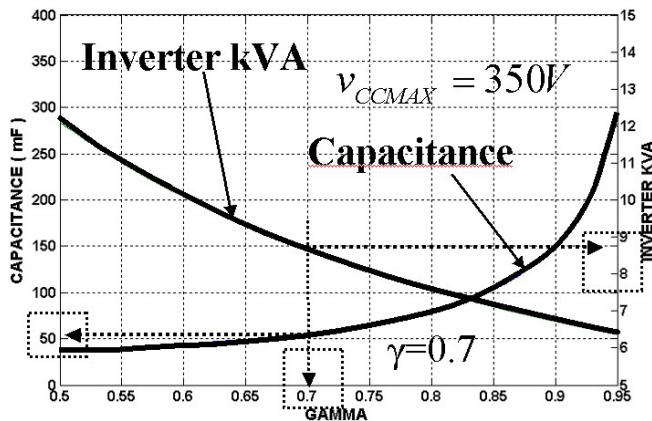


Fig. 2. Inverter KVA rating and DC-link capacitance as function of  $\gamma$  (gamma)

Assuming  $P_{load} = 10\text{ kW}$ ,  $v_{CCMAX} = 350\text{V}$ ,  $\gamma = 0.7$ ,  $k_L = k_C = 0.1$ ,  $\alpha_{1\phi} = 0.5$ ,  $\alpha_{3\phi} = 0.35$  and  $v_{L-L} = 220\text{V}$ , the injection transformer turns ratio is  $N_s/N_p \approx 2.50$ , the DC-link capacitance is  $C = 56\text{mF}$  and  $S_{INV3\phi} = 8.642\text{ kVA}$ .

The apparent power of a single-phase transformer is  $S_{TR1\phi} = 1.67\text{ kVA}$ . As stated in [4], depending on DVR starting instant and on the transformer load, the flux linkage can be as much as the double of its maximum rated value for the worst case and the transformer may saturate. Thus, in order to avoid saturation, the apparent power of each transformer shall be multiplied by two, resulting in  $S_{TR1\phi} = 3.33\text{ kVA}$ . This solution is cost-effective for low-power DVRs[4].

As the proposed DVR is designed to compensate voltage harmonics in steady-state, it will be always connected to the load, except when faults as short-circuits occur in the grid. The disadvantage of continuous operating mode is essentially the inverter switching losses. The main advantages are speed of response of the device, since there is no standby (idle) mode. The choice of steady-state DVR with harmonic

compensation can be determined by the load sensibility, which is analyzed during project development.

## IV. CONTROL SYSTEM

#### A. Control algorithm

Fig. 3 and 4 show the block diagrams of the discrete time control algorithm of the DVR under analysis. The algorithm is essentially composed by two blocks: Reference Generation and Phase Locked Loop (PLL) Block and Voltage Control Block.

Referring to fig.3, where  $k$  is the  $k$ -th sample, the PLL reference voltage  $v_{PLL}(k)$  is compared to the mains voltage  $v_{MAINS}(k)$  in order to determine the input reference voltage of the voltage loop block  $v_{REF}(k)$ , that is, the voltage to be synthesized by the power inverter.

The Voltage Control Block is based on a multiloop control technique, in which an external Voltage Loop is connected to a faster Current Loop. The main advantage of this structure is that the current loop provides intrinsic overload protection by limiting the inductor current.

Since the tracking error after a certain number of modulation periods must be zero and a simple design and implementation as well as a fast dynamic response is always achievable, deadbeat response controllers are adopted in current and voltage loops (fig.4). However, a reasonable model of the system under control must be employed for a good performance of digital predictive controllers [6],[7].

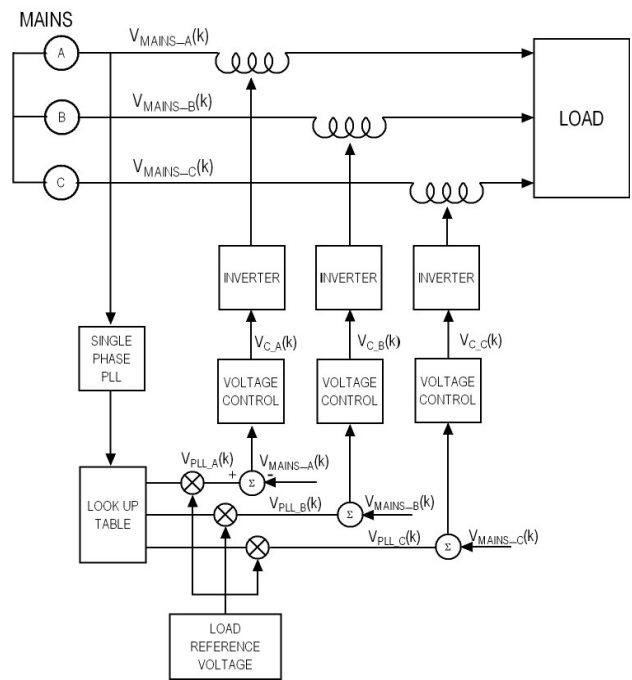


Fig.3. Reference Generation

The output of the voltage controller establishes the filter inductor current reference  $i_{L,REF}(k)$ . The current controller is responsible for tracking the reference current, forcing the error to zero. A zero-order hold (ZOH) sampling of the normalized output of the current loop is provided and applied to the PWM modulator to synthesize the inverter voltage  $v_c(k)$ .

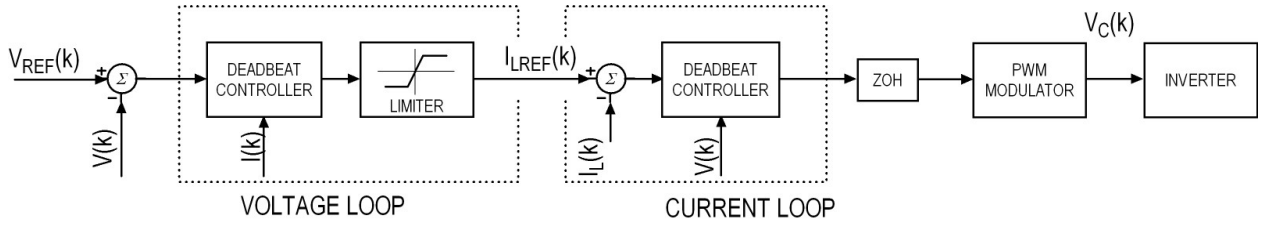


Fig. 4. Voltage Control Block

### B. Reference Generation and Phase-locked-loop (PLL)

The magnitude and the phase angle of the reference voltage  $v_{PLL}(k)$  are generated by means of an internal normalized sinusoidal signal obtained from a look up table. The frequency of  $v_{PLL}(k)$  is given by the PLL.

The Phase Locked Loop (PLL) is based on a rising zero-crossing detection of the sinusoidal reference to generate synchronization signals with the same frequency of the mains voltage. The algorithm is implemented in a discrete-time model and consists in forcing the first sample of the next mains period to be coincident with the zero crossing of the internal reference voltage  $v_{PLL}(k)$ , by inserting equally spread samples (fig.5).

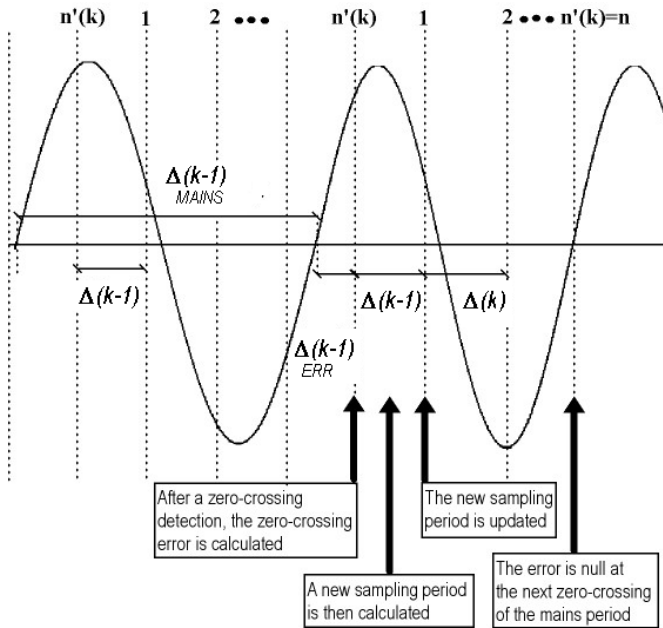


Fig. 5. PLL algorithm graphical description

At the first time the algorithm runs, it detects the first zero-crossing and calculates the voltage reference phase angle. From the second zero-crossing on, as a new detection occurs, a new computation of the sampling period  $\Delta(k)$  is made, taking into account the previous mains period  $\Delta_{MAINS}(k-1)$ , the last cumulative number of samples  $n(k-1)$ , the total number of samples per mains period  $n$  and the current zero-crossing error  $\Delta_{ERR}(k)$ , according to (10).

$$\Delta(k) = \frac{\Delta_{MAINS}(k-1) - \Delta_{ERR}(k) - \Delta(k-1)}{2n - n'(k-1) - 1} \quad (10)$$

It shall be noted that the zero crossing calculation is based on a linear interpolation, since a sinusoidal signal is approximately linear near zero-crossing region.

The PLL and reference generation algorithms are applied only for a reference phase A. The voltage references for the remaining phases (B,C) are calculated by displacing a pre-defined number of samples in order to obtain a balanced three-phase system, i.e., load voltage unbalances compensation can be achieved. Load voltage harmonic and sag-swell compensation is implemented by calculating  $v_{REF}(k)$ .

The Reference Generation and PLL algorithms have been improved taking into account the positive sequence and long term variation (e.g. slow voltage increase due to light load conditions) of the mains voltages [13],[14] and will be implemented in the next prototype.

### C. Current and Voltage Loops

Considering the averaged model of fig.6, the inverter is represented by a controlled voltage source. The inverter voltage and output current are constant between two sampling periods [7], that is, a zero-order hold (ZOH) sampling of the PWM reference voltage is provided. Assuming that the sampling frequency is much higher than the resonance frequency of the output filter, the control system discrete time dynamic equations are:

$$x(k+1) = \Phi \cdot x(k) + \Gamma_1 \cdot v_C(k) + \Gamma_2 \cdot i(k) \quad (11)$$

$$y(k) = D \cdot x(k) \quad (12)$$

where:

$$\Phi = \begin{bmatrix} 1 & \Delta(k)/C_F \\ -\Delta(k)/L_F & 1 \end{bmatrix} \quad (13) \quad \Gamma_1 = \begin{bmatrix} \Delta(k)/C_F \\ 0 \end{bmatrix} \quad (14)$$

$$\Gamma_2 = \begin{bmatrix} 0 \\ \Delta(k)/L_F \end{bmatrix} \quad (15) \quad x(k) = \begin{bmatrix} v(k) \\ i_L(k) \end{bmatrix} \quad (16) \quad D = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad (17)$$

where  $v(k)$  is  $k$ -th output voltage at the inverter side,  $i_L(k)$  is the  $k$ -th filter inductor current and  $i(k)$  is the  $k$ -th load current at the inverter side of the DVR.

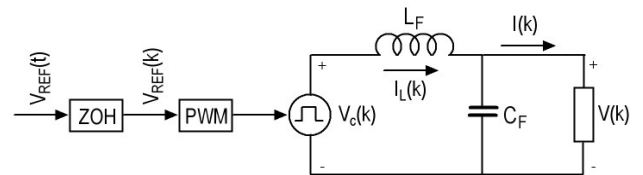


Fig. 6. Inverter averaged model

Substituting (13)-(16) into (11), the inverter voltage and inductor current are described by (18) and (19), respectively:

$$v_C(k) = \frac{i_L(k+1) - i_L(k)}{\Delta(k)} \cdot L_F + v(k) \quad (18)$$

$$i_L(k) = \frac{v(k+1) - v(k)}{\Delta(k)} \cdot C_F + i(k) \quad (19)$$

The control technique consists in making the current error equal to zero by the end of the following sampling period, that is:

$$i_L(k+1) = i_{LREF}(k) \quad (20)$$

$$v(k+1) = v_{REF}(k) \quad (21)$$

Substituting (20) into (18), considering the output voltage samplings as disturbances in the current loop and applying the z-transform to the resultant equation, the closed loop poles in z-plane are [8]:

$$z_{1,2} = \frac{1}{2} \pm \frac{j}{2} \sqrt{4\alpha - 1} \quad (22)$$

where  $\alpha$  is a constant that represents a mismatch between the modeled and real filter inductances. As can be seen in (22), deadbeat response is not achieved in the current loop, since the closed loop poles are not at the origin. Moreover, if  $\alpha = 1$ , a low-order frequency equal to  $1/6$  of the sampling frequency will be present in the inductor filter current and the current controller response is critically stable [8]. As a consequence, care must be taken when designing the output LC filter and detuning shall be considered as an option to avoid undesirable resonances.

As a fixed number of samples per cycle of the mains voltage is adopted [5], the sampling frequency, which is equal to the switching frequency, is not constant in order to achieve synchronization. However, since the sampling period is updated every mains cycle in the control loops and the line frequency does not change significantly, the controller dynamic response is not affected.

## V. SIMULATION RESULTS

The DVR control system was simulated with PSIM (v.5.01) for a two-phase voltage sag to 58% (remaining voltage) with 17.5% of the nominal load current for a resistive load and simulation parameters of Table 1.

TABLE 1

DVR simulation parameters

Mains Voltage Harmonic Content: 3 <sup>rd</sup> (4%); 5 <sup>th</sup> (3.7%); 7 <sup>th</sup> (2.77%); 9 <sup>th</sup> (1.25%)	
Mains voltage phase-to-neutral magnitude	127V <sub>RMS</sub>
Mains equivalent impedance	$\cong 5\%$
Load current percentage	17.5%
DC-Link Voltage	350V
Output filter inductance	5mH
Output filter capacitance	7.5 $\mu$ F
Switching frequency	6.667kHz
Inverter Deadtime	4.3 $\mu$ s
Reference current limit	6.3A
Series transformer turns ratio (Ns/Np)	2.51
Series transformer pri.winding leakage inductance *	0.0667 mH
Series transformer sec.winding leakage inductance*	0.1234 mH
Series transformer magnetizing inductance	3.8411H
Series transformer pri.winding resistance *	56.6m $\Omega$
Series transformer sec.winding resistance *	44.24m $\Omega$

\* Referred to primary (load) side

Referring to section III.D, the filter inductance, switching frequency and the filter capacitor were modified during project development.

The PLL and reference generation block was represented by a sinusoidal, 60Hz voltage-source. Fig. 7 and fig. 8 show the mains and load voltages, respectively.

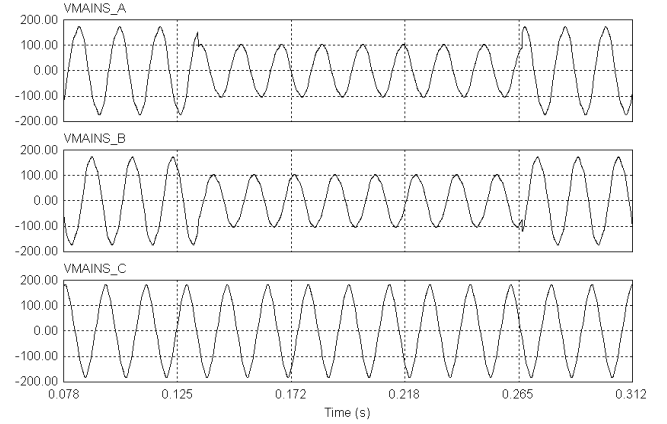


Fig. 7. Two-phase voltage sag to 58% (simulation), mains voltages. Phase A (top), phase B (center), phase C (bottom)

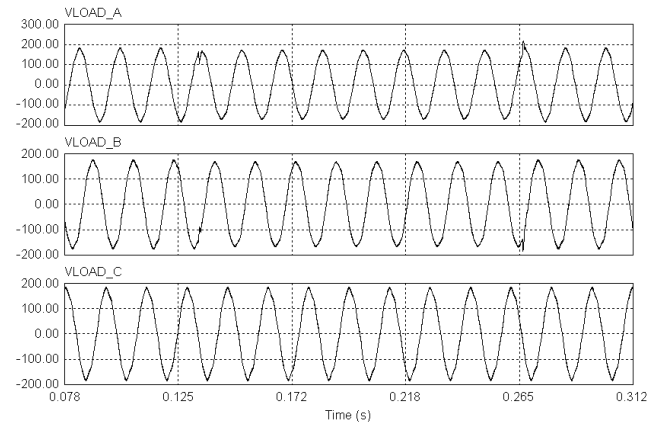


Fig. 8. Two-phase voltage sag to 58% (simulation), load voltages. Phase A (top), phase B (center), phase C (bottom)

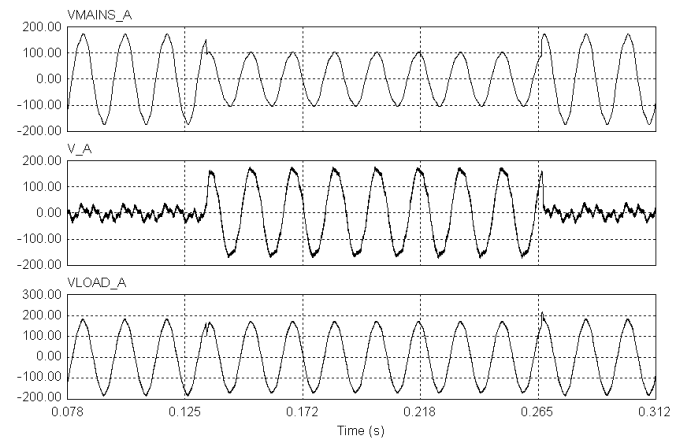


Fig. 9. Two-phase voltage sag to 58% (simulation), phase A. Mains Voltage (top), Injected Voltage referred to inverter side (center), Load Voltage C (bottom)

The DVR injected voltage can be seen in fig. 9 (center). It is important to note that in steady-state the DVR compensates voltage harmonics with relatively low active power requirements when compared to the voltage sag interval of fig. 9.

In Fig. 10, current and control loops behavior during voltage sags is evaluated. It can be observed that the controllers have reasonable tracking performance with the presence of voltage harmonic distortion and even with low load current levels, when inductor current ripple is quite high. Further improvements on control are under implementation.

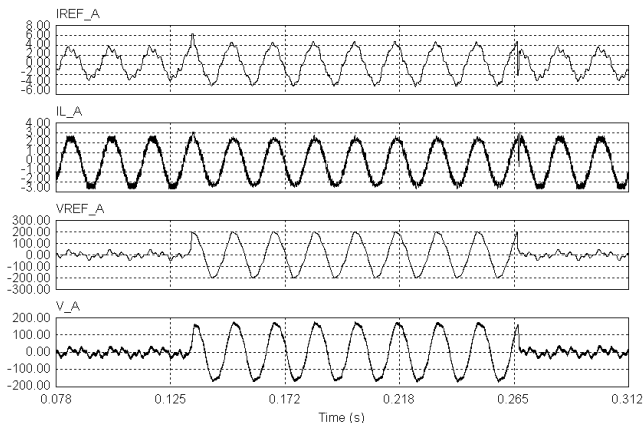


Fig. 10 . Control loop during voltage sag to 50% (simulation). From top to bottom: Reference current, Inductor current, Output capacitor reference voltage, Output capacitor voltage

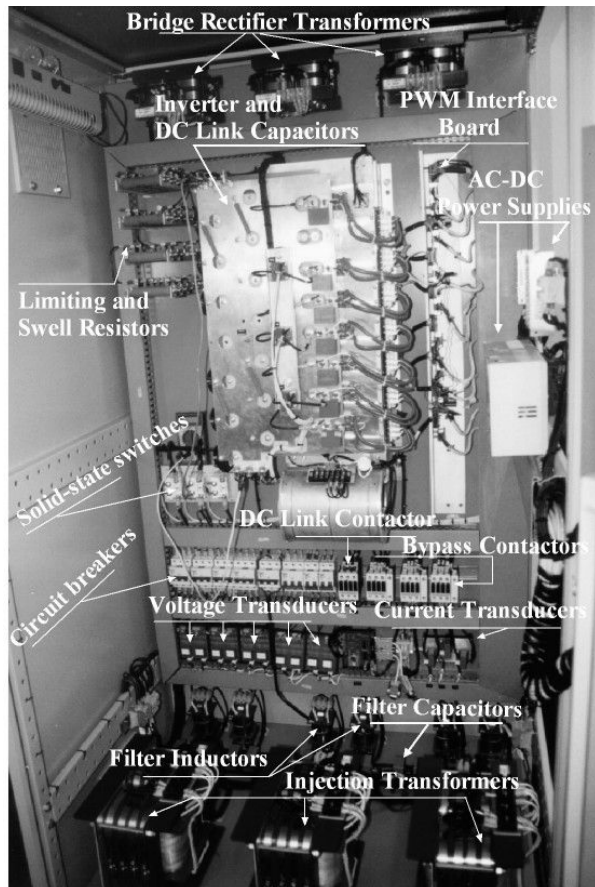


Fig. 11. 5kVA/220V-DVR-prototype

## VI. EXPERIMENTAL RESULTS

The control algorithm was implemented in a 16-bit fixed-point Analog Devices ADSP21992 DSP in the 5-kVA/220V prototype of fig. 11.

The prototype was tested with parameters of Table 1 for a two-phase voltage sag to 58%. Voltage sags were generated by using 0.05 p.u. series resistors in the mains circuit and by inserting 0.075 p.u. parallel resistors for voltage sags., taking as base the line-to-neutral load voltage and the load current.

Fig. 12 and fig. 13 show the mains and load voltages, respectively, obtained with differential oscilloscope probes. The injected voltage during voltage sags and steady-state for Phase A can be noted in Fig. 14.

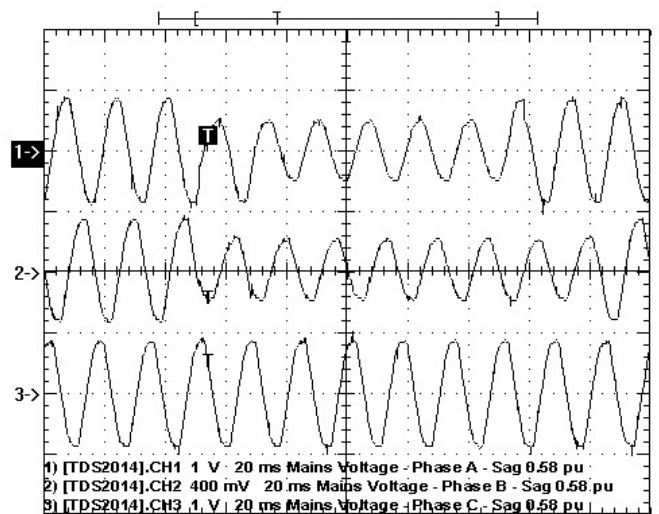


Fig. 12 . Mains Voltages – Two-phase voltage sag to 58% (measured). Top: Phase A, Center: Phase B, Bottom: Phase C. Time Scale: 20ms. Voltage Scale: 200V/div

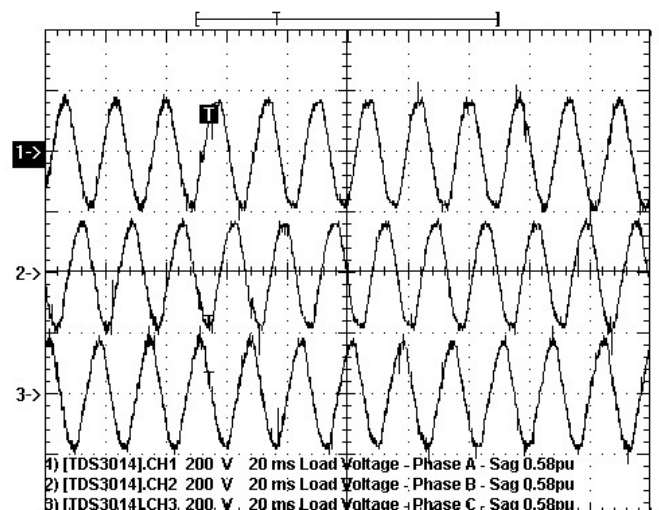


Fig. 13 . Load Voltages – Two-phase voltage sag to 58% (measured). Top: Phase A, Center: Phase B, Bottom: Phase C. Time Scale: 20ms. Voltage Scale: 200V/div



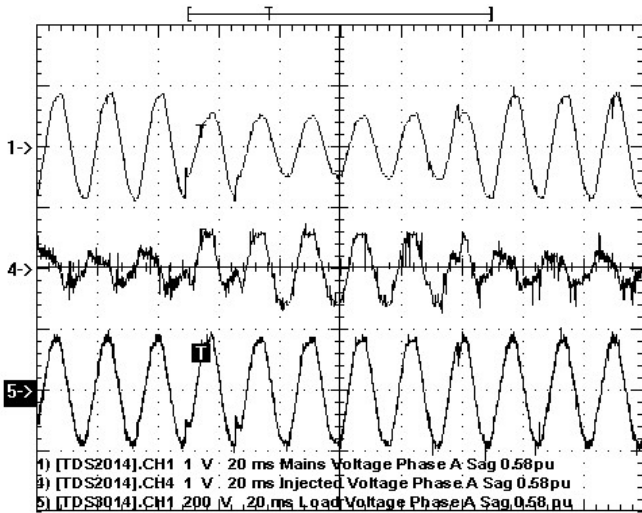


Fig. 14 . Two-phase voltage sag to 58% (measured), phase A. Top: Mains Voltage, 200V/div. Center: Injected Voltage referred to inverter side, 270V/div. Bottom: Load Voltage, 200V/div. Time Scale: 20ms

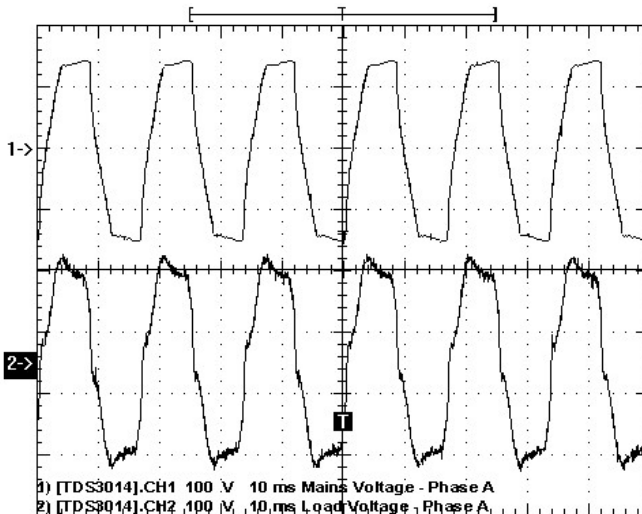


Fig. 15 . Voltage harmonic compensation. Mains Voltage (top) and Load Voltage (bottom). Time Scale: 10ms. Voltage Scale: 100V/div

The performance of the device on voltage harmonic compensation during steady-state is evaluated by means of a non-linear load connected to the mains before the DVR to distort the line voltage. The Total Harmonic Distortion (THD) [9] of the mains voltage is 14.64% (Fig.15) and the fundamental amplitude is equal to 161.95V (peak). The THD of the load voltage is 14.83%, and the 60Hz amplitude is 176.57V (Fig.16). These results show that the DVR does not work properly for harmonic voltage compensation, since the control loop still shall be improved, as stated before. However, as can be seen in Fig. 12 and fig. 13, it compensates voltage sags satisfactorily.

The efficiency  $\eta$  of the device is evaluated by (23) when the DVR imposes zero voltage on the series injection transformer:

$$\eta = \frac{P_{LOAD}}{P_{MAINS}} \quad (23)$$

where  $P_{LOAD}$  is the load active power in W and  $P_{MAINS}$  is the mains active power. For load currents between 19.32% and

46.87% of the nominal current, the measured efficiency was between 95.62% and 95.8%.

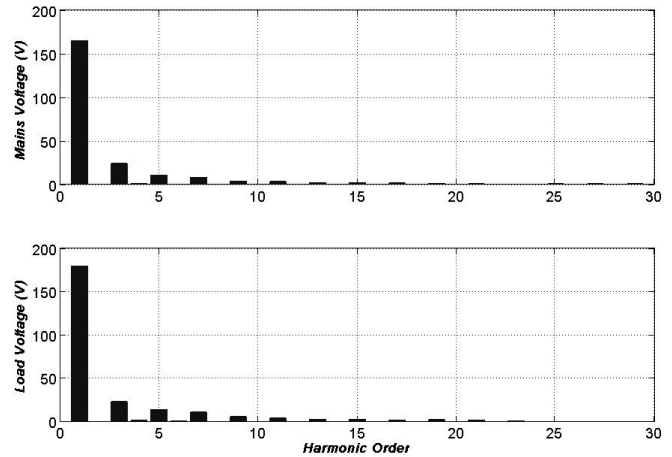


Fig. 16 . Voltage harmonic spectra. Mains Voltage (top) and Load Voltage (bottom)

## VII. CONCLUSION

This paper has presented the simplified design and power requirements as well as the control algorithms derivation of a low-power Dynamic Voltage Restorer (DVR) which compensates voltage sags and harmonics. The algorithms were analyzed through computer simulation and implemented in a Digital Signal Processor (DSP). Finally, experimental results of a 5-kVA/220V prototype have been presented in order to validate the proposed approach. Preliminary results on voltage harmonic compensation of the DVR are also shown, demonstrating the need of improvements on control, which are under development.

## REFERENCES

- [1] "IEEE recommended practices for monitoring electric power quality", *IEEE Std.1159-1995*.
- [2] M.J. Sullivan, T. Vardell, M. Johnson, "Power interruption costs to industrial and commercial consumers of electricity" *IEEE Transactions on Industry Applications*, vol.33, no.6, pp.1448-1458, Nov/Dec 1997.
- [3] L. Matakas Jr., W. Komatsu, J.A. Jardini, S.U. Ahn, M. Galassi, F.O. Martinz, S. Copeliovitch, F.A.T. Silva, M. Masuda, J. Camargo, E.R. Zanetti, "A Low Power Dynamic Voltage Restorer with Voltage Harmonic Compensation", in *Proc. of the 2005 International Power Electronics Conference (IPEC)*, pp.475-481, May 2005, Japan.
- [4] C. Fitzer, A. Arulampalam, M. Barnes, R. Zurowski, "Mitigation of saturation in dynamic voltage restorer connection transformers", *IEEE Transactions On Power Electronics*, Vol. 17, no. 6, pp. 10058-1066, November 2002.
- [5] A.D. Junqueira, W. Komatsu, L. Matakas Jr., "Digital implementation of three-phase rectifier with deadbeat controller", *Revista de Eletrônica de Potência da Sobraep*, vol.7, no.1, November 2002, Brazil.

- [6] L. Malesani, P. Mattavelli, S. Buso, "Robust deadbeat current control for PWM rectifiers and active filters", *IEEE Transactions on Industry Applications*, vol.35, no.3, pp.613-620, May-Jun- 1999.
- [7] P. Mattavelli, S. Buso, "Uninterruptable power supply multi-loop control employing digital predictive voltage and current regulators", *IEEE Transactions on Industry Applications*, vol.37, no.6, pp.1846-1854, Nov-Dec 2001.
- [8] F. O. Martinz, A.D. Junqueira, M. Galassi, L. Matakas Jr., "Stability Analysis of a digital predictive current controller for PWM converters", in *Proceedings of the 8<sup>th</sup> Brazilian Power Electronics Conference*, pp.146-150, June, 2005, Brazil.
- [9] "IEEE Recommended Practices for Harmonic Control in Electrical Power Systems", *IEEE Std.519-1992*.
- [10] W.E. Brumsickle, R.S. Schneider, G.A. Luckjiff, D.M. Divan, M.F. McGranaghan, "Dynamic Sag Correctors: Cost-effective industrial power line conditioning", *IEEE Transactions on Industry Applications*, vol.37, no.1, pp.212-217, Jan-Feb 2001.
- [11] J.G. Nielsen, F. Blaabjerg, "Comparison of system topologies for Dynamic Voltage Restorers", *Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE Industry Applications Conference*, vol.4, pp. 2397 - 2403.
- [12] J. Praveen, B.P. Muni, S. Venkateswarlu, H.V. Makthal, "Review of Dynamic Voltage Restorer for Power Quality Improvement", in *Proc. of the Thirty Annual Conference of the IEEE Industrial Electronics Society*, 2004, pp. 749 - 754.
- [13] J.A. Jardini, S.U. Ahn, L. Matakas Jr., W. Komatsu, M. Masuda, F.A.T. Silva, M. Galassi, F.O. Martinz, S. Copeliovitch, M.A. Oliveira, J. Camargo, E.R. Zanetti, E.G. Lima, "Implementação e Testes alfa da Geração de Referência e Controle em um Protótipo de Restaurador Dinâmico de Tensão", in *Proc. of the 6<sup>th</sup> Seminário Brasileiro sobre Qualidade de Energia Elétrica (SBQEE)*, 2005, pp. 205 - 212.
- [14] M. Masuda, S.U. Ahn, J.A. Jardini, L. Matakas Jr., W. Komatsu, F.A.T. Silva, S. Copeliovitch, F. O. Martinz, M. Galassi, M.A. Oliveira, J. Camargo, E.G.Lima, "Desenvolvimento de Restauradores Dinâmicos de Tensão de Baixa Potência", in *Proc. of the 3<sup>rd</sup> Congresso de Inovação Tecnológica em Energia Elétrica (CITENEL)*, 2005.

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