DOUBLE MODULATION APPLIED TO A HIGH POWER FACTOR RECTIFIER WITH HIGH FREQUENCY TRANSFORMER FOR UPS APPLICATION

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***Abstract* – The bridgeless boost-full-bridge rectifier is used as preregulator for a high frequency isolated UPS and the asymmetric pulse width modulation (APWM) modulation is applied in order to obtain a high quality input current with high power factor. The rectifier operates with soft-switching and reduced conduction losses improving the efficiency. A simultaneous phase-shift modulation allows obtain a fast output voltage control and step-up/step-down static gain, becoming possible the operation in a wide voltage range. An auxiliary power feed-forward action allows improving the dynamic response of the output voltage and primary side DC-bus voltage for the load transient. The double modulation and the auxiliary control action reduce the DC-bus voltage overshoot and undershoot during the output load transients, reduce the converter filters capacitance and limit the maximum voltage across the switches. The theoretical analysis and design procedure are presented for the modulations proposed and the experimental results were obtained from a 2 kW prototype operating with switching frequency equal to 44 kHz. The experimental results are presented using four different combinations of control structures showing comparatively the dynamic improvements.**

***Keywords* –AC-DC Power Conversion, Digital Control, Rectifiers.**

I. INTRODUCTION

The AC-DC converters operating with high power factor (HPF) and low input current harmonic distortion are important to maintain the energy quality of the utility grid. A common configuration used in most part of applications is composed by two stages. The input stage is a high power factor preregulator followed by a second stage as a DC-DC converter, used in telecommunication infrastructure application or a DC-AC converter used in AC machine drive or uninterruptible power supply (UPS) applications [1]-[3].

The conventional structure used in UPS applications is a non isolated boost converter as pre-regulator and a full-bridge non isolated inverter. When the galvanic isolation is necessary, a simple solution is the inclusion of a low frequency transformer in the pre-regulator input or in the inverter output. This is an usual structure used in true on-line UPS and it is a robust and reliable solution. However, the galvanic isolation obtained with low frequency transformer increase the weight, volume and cost [1]. Therefore, the development of topologies including the galvanic isolation in high frequency link can increase significantly the UPS power density [1], [3], [4].

A HPF rectifier with high-frequency transformer is proposed in this paper presenting some operation characteristic for high efficiency and high power density applications. All switches operate with soft-commutation allowing the operation with high switching frequency.

A bridgeless rectifier configuration is used reducing the conduction losses. The high-frequency multiphase operation reduces the input current ripple and shares the current among the input inductors and switches. The non idealities of the circuit, as the transformer leakage inductance, are used by the power circuit in order to obtain soft-commutation and the use of dissipative snubbers is not necessary.

However, the proposed converter presents as drawback two DC-bus capacitor, one at the primary and other at the secondary side. Some improvements in the control strategy of the preregulator are proposed in this paper reducing the bus capacitor volume and the voltage overshoot and undershoot at the load transient. The control improvements allows the use of the minimum DC-bus capacitance, limited by the maximum RMS capacitor current, operating with an overshoot and undershoot close to 1% in the DC-bus voltage at the primary and secondary sides.

Four control structures are presented combining different control techniques and the results are analyzed and compared, showing the high dynamic performance obtained.

II. PREREGULATOR POWER CIRCUIT

The use of high-frequency transformer is possible replacing the classical boost converter with low frequency transformer in the input by a rectifier with high-frequency transformer link. However, this is a high complexity solution and there are several problems to be solved in order to maintain the converter robustness, efficiency and cost in a competitive level. Some alternatives for low output power applications (P_o<500 W) are the use of single switch isolated DC-DC converters such as flyback, SEPIC and CUK topologies, mainly operating in discontinuous conduction mode (DCM) [4]. The continuous conduction mode (CCM) normally is considered for applications with output power higher than 500 W. A first solution is the replacement of the classical non-isolated boost converter by the current fed full-bridge converter [5]. However, this solution presents some limitations as the hard-switching commutation that reduces the efficiency. The energy stored in the transformer leakage

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inductance results in switch overvoltage and snubber circuits are necessary. The active clamping technique can be used in order to solve some of these problems [6]. However, the additional switch and isolated command circuit increase the cost and complexity and a specific command signal for the auxiliary switch must be generated. Also, these solutions present the conduction of four semiconductors at the primary side in each operation stage, besides the auxiliary switch, increasing the conduction losses.

Another alternative for the high-frequency isolated rectifier implementation is the use of solutions based on integrated isolated DC-DC converters. An interesting topology is the integration of a boost DC-DC converter with the half bridge DC-DC converter. This configuration was firstly presented in [7] and is also proposed with some modification in [8]-[10].

A bridgeless HPF rectifier with high-frequency isolation using the boost-half-bridge converter is presented in [11]. The operation as rectifier with an asymmetrical PWM modulation allows obtaining zero voltage switching (ZVS). The replacement of two diodes of the rectifier bridge by the half-bridge commutation leg reduces the rectifier conduction losses. However, the topology presented in [11] was developed operating in DCM at the input side, limiting the use in low power applications. Also, the asymmetrical operation of the half-bridge section can result in high current in the semiconductors in high power application.

A better current distribution and symmetrical operation can be obtained for high power application using the integration of a multiphase boost DC-DC converter with a full-bridge DC-DC converter. This configuration was presented in [12] in a DC-DC converter application using the phase-shift modulation. The operation with asymmetrical PWM or with phase-shift modulations allows obtaining ZVS commutation and the current sharing between the commutation legs. The full-bridge topology is indicated for high power operation and this configuration is adopted in this work for the UPS application.

A bridgeless rectifier using the boost-full-bridge with current source output characteristic was proposed as a single stage switch mode power supply (SMPS) in [13]. The SMPS application presents low output voltage (V_o=48 V) and the output inductor filter is designed for the full-bridge operation in CCM at nominal output power. A two duty-cycle modulation was proposed in [13] for the boost-full-bridge rectifier in order to comply with the SMPS application requirements using a single stage converter. A duty-cycle defined by the simultaneous conduction period of the diagonal switches of the full-bridge are used to control the output voltage. Another duty-cycle defined by the conduction period of the lower switches or upper switches of the full-bridge are used to control the input current in order to obtain a high power factor.

However, the two duty-cycles modulation are not independent and one modulation limits the action of the other, imposing design and operation restrictions [13]. Some undesirable operation characteristics are the large primary side DC-bus voltage variation, input power factor reduction and harmonic distortion increment with the load and input voltage variations, input zero current cross distortion and operational problems at light load. Also the operation with soft commutation was not presented in [13].

The requirements for the HPF preregulator output voltage in a two stage UPS application are lower than in a single-stage SMPS. The operation with low frequency output voltage ripple and low output voltage dynamic performance is possible in UPS application. The second stage, that is the inverter, is designed to operate with a bus voltage with some variation without change the inverter output voltage quality. Also, preregulators used in UPS application presents high output voltage (V_o=400 V) and the operation requirement as input voltage and load variation are high, mainly with the UPS supplying non linear loads. The high power factor and low input current harmonic distortion for all input voltage and load range are also very important parameters in UPS application. Therefore, modifications in the modulation, control and topology of the boost-full-bridge rectifier are proposed in this paper in order to obtain a high performance preregulator for UPS application with high frequency isolation. The topology modifications are the elimination of the output inductor filter and the full-bridge converter section operating in DCM. These modifications are more adequate for the operation with high output voltage (V_o=400 V) and change significantly the converter operation and analysis. The voltage source output characteristic allows the operation with a semiconductors voltage at the secondary side lower than with the current source output characteristic. Also, the use of snubbers at the secondary side is not necessary eliminating the output filter inductor. The limitation of the current variation between the primary and secondary sides of the full-bridge is accomplished only by the transformer leakage inductance. A relative small inductance can be included in series with the transformer for the soft-commutation requirements. The analysis of the boost-full-bridge rectifier with output voltage source characteristic and the DCM operation of the full-bridge section operating with the asymmetric PWM modulation was not presented in previous works. Therefore, the analysis and design procedure is developed for the proposed modulation and after the simultaneous phase-shift modulation and different control strategies are included, improving the control performance and reducing the DC-bus capacitance at the primary and secondary sides.

III. BOOST-FULL-BRIDGE RECTIFIER OPERATION WITH THE APWM MODULATION

A. Simplified Operation Analysis and Theoretical Waveforms

The bridgeless boost-full-bridge rectifier with voltage source output characteristic used in this work is shown in Figure 1. This converter can be considered as the integration of a bridgeless multiphase boost converter with two commutation legs as presented in [14] and a ZVS full-bridge DC-DC converter without the output inductor filter presented in [15] and after in [16]-[18], both converters sharing the same power switches. The bus capacitor C_b at the primary side is the output of the bridgeless boost converter and is also the input of the full-bridge DC-DC converter.

The modulation used in order to obtain a high power factor with low input current harmonic distortion is the

asymmetric PWM and the same modulation signal is applied to each commutation leg, but with a constant phase-shift equal to 180º. This modulation also defines the energy transference from the primary side DC-bus voltage to the secondary side DC-bus voltage through the full-bridge section.

The operation of the proposed circuit can be analyzed in a half-cycle of the AC input voltage using the equivalent circuit presented in Figure 2. Considering an unitary transformer turns ratio, the power transformer is eliminated by simplification and all circuit is referred to the converter primary side.

The effects of the transformer leakage inductance (L_d) and the magnetizing inductance (L_m) are considered in the equivalent circuit. The input inductors are replaced by current sources with half of the converter input current. The operation stages of the soft-commutation are not presented by simplification.

The theoretical waveforms are presented in Figure 3. At the positive half-cycle of the input voltage, the input inductors (L_{ia}-L_{ib}), represented by current sources in Figure 2, store energy when the PWM signal is applied to the upper switches M_{1a}-M_{1b}. The lower switches M_{2a}-M_{2b} operates as the output diode of the classical boost during the energy transference to the bus capacitor C_b and the complementary signal $\overline{PWM}$ is applied to these switches.

At the negative half-cycle of the input voltage, the switches functions are changed. The input current is shared by the two phases and also the input current ripple is equal to half of the inductors current ripple due to the complementary operation resultant of the constant 180º phase-shift modulation.

The input diode D_{R1} conducts during all half-cycle of the AC input voltage and the diode D_{R2} conducts during the other half-cycle.

Considering the complementary operation of the switches of each commutation leg, the ZVS commutation is obtained in all power switches with the energy stored in the transformer leakage inductance, as shown in Figure 3. The ZVS full-bridge converter operation with input and output voltage source characteristic and the soft-switching analysis are presented in [15]-[18].

The output diodes have no reverse recovery current due to the low di/dt limited by the transformer leakage inductance. The average magnetizing current i_{Lm} and the average voltage of the magnetizing inductance present null value for any converter duty-cycle, as shown in Figure 3.

Therefore, there are no DC or low frequency components in the high-frequency transformer.

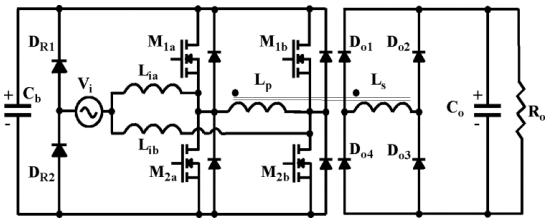


Fig.1. Bridgeless boost-full-bridge rectifier with voltage source output characteristic.

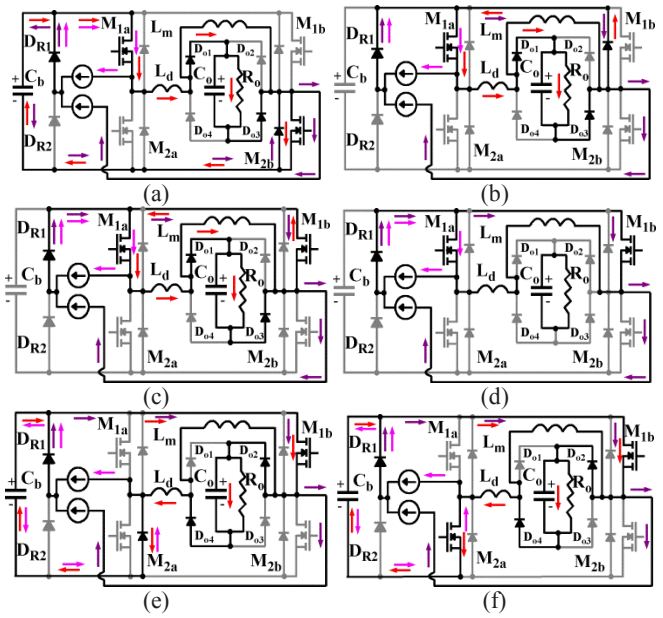


Fig. 2. Simplified operation stages for half-cycle of the AC input voltage. (a) First stage [t_o-t_1]. (b) Second stage [t_1-t_2]. (c) Third stage [t_2-t_3]. (d) Fourth stage [t_3-t_4]. (e) Fifth stage [t_4-t_5]. (f) Sixth stage [t_5-t_6].

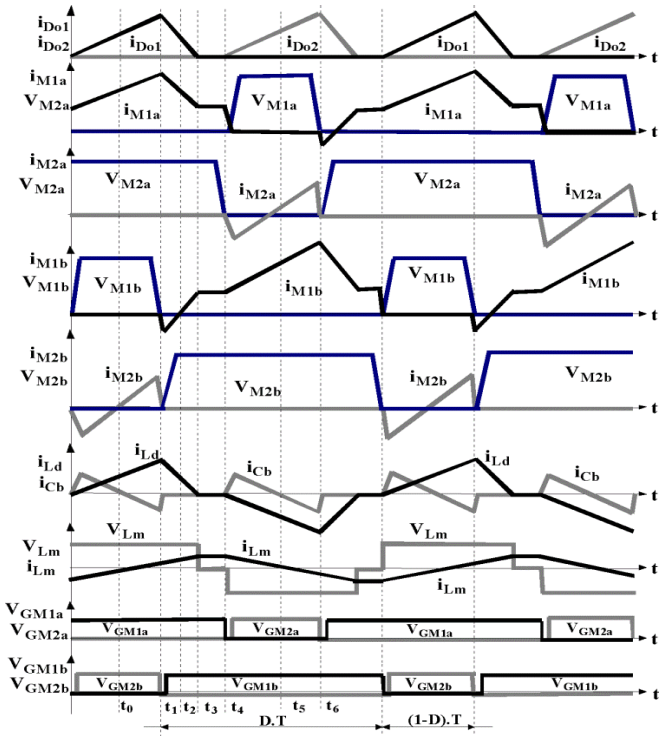


Fig. 3. Main theoretical waveforms.

B. Mathematical Analysis

The development of the main equations and the static gain of the boost-full-bridge converter with output voltage source characteristic and operating in DCM at the output are presented. Initially is considered the operation as a DC-DC converter with constant input voltage and after the equations are applied considering the operation as rectifier with an AC input voltage. The transformer turns ratio is considered unitary in the theoretical analysis and in the experimental prototype.

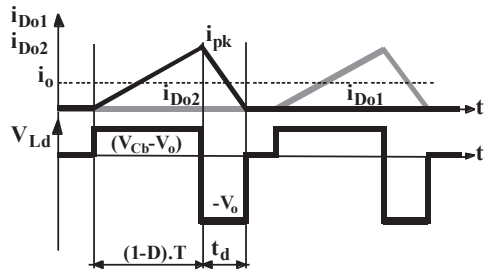


Fig. 4. Output rectifier current and leakage inductance voltage waveforms.

The main theoretical waveforms used in the equations development is the output rectifier current waveform presented in Figure 4. The voltage applied across the leakage inductance L_d is equal to the primary side DC-bus voltage V_{Cb} minus the output voltage V_o, during the fifth and sixth operation stages. Therefore, the output peak current i_{pk} can be calculated by:

$$i_{pk} = \frac{(V_{Cb} - V_o)(1-D)T}{L_d}. \quad (1)$$

The proposed converter operates as a classical multiphase boost converter at the primary side. Therefore, the primary side bus voltage is calculated by:

$$V_{Cb} = \frac{V_i}{1-D}. \quad (2)$$

Replacing (2) in (1), the output peak current can be also calculated by:

$$i_{pk} = \frac{V_i - V_o(1-D)}{L_d f}. \quad (3)$$

The leakage inductance is demagnetized with the output voltage V_o applied across the leakage inductance as presented in the second and third operation stages.

The period of leakage inductance demagnetization (t_d) is calculated by:

$$t_d = \frac{L_d i_{pk}}{V_o}. \quad (4)$$

Replacing (1) in (4), the period of leakage inductance demagnetization (t_d) is not dependent of the leakage inductance value and it is calculated by:

$$t_d = \frac{(V_{Cb} - V_o)(1-D)T}{V_o}. \quad (5)$$

The instantaneous average output current (i_o) is calculated by the area of the output current waveform presented in Figure 4 and is equal to:

$$i_o = \frac{i_{pk}}{T}\left[(1-D)T + t_d\right]. \quad (6)$$

Also, replacing (5) in (6) the instantaneous average output current is equal to:

$$i_o = \frac{i_{pk} V_{Cb}(1-D)}{V_o}. \quad (7)$$

Replacing (2) in (7), the instantaneous average output current is equal to:

$$i_o = \frac{i_{pk} V_i}{V_o}. \quad (8)$$

Replacing (3) in (7), the primary side bus voltage can be calculated as a function of the instantaneous average output current and voltage, such as:

$$V_{Cb} = \frac{i_o V_o L_d f}{V_i(1-D) - V_o(1-D)^2}. \quad (9)$$

Finally, the converter static gain is obtained replacing (2) in (9) and the result is given by:

$$V_o = \frac{V_i}{1-D} - \frac{i_o V_o L_d f}{V_i(1-D)}. \quad (10)$$

Considering a parameter *k* given by:

$$k = \frac{i_o V_o L_d f}{V_i} \quad (11)$$

the converter output voltage is calculated by:

$$V_o = \frac{V_i - k}{1-D}. \quad (12)$$

The static gain of the converter is similar to the static gain of the classical boost converter with a reduction (k) that is dependent of the leakage inductance, switching frequency and also changes with the load.

The specifications presented in Table I are considered in the application of the equations developed and in the experimental prototype.

Considering the converter operation with an AC input voltage, the instantaneous input current ($i_i(\omega t)$) can be obtained in order to calculate the instantaneous duty-cycle variation. Considering an ideal operation without losses, this current is given by:

$$i_i(\omega t) = \left(\sqrt{2}\frac{P_o}{V_{iRMS}}\right)\sin(\omega t). \quad (13)$$

TABLE I
Steady-State Converter Specification

Output power	P_o=2 kW
Output voltage	V_o=350 V
Primary side DC-bus voltage	V_{Cb}=406 V
Peak AC input voltage	V_{ipk}=155 V
RMS AC input voltage	$V_{iRMS} = V_{ipk}/\sqrt{2}$
Switching frequency	f=44 kHz
AC input voltage frequency	f_{AC}=60 Hz

Considering an ideal operation without losses, replacing (13) in (8), the instantaneous average output current is obtained as:

$$i_o(\omega t) = \frac{i_i(\omega t) V_i(\omega t)}{V_o}. \quad (14)$$

The average output current (I_o) is equal to half of the peak value of the instantaneous average output current ($i_o(90^o)$) and it is equal to $I_o=P_o/V_o=5.714$ A. From (10), the duty-cycle variation can be calculated as:

$$D(\omega t) = 1 - \frac{Vi(\omega t)^2 - V_o i_o(\omega t) L_d f}{V_o V_i(\omega t)} \quad (15)$$

where:

$$V_i(\omega t) = V_{ipk} \sin(\omega t) \quad (16)$$

Replacing (14) in (15), the duty-cycle variation can be calculated by:

$$D(\omega t) = 1 - \frac{Vi(\omega t) - i_i(\omega t) L_d f}{V_o}. \quad (17)$$

Considering the leakage inductance equal to zero, the duty-cycle variation is equal to the classical boost converter.

An external inductor can be included in series with the transformer primary winding in order to increase the transformer leakage inductance and the soft-commutation range as presented in [14]. However, this inductance also defines the DCM operation range of the full-bridge converter and the difference between the primary-side DC-bus voltage and the output voltage defined by the parameter k shown in (11).

The full-bridge section can be designed at the boundary of CCM and DCM at the nominal operation conditions in order to reduce the current stress. Considering the input power equal to 2.2 kW, the peak current at the transformer primary winding and the value of the leakage inductance for the boundary operation of DCM and CCM are calculated respectively by:

$$i_{pk} = \frac{2P_i}{V_{ipk}} = \frac{2 \cdot 2200}{155} = 28.39A \quad (18)$$

$$L_d = \frac{(V_{Cb} - V_o) V_o}{V_{Cb} 2 f i_{pk}} = \frac{(406 - 350) \cdot 350}{406 \cdot 2 \cdot 44 \cdot 10^3 \cdot 28.39} = 19.3 \mu H. \quad (19)$$

Considering the use of the inductance L_d=19.3 µH, the full-bridge section will operate at the boundary of DCM and CCM close to the nominal output power. The voltage difference between the primary side DC-bus voltage and the output voltage is equal to 56 V, as specified in Table I. The minimum duty-cycle at the peak of the AC input voltage is equal to $D(90^o)$=0.619 calculated by (15). Each switch operates with the PWM signal in one half-cycle of the input voltage and operates with the complementary signal in the other half-cycle of the input voltage. The other commutation leg presents the same modulation with a phase-shift equal to 180º.

IV. CONTROL STRATEGIES AND DOUBLE MODULATION

As presented in the theoretical analysis and in the converter static gain shown in (12), the proposed rectifier operation is similar to a classical boost converter. Thus, the classical control structure used in the boost preregulators can be applied in the proposed rectifier. But the classical preregulator control normally presents a slow dynamic performance resulting in relative high DC-bus overshoot/undershoot at the load transient. This problem can be minimized increasing the DC-bus capacitance in order to supply the difference between the instantaneous input and output power during the load transient.

However, this problem is more significant in the proposed rectifier because there are two DC-bus, one at the primary and other at the secondary side. Also, the power switches of the boost-full-bridge converter must support the maximum primary side DC-bus voltage. The power switches of the second stage (inverter) must support the maximum DC-bus voltage at the secondary side. Therefore, some modifications in the classical preregulator control are proposed in order to improve the dynamic performance and also to reduce the DC-bus capacitance to a minimal value at the primary and secondary sides. Four control strategies are developed and the first control structure considered is the classical average current mode control using the asymmetric PWM modulation. The results obtained with this classical control are considered as reference for the comparison with the three others control strategies used to improve the rectifier dynamic response.

A. Average Current Mode Control Using the APWM Modulation

The average current mode control is one of the most widely used methods to correct the power factor of rectifiers and can be adapted for the boost-full-bridge isolated rectifier. The input section of the rectifier operates in CCM and a fast internal current control loop and a slow external voltage loop can be used to obtain high input power factor and regulate the output voltage, as shown in Figure 5.

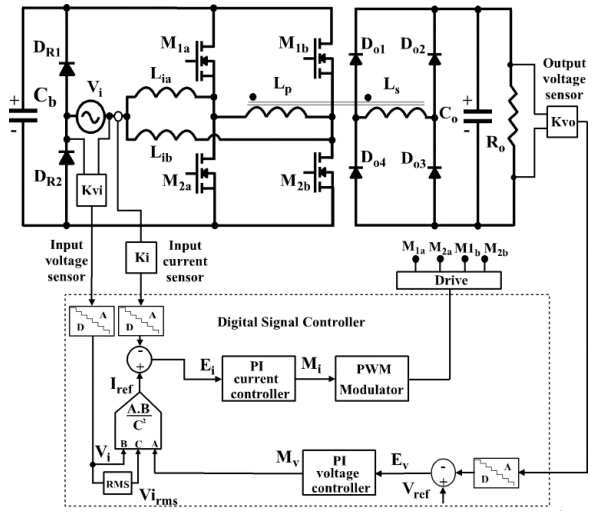


Fig. 5. Classical average current mode control using the asymmetric PWM modulation.

The input current is compared with a current reference (I_{ref}) and the error signal (E_i) is applied to a proportional-integral (PI) controller defining the converter modulation (M_i). The model of the system for current control loop is the same of the classical multiphase boost converter and the same design parameters can be considered. A classical boost design procedure is used and considering a cross frequency f_{ci}=1.7 kHz and phase margin M_{fi}=80º, the PI controller designed with a sample rate of f_{Si}=22 kHz is given by:

$$PI_i(z) = \frac{M_i(z)}{E_i(z)} = \frac{0.5(z-0.92)}{z-1}. \quad (20)$$

The input current reference I_{ref} is obtained by the multiplication of the current waveform (input B), that is the same input voltage waveform V_i, by the current amplitude (input A) defined by the output voltage control loop (M_v).

The voltage control loop is developed comparing the output voltage reference (V_{ref}) with the output voltage (V_o). The output voltage presents a low frequency ripple (twice of the input voltage frequency) as occurs in all preregulators due to the difference between the instantaneous input and output power. The voltage control loop output M_v must be only a DC component without the low frequency ripple in order to maintain the sinusoidal current waveform and the HPF. Therefore, the voltage control loop has a very low bandwidth and the cut-off frequency is typically ten-fold lower than ripple frequency. The slow dynamic in the voltage control loop causes a very slow transient response and high overshoot/undershoot in the DC-bus voltage during load transients. The DC bus output capacitor may be increased to limit the voltage transient for the second stage that is a voltage inverter in an UPS application.

If a load transient occurs, the input power will be different of the output power resulting in the output voltage variation. As the voltage control loop is slow due to the low frequency ripple rejection, the current reference amplitude is changed slowly until to obtain the power balance, regulating the output voltage. Therefore, the output voltage can change significantly during the load transient using this classical control structure.

The dynamic of the ZVS full-bridge DC-DC converter is much faster than the low bandwidth voltage control loop. Thus, the DC-DC full-bridge section can be considered a gain at steady-state for the voltage control loop.

The same design parameters of the classical preregulator are considered in the voltage control loop design. The voltage control loop cross frequency is equal to f_{cv}= 15 Hz and phase margin M_{fv}=80º. Using a sample rate of f_{Sv}=2.7 kHz, the designed PI voltage controller is given by:

$$PI_v(z) = \frac{M_v(z)}{E_v(z)} = \frac{1.884(z-0.994)}{z-1}. \quad (21)$$

The DC-bus voltage at the primary side is unregulated as shown in Figure 5 and can present voltage variation at the load transient and at steady-state.

B. Average Current Mode Control Using the APWM Modulation and the Output Power Feed-forward

Some techniques have been developed in order to improve the operation of the classical rectifier average current mode control. The works presented in [19]-[21] are proposed to solve the problem of the slow voltage control loop and poor dynamic performance. Some solutions proposes the elimination of the low frequency ripple from the voltage control loop using notch filters in the sample of the output voltage. This allows the increment of the bandwidth and the cut-off frequency. There are also no linear techniques with more complex solutions as presented in [21].

A fast output power feed-forward technique is used in this work obtaining a fast change in the input current reference at the load transients independently of the slow output voltage control loop and also maintaining the high power factor operation. The fast operation of the output power feed-forward allows the definition of the correct input current value for the output load transient. This reduces significantly the DC-bus capacitor undershoot and overshoot. The control system structure is presented in Figure 6, which is basically the same presented in the previous session, but now including a sum of a second signal (M_p) in the definition of the input current reference, beside the output voltage control loop (M_v), such as:

$$I_{ref} = \frac{K_{Vi}V_i \dfrac{P_o}{V_{iRMS}}}{V_{iRMS}} + \frac{K_{Vi}V_iM_v}{V_{iRMS}}. \quad (22)$$

The output power feed-forward operates obtaining the rectifier output power and the correct input current reference is calculated, maintaining the input and output power balance.

When a load transient occurs, the output power is calculated by the average value of the instantaneous output power. This result is divided by the RMS input voltage, calculating the correct input current reference amplitude at each cycle of the AC input voltage.

The output power feed-forward (M_p) defines the total current reference amplitude (input A) with the use of correct parameters. The voltage control loop operates only with a small contribution in the determination of the reference current amplitude during the transients and presents null value at steady-state (M_v=0). This auxiliary control action can be used also in the classical non isolated boost rectifier.

The output power is obtained with the measurement of the output voltage and current. But in an UPS application normally the UPS output power is measured and this information can be applied to the control of the rectifier stage without the use of additional current sensor.

The DC-bus voltage at the primary side is unregulated with this control structure, as shown in Figure 6, and can present voltage variation at the load transient and at steady-state.

C. Average Current Mode Control Using the Double Modulation APWM/PS

The power transference between the primary side to the secondary side through the full-bridge DC-DC converter section can be obtained also with the phase-shift modulation.

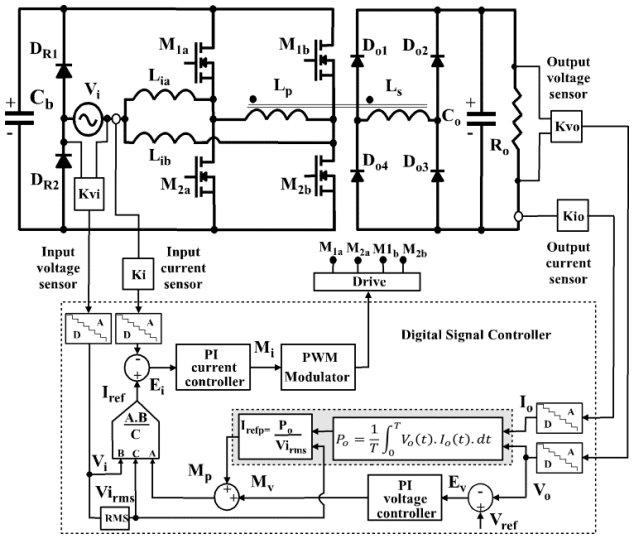


Fig. 6. Control system using the modulation APWM and output power feed-forward.

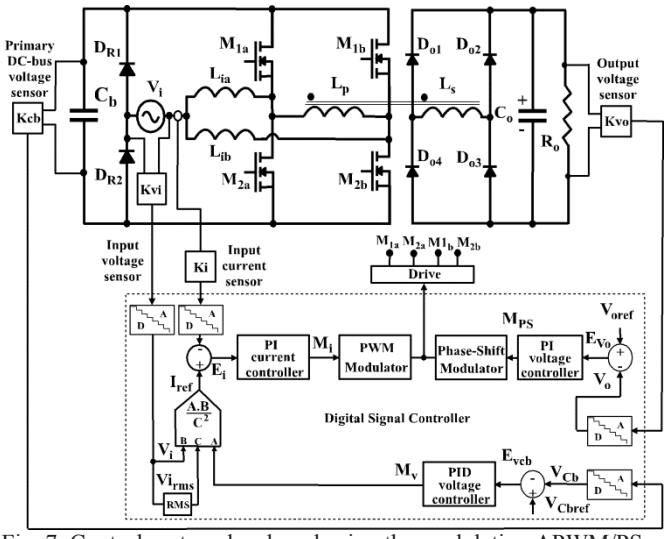
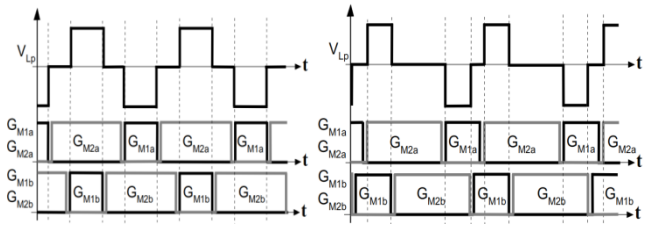


Fig. 7. Control system developed using the modulation APWM/PS.



(a) (b) APWM/PS

Fig. 8. Modulation strategy for the boost-full-bridge rectifier. (a) APWM. b) APWM/PS.

Appling the same APWM in both commutation legs with a phase-shift equal to zero, it is possible to control the input current and the primary side DC-bus voltage, maintaining null the output voltage.

Changing the phase-shift between the commutation legs from 180º to 0º, the rectifier output voltage will be linearly reduced from the maximum output voltage value calculated by (10) to zero as a step-down converter.

The following operation characteristics are obtained using the double modulation APWM/PS:

- a fast and independent output control loop can be developed controlling the full-bridge phase-shift, improving the dynamic response of the output voltage, maintaining high power factor and low input current harmonic distortion.
- The classical average current mode control can be used to regulate the primary side DC-bus voltage with the APWM modulation, limiting the primary side DC-bus voltage variation at the load transient. This increases the converter reliability and also improves the operation conditions for the control of the output voltage. A second independent control loop can be used to control the output voltage with the phase-shift modulation.
- The operation with a large voltage range is possible due to the step-up/step-down output characteristic obtained with the double modulation.
- The independent control operation allows obtaining a high power factor and low input current distortion in all output voltage range.
- The fast control of the output voltage allows the reduction of the overshoot/undershoot at the load transients and the reduction of the DC-bus capacitors.
- The independent control system operation allows the use of the classical models of the boost converter for the input section and the full-bridge converter for the output section. The controls present the same flexibility of a two stage converter composed by a boost AC-DC and full-bridge DC-DC structures, but using a single stage converter.

The input current waveform is defined by the APWM and the simultaneous phase-shift modulation does not change the input current waveform.

The control structure using the double modulation APWM/PS is presented in Figure 7.

The classical average current mode control regulates the primary side bus voltage and obtain high power factor changing the converter duty-cycle. A fast output voltage control loop regulates the output voltage changing the phase-shift of the two commutation legs. The asymmetric PWM and simultaneous modulation are presented in Figure 8. The average current at the transformer primary side is null with both modulations.

However, there is a limitation in the simultaneous modulation operating as a high power factor rectifier. When the instantaneous AC input voltage is near to the zero crossing, the duty-cycle of the APWM is close to one and the complementary signal is close to zero for the input current waveform to follow the input voltage waveform.

Therefore, even with a fast output voltage control loop, the low frequency ripple of the output voltage is not eliminated due to the extreme value of duty-cycle near of the zero crossing of the input voltage. The low frequency ripple can be reduced limiting the maximum duty-cycle value, allowing the power transference from primary side to the output at the input AC voltage zero crossing.

However, this maximum duty-cycle limitation will reduce the input power factor increasing the input current distortion. The experimental results show that limiting the maximum duty-cycle to D=0.8, the power factor was reduced from 0.999 to 0.977 and the output low frequency voltage

ripple was reduced from 10 V to 2 V. The low frequency output voltage ripple is not a problem for the preregulator operation in UPS application and the maximum duty-cycle is not limited in this application.

The controllers applied in the input current control loop and in the DC-bus voltage control loop are the same used in the control systems presented in the previous sections. However, the primary side DC-bus voltage is controlled by the classical control structure.

The fast output voltage control loop changes the converter phase-shift and a PI controller is used considering a cross frequency equal to f_{cPS}= 350 Hz and phase margin M_{fPS}=80º. Using a sample rate of f_{SPS}=22 kHz, the designed PI voltage controller is given by:

$$PI_{PS}(z) = \frac{M_{PS}(z)}{E_{Vo}(z)} = \frac{10.38(z-0.982)}{z-1}. \quad (23)$$

An important design parameter that must be considered for the correct operation of the double modulation control system is the minimal value of the regulated DC-bus at the primary side (V_{Cb}). The V_{Cb} voltage must be the factor "k", calculated by (12), higher than the output voltage referred to the primary side.

If a primary side DC-bus voltage undershoot occurs due to a load increment transient and the primary side DC-bus voltage to reach a value lower than this minimum limit, the output voltage will be reduced during the load transient even with the maximum action of the phase-shift output voltage control loop.

D. Average Current Mode Control With the APWM/PS Modulations and the Output Power Feed-forward

The classical average current control used to regulate the primary side DC-bus voltage in the previous structure presents a slow dynamic performance resulting in high overshoot/undershoot in the primary side DC-bus voltage during load transients. Also, a minimal value of the primary DC-bus voltage must be ensured during the load increment transient, as commented in the last section for the correct operation of the fast phase-shift output voltage control. This problem can be solved elevating the reference of the primary side DC-bus voltage. But this increases the switch voltage and also limits the possibility of reduction of the primary side DC-bus capacitance.

The primary side DC-bus voltage control operation can be improved applying the auxiliary output power feed-forward action, reducing overshoot/undershoot of the primary side DC-bus voltage under the load transient.

This results in a better operation condition for the fast output voltage control loop with the phase-shift operation and also allows the reduction of the primary side DC-bus capacitance. The control structure using the double modulation APWM/PS and the output power feed-forward action is presented in Figure 9.

The average current mode control regulates the primary side bus voltage and obtain high power factor. The amplitude of the input current reference is calculated by the slow control loop of the primary side DC-bus voltage and by the fast output power feed-forward algorithm.

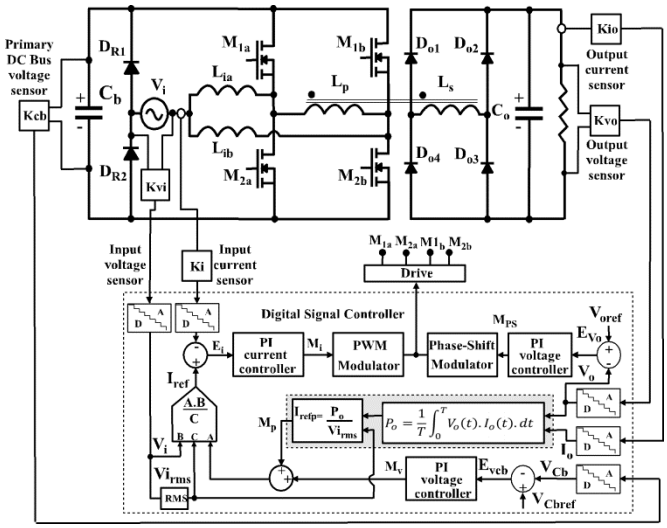


Fig. 9. Control system developed using the modulation APWM/PS and output power feed-forward.

Therefore, the fast balance of the input and output power during the load transient ensure a reduced overshoot/undershoot at the primary side DC-bus voltage. The controllers used are the same presented in the previous sessions.

V. EXPERIMENTAL RESULTS

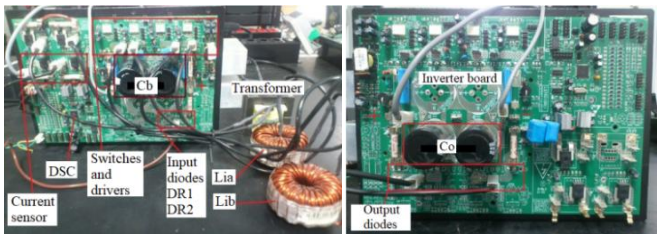
The static and dynamic performance of the proposed rectifier presented in Figure 1 is verified with the implementation of a prototype considering the specifications presented in Table I. Table II presents the main prototype parameters obtained with a design procedure using the main equations presented in the theoretical analysis. The experimental prototype is presented in Figure 10 and is divided in two boards fixed in both sides of a heat sink. All rectifier components at the transformer primary side are in the rectifier board shown in Figure 10a. The rectifier components at the secondary side, that are the output diode bridge and output filter capacitor, are in the inverter board presented in Figure 10b, that shows also all components of the inverter stage of the UPS.

The design of the input inductors and filter capacitors follows the classical procedure of the boost converter and the design of the power transformer follows the design procedure of the full-bridge DC-DC converter.

A. Experimental Results - Steady-state Operation

The high power factor operation can be observed in Figure 11a. The total harmonic distortion of the grid voltage and of the rectifier input current are equal to THD_V=6% and THD_i=8% respectively. The voltage at the DC-bus primary (C_b) and secondary (C_o) sides are presented in Figure 11b. Considering the converter operation with the parameters presented in Table II and with L_d=19.3 µH, the voltage difference between primary and secondary bus voltage is close to 56 V as specified in the converter design.

The ZVS commutation of the switches of a commutation leg is presented in Figure 12, as presented in the theoretical waveforms. The switch voltage is equal to the primary side DC-bus voltage (V_{Cb}).



(a) (b)

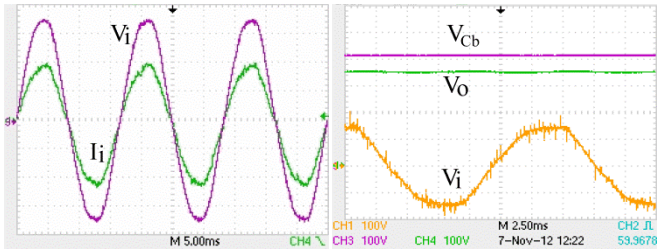
Fig. 10. Experimental prototype. a) Rectifier board. b) Inverter board.

The current at the transformer primary side is shown in Figure 13a. The transformer is magnetized and demagnetized at each switching cycle and does not present DC or low frequency current at the primary side.

The current in each input inductor (L_{ia} and L_{ib}) is presented in Figure 13b. This acquisition also shows that the input current is the sum of the input inductor currents, presenting half of the current ripple and twice of the average current and frequency.

TABLE II
Circuit Parameters and Components

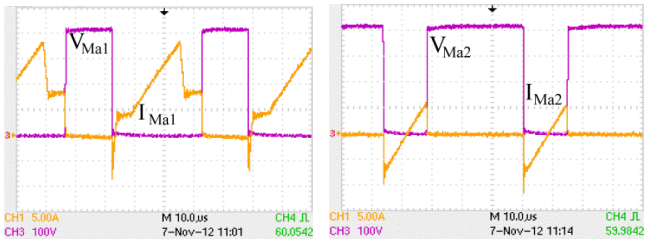
Output Power	P_o=2 kW
Output Voltage	V_o=350 V
Input Voltage	V_{in}=110 V_{rms}
Switching Frequency	f=44 kHz
M_{1a}, M_{1b},M_{2a}, M_{2b}	IRGP50B60PD1
D_{o1} - D_{o4} D_{R1} - D_{R2}	MUR1560
L_{ia}, L_{ib}	525 µH – Toroidal core
L_p, L_s	Transformer core EE65/26: L_P=2.68 mH, L_S=2.68 mH, L_d=8.0 µH. Primary winding in series with a resonant inductor equal 11 µH. Core EE42/15.
C_o	1880 µF- Four capacitors 470 µFx400 V (parallel)
C_b	940 µF- Two capacitors 470 µFx450 V (parallel)
Digital Controller	DSC MC56F8257



(50 V/div - 10 A/div - 5 ms/div) (100 V/div - 2.5 ms/div)

(a) (b)

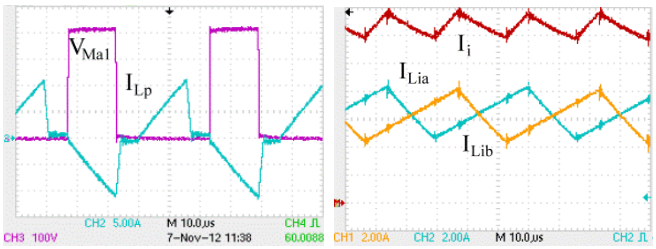
Fig. 11. Input voltage, input current and primary and secondary DC-bus voltages. (a) Input voltage (V_i) and input current (I_i). (b) Input and output voltage (V_o) and primary DC-Bus voltage (V_{Cb}).



(100 V/div - 5 A/div - 10 µs/div) (100 V/div - 5 A/div - 10 µs/div)

(a) (b)

Fig. 12. Switch voltage and current. (a) Switch voltage and current operating with the PWM signal. (b) Switch voltage and current operating with the $\overline{PWM}$ signal.



(100 V/div - 5 A/div - 10 µs/div) (2 A/div - 10 µs/div)

(a) (b)

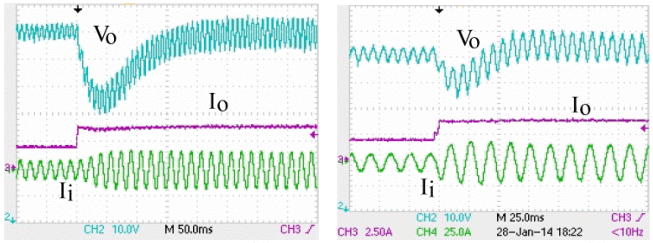
Fig. 13. Primary winding and inductors currents. (a) Primary winding current (I_{LP}) and switch voltage (V_{Ma1}). (b) Input inductors current (I_{Lin}) and input rectifier current (I_i).

Efficiency equal to 92% was obtained using low cost IGBTs. However, the efficiency can be improved replacing the power switches by low resistance MOSFETs or silicon-carbide switches that are more adequate than IGBTs for ZVS switch turn-off.

B. Experimental Results - Control System Operation

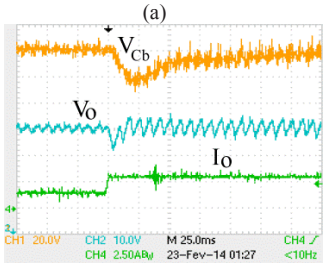
The four control structures presented in the theoretical analysis were tested using the digital signal controller MC56F8257. All experimental results were obtained with the primary side DC-bus capacitor equal to C_b=940 µF and the secondary DC-bus equal to C_o=1880 µF. Only in the last results obtained with the most complete control structure, the primary and secondary DC-bus capacitance were reduced to half of the value adopted in the previous tests.

Figure 14 shows the experimental results obtained from the four control structures for a load increment from 50% to the 100% of the output power. The output voltage and current and the input current are presented in Figure 14a, using the classical average current mode control with the APWM modulation shown in Figure 5. The output voltage variation is close to 30 V with a DC value of 350 V. The voltage undershoot is 8.5% and the setting time is ten cycles of the AC input voltage. The slow variation of the input current amplitude, due to the slow increment of the reference current amplitude defined by the low bandwidth voltage control loop, can be observed in this result. The performance obtained with the classical control is adequate for the most part of the applications and is similar to the dynamic results of the classical non isolated rectifiers. The first improvement in the average current control structure is the inclusion of the auxiliary output power feed-forward action presented in Figure 6, which is the second control structure. The result obtained is shown in Figure 14b. The output voltage transient average value is close to 10 V with a DC value of 350 V. The output voltage undershoot was reduced from 8.5% to 2.85% and the setting time was reduced from ten cycles to three cycles of the AC input voltage. The fast stabilization of the input current also can be observed using the fast auxiliary control action. However, the primary side DC-bus voltage is unregulated with the first and second control structures. The results obtained with the third control structure using the double modulation presented in Figure 7 are shown in Figure 14c. The output voltage undershoot was reduced to 1.42% and the setting time was reduced for one cycle of the AC input voltage due to the fast action of the output voltage control loop, changing the phase of the system.

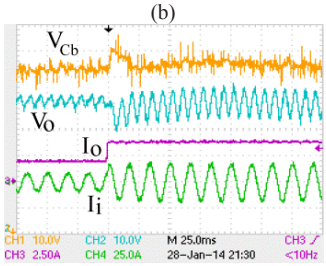


(10V - 2.5A - 25A - 50 ms/div) (a)

(10V - 2.5A - 25A - 25ms/div) (b)



(20V - 10V - 2.5A - 25ms/div) (c)



(10V - 2.5A - 25A - 25ms/div) (d)

Fig. 14 - Load transient from 50% to 100% of the output power with C_b= 940 µF and C_o=1880 µF. (a) Average current control. (b) Average current control and output power feed-forward. (c) Average current control and double modulation APWM/PS. (d) Average current control with double modulation APWM/PS and output power feed-forward.

Another important result shown in Figure 14c is that the primary side DC-bus voltage (V_{CB}) is regulated with this control structure.

However, as the slow voltage control loop of the average current control is used to control the primary side DC-bus voltage, the transient response is ten cycles of the AC input voltage and the voltage undershoot is close to 30 V.

The experimental results of the last and more complete control structure presented in Figure 9, including the auxiliary output power feed-forward in the control of primary side DC-bus voltage are shown in Figure 14d. The output voltage control loop maintains the fast control action. The fast change in the input current is also presented in Figure 14d, maintaining the high power factor. The primary side DC-bus voltage is regulated and presents an overshoot equal to 10 V instead an undershoot equal 30 V presented in the third control structure. The setting time was reduced from ten cycles of the AC input voltage to one cycle. The changing in the response behavior from the voltage undershoot to a limited voltage overshoot of the primary side DC-bus is favorable to the control of the output voltage due to the minimal voltage difference between the output voltage and the primary side DC-bus voltage (factor "k") that must be ensured, allowing the reduction of the DC-bus capacitance.

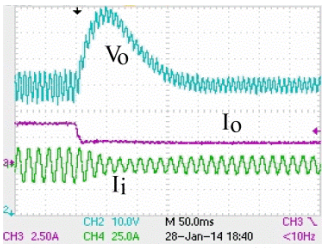
Figure 15 shows the experimental results obtained from the four control structures for a load decrement from 100% to the 50% of the output power. The average current control result, shown in Figure 15a, presents an output voltage overshoot of 30 V with a setting time of eight cycles of the AC input voltage.

The result obtained with the second control structure including the auxiliary output power feed-forward is presented in Figure 15b. The output voltage overshoot is reduced to 10 V and the setting time is three cycles of the AC input voltage.

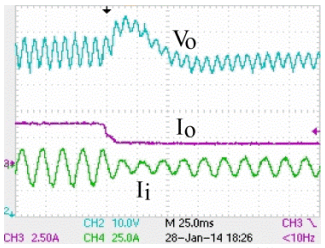
The result of the third control system using the double modulation is presented in Figure 15c. The output voltage overshoot is reduced to 5 V and the setting time is one cycle of the AC input voltage. The primary side DC-bus voltage is regulated with this control structure and presents an overshoot equal to 40 V.

The results of the fourth control structure shown in Figure 9, including the auxiliary output feed-forward action in the control of the primary side DC-bus voltage, are presented in Figure 15d. The output voltage control loop maintains the fast control action. The primary side DC-bus voltage is regulated and presents an undershoot equal to 8 V instead an overshoot equal to 40 V presented in the previous control structure.

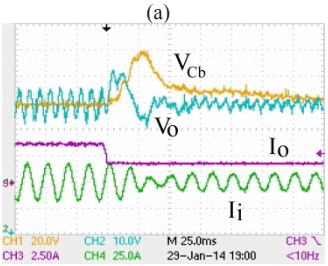
After the acquisitions of the experimental results obtained from the four control systems proposed, the load transients were repeated for the most complete control structure shown in Figure 9, reducing the primary and secondary DC-bus capacitance to half of the value used in the previous testes (C_b=470 µF and C_o=940 µF).



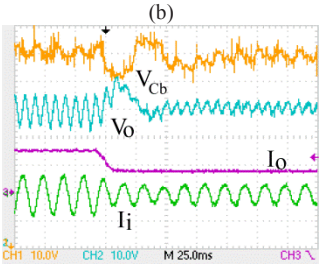
(10V - 2.5A - 25A - 50ms/div) (a)



(10V - 2.5A - 25A - 25ms/div) (b)

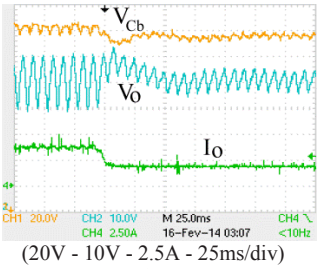


(20V-10V- 2.5A - 25A - 25 ms/div) (c)

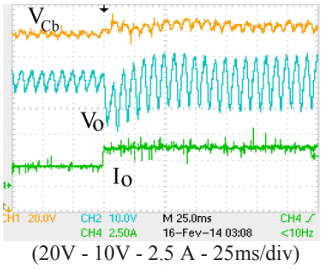


(10V-2.5A-25A-25 ms/div) (d)

Fig. 15 - Load transient from 100% to 50% of the output power with C_b= 940 µF and C_o=1880 µF. (a) Average current control. (b) Average current control and output power feed-forward. (c) Average current control and double modulation APWM/PS. (d) Average current control with double modulation APWM/PS and output power feed-forward.



(20V - 10V - 2.5A - 25ms/div) (a)



(20V - 10V - 2.5 A - 25ms/div) (b)

Fig.16. Average current control with double modulation APWM/PS and output power feed-forward with C_b= 470 µF and C_o=940 µF. (a) Load transient from 100% to 50% of output power. (b) Load transient from 50% to 100% of output power.

These results are presented in Figure 16a for the load decrement form 100% to 50% and in Figure 16b for the load increment from 50% to 100%.

In both results the primary DC-bus voltage and the output voltage present a variation close to the low frequency ripple and very fast response.

The classical average current mode control shown in session IV presents an adequate operation for many applications. However, the typical 10% of output voltage overshoot operating with Vo=400 V results in the utilization of higher voltage-rated capacitors (higher than 450 Vdc). The primary side DC-bus voltage also presents a large voltage variation.

Figures 16a and 16b shows that the combination of the double modulation APWM/PS and the output power feed-forward action allows the reduction of the voltage overshoot/undershoot close to 1% in both primary and secondary DC-bus, even operating with the minimum capacitance limited by the RMS capacitor current. Therefore, a reduced capacitance for the primary and secondary DC-bus and lower cost 450 V rated capacitors can be used with the proposed control structure. The maximum switch voltage at the primary side is limited to 410V at the load transient.

VI. CONCLUSION

The bridgeless boost-full-bridge rectifier with voltage source output characteristic is proposed as preregulator of an UPS with high-frequency transformer isolation. The operation with the input section in CCM and output section in DCM with voltage source output characteristic was presented and analyzed. The steady-state operation obtained presents some desirable characteristics for a high performance rectifier as high switching frequency with ZVS soft commutation, reduced conduction losses with the bridgeless configuration and low input current ripple due to the multiphase operation. However, the proposed converter presents two DC-bus capacitors at the primary and secondary sides and some developments are presented in order to reduce the converter capacitance.

Four control structures are proposed to control the isolated preregulator. The classical average current mode control with the APWM modulation was used obtain high power factor and regulating the output voltage. However, the typical control performance with 10% of overshoot/undershoot and a setting time of ten cycles of the AC input voltage were obtained. Also the primary side DC-bus voltage presents a large variation and the DC-bus capacitors cannot be reduced due to the limitations of the control performance.

The output power feed-forward algorithm is introduced in the preregulator control structure obtaining a fast output voltage response with overshoot/undershoot lower than 3% and a setting time of three cycles of the AC input voltage. But the primary side DC-bus voltage is not controlled and can present a large variation during the load transient.

The preregulator output current sensor used in the output power feed-forward is not necessary in two stages structures where the output power or current of the system is already measured, as in UPS and telecom applications.

The double modulation APWM/PS was developed regulating the primary side DC-bus voltage and the output voltage. The phase-shift modulation allows the development of a fast output voltage control maintaining the HPF. An overshoot/undershoot close to 1% and a setting time of one cycle of the input voltage is obtained. But a minimal voltage difference between the primary DC-bus voltage and the output voltage must be maintained in the load increment transient in order to maintain the high performance of the output voltage control. The primary DC-bus voltage presents the same performance of the classical average current control and presents 10% of overshoot/undershoot.

The best control performance was obtained using the double modulation APWM/PS operating with the output power feed-forward action where both primary DC-bus voltage and the output voltage presents an overshoot/undershoot close to 1% even operating with half of the capacitance used in the previous control structures. This result maintain limited the maximum switch voltage and capacitors voltage at the load transient, increasing the converter reliability and allowing the operation with the minimal capacitance at the primary and secondary DC-bus.

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