STUDY OF THE MODULATION SCHEMES IN THE HYBRID THREE-PHASE MULTILEVEL INVERTER

Marcos Vinicius Bressan[1], Marcello Lobo Heldwein[2], Alessandro Luiz Batschauer[1]
[1]UDESC/nPEE, Joinville – SC, Brazil
[2]UFSC/INEP, Florianópolis – SC, Brazil
e-mail: bressan.marcosvinicius@gmail.com, heldwein@inep.ufsc.br, batschauer@joinville.udesc.br

***Abstract* – This work proposes and analyzes modulation strategies for a hybrid three-phase multilevel inverter, which employs two different topologies in a cascade connection, a three-phase Neutral Point Clamped (NPC) converter and single-phase half-bridge converters. Two different modulation schemes are proposed: the hybrid modulation and the space vector modulation. The both modulation schemes can synthesize five voltage levels in the output phase voltage at the hybrid three-phase multilevel inverter with symmetrical dc sources. The modulation schemes operate the three-phase NPC in low-switching frequency and the half-bridge converters in high-switching frequency. Thus, semiconductors with low conduction losses can be used for three-phase NPC, decreasing the semiconductor losses. The hybrid three-phase multilevel inverter structure and modulation schemes are explained in detail and verified by simulation and experimental results.**

***Keywords* – Cascade Multilevel Converter, Hybrid Modulation, Hybrid Multilevel Inverter, Medium-voltage, Pulse Width Modulation, Space Vector Modulation.**

NOMENCLATURE

S_{jA}	Switches of the phase A.
$V_{x,y}$	dc source voltage values.
V_{ref}	Reference waveform of the output phase voltage.
M_a	Modulation index.
ω_o	Output angular frequency.
V_{cc}	Bus voltage.
$V_{g,h}$	Signals reference in gh coordinates.
P_{dc}	Active power to flow through the power supply.
i_o	Output current.
V_{RMS}	Supply voltage.
f_r	Supply frequency.
f_c	Carrier frequency.
f_o	Output frequency.
L_o	Load inductance.
R_o	Load resistance.
P_o	Load active power.
v_{AB}	Output line voltage between phases A and B.
i_A	Output phase current, phase A.

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I. INTRODUCTION

Voltage source multilevel converters have been highly developed in recent years through industrial and academic research, mainly due to their inherent capacity to process larger quantities of electric power in medium voltage (MV) applications, while employing mature semiconductor technologies [1]–[4]. As a result, the modern multilevel converters can synthesize higher output voltage levels with low voltage semiconductors and are a adequate solution for MV power electronics applications. Another great advantage of this technology is the typical output voltage waveform quality when compared to a two-level inverter. Multilevel inverters can synthesize a output voltage with more than two steps from the combination of different dc source levels, output voltage is close to a sinusoidal waveform and with relatively low harmonic distortion.

The most well known multilevel inverter topologies are arguably the Neutral Point Clamped Converter (NPC), the Flying Capacitor Converter (FC), the Cascaded H-Bridge Converter (CHB) and the Modular Multilevel Converter (MMC). The three-level/-phase NPC is well known and widely used in industrial applications in the MV and low voltage (LV) [5], [6]. Its structure can be driven with different modulation schemes, e.g., carrier-based pulse modulation, space vector modulation and optmized synchronous [7]. The NPC is used in power system applications, e.g., power flow control [8], and in motor drive applications [9]. Its main advantageous is not require bulky isolated dc sources, as in CHBs, or a large amount of capacitance, as in FCs. The FC [10] uses floating (or flying) capacitors that provide the clamping potentials to the switches and generate the multiple dc voltage levels to the converter output. FCs present a large number of redundant states that can be used to balance the floating capacitor voltages. The CHB structure employs of the series connection of identical cells, i.e., single-phase converters. Thus, the single-phase H-bridge converter is usually employed in CHB and each cell requires an isolated dc voltage source. Its modular structure is easy expandede and allows to use of low-voltage semiconductors in high voltage/power applications. In [11], the association of the two single-phase half-bridge converters has been used as the basic cell of the cascaded topology. This basic cell can generate three levels of output voltage, such as the H-bridge converters. The disadvantage of the cascaded converters are their separate dc sources that generally formed by bulky and expensive phase-shifting transformers [3], [12]. The MMC was presented in [13], and was recently accepted as a suitable choice in power systems applications at high voltage [14].

Its modular structure composed of series connection of half-bridge converters and does not require the isolated dc sources (phase-shifting transformers). Increasing the number of series connection converters increasing the number of the output voltage levels of the MMC.

Anther type of cascaded multilevel inverters are the hybrid multilevel inverters. They can be formed from the association of different converters topologies in their structure, e.g., employing NPC and full-bridge converters in the cells [15], [16]; or from different semiconductor technologies [17], [18], e.g., Integrated Gate-commutated Thyristors (IGCTs) or Gate Turn-off Thyristors (GTOs); or using different modulation schemes in each cell [19]. As an example, in reference [15] the authors proposed a three-level NPC cascaded connection with H-bridge cells generating up to fifteen levels of output phase voltage. However, dc voltage sources must be isolated from each other. In [19] and [20], the single-phase full-bridge converters are connected in series with a three-phase two-level converter to increase the number of output voltage levels. In all cases those topologies have particular modulation schemes and controls. Another hybrid solution was presented in [21], where single-phase half-bridge converters are connected to a three-phase two-level inverter. The single-phase half-bridge converter are connected in a particular way to replace H-bridge converters. Its modulation strategy used a low swithcing frequency in the three-phase inverter two-level and high-switching frequency in the half-bridge converters, that this enables to use different power semiconductors in the structure and reducing the power losses. However, the main disadvantage of this topology is the requirement of isolated power supplies for each half-bridge converter and for the three-phase two-level inverter. In [22], a hybrid multilevel inverter has been proposed from a three-phase NPC that is connected in series with single-phase full-bridge converters. This hybrid multilevel inverter is supplied only from a single dc source voltage at the three-phase NPC and there is no need to use transformers to provide the isolation to the single-phase converters. However, the capacitor voltage of the single-phase converters must be controlled. Another disadvantage is that the semiconductor of the three-phase NPC must block the peak of the output voltage, once the half-bridge converters don't supply active power to load and work with lower blocking voltages.

Therefore, for proper operation of the multilevel inverters, the choice of the adequate modulation scheme is fundamental. Some multilevel inverters can be operated with a large range of types of modulation schemes, in high or low-switching frequency.

The low-frequency modulation schemes usually operate the switches in the fundamental frequency, e.g., selective harmonic elimination (SHE), space vector control and nearest voltage level [23], [24]. These modulation schemes are interesting in multilevel inverters with higher number of output voltage levels, where the output voltage waveform is naturally close to a sine waveform [25]. For multilevel inverters with low number of output voltage levels, the high frequency modulation schemes are widely employed, e.g., carrier-based pulse width modulations (CB-PWM) and space vector modulation (SVM) [1], [3], [10]. High-frequency modulation schemes increase the switching losses, however they increase the output signal quality when compared to low-frequency modulation schemes. This characteristic allows reducing the size, volume and cost of the expensive output filters. The most weel-known carrier-based pulse width modulations are: phase disposition pulse width modulation (PD-PWM), phase opposition disposition (POD-PWM), alternative phase opposition disposition (APOD-PWM) and phase shift pulse width modulation (PS-PWM). Basically, the difference among those modulation schemes is the phase and offset disposition of the carrier signals, generating different command signals for the switches. The PD-PWM and PS-PWM are usually employed in multilevel inverters due to their characteristics. The PD-PWM has a low total harmonic distortion (THD) in the output line voltages, however it has poor semiconductor losses distribution. The PS-PWM can provide even current distribution among the semiconductors of the structure, i.e., even losses by inverter [26]. This feature makes the PS-PWM main modulation scheme to be used in modular converters. Both modulation schemes are easily applied independently on the number of the output step levels. Another widely studied high-frequency modulation scheme is the SVM. Due to its high degree of freedom it offers significant flexibility to operation of the power converter [2]. As an example, in [27], the SVM is applied to remove the low-frequency voltage oscillation that appears in the neutral point of the NPC, and, in [28], the SVM was used to reduce common-mode voltage (CMV) at the output of a multilevel inverter. For both cases, the inverter is penalized with increase of the switching and, consequently, the switching losses.

Others modulation schemes are proposed as a solution for specific problems found in some multilevel inverters [29]–[31]. In [29], the carrier signals have different operation frequencies, decreasing the switching losses in the semiconductors and slightly increasing the distortion in the output voltage, but all the switches are operating in high frequency. In [30], a pulse width modulation strategy was proposed for the CHB operating under unbalanced dc sources. The strategy uses the injection of the offset voltages in the reference signals to compensate the output voltage imbalance caused by unbalanced dc source. In [31], the PS-PWM strategy was improved, resulting in faster natural voltage balancing of the flying capacitors. However, this modified PS-PWM strategy does not allow to distribute the losses for all semiconductors of the FC.

In [32], the authors have proposed a hybrid multilevel inverter employing a three-phase NPC connected in series with half-bridge converters. A modulation strategy was proposed, allowing a low-switching frequency at the three-phase NPC, while the half-bridge converters switch in a high frequency. This feature allows the use of low conduction losses semiconductors in the three-phase NPC, reducing the losses of the multilevel inverter.

This work presents and analyzes different PWM strategies employed in a hybrid three-phase multilevel inverter [32], shown in Figure 1. The hybrid modulation and two types of space vector modulation are explored. The modulation strategies allows the three-phase NPC to be switched in low

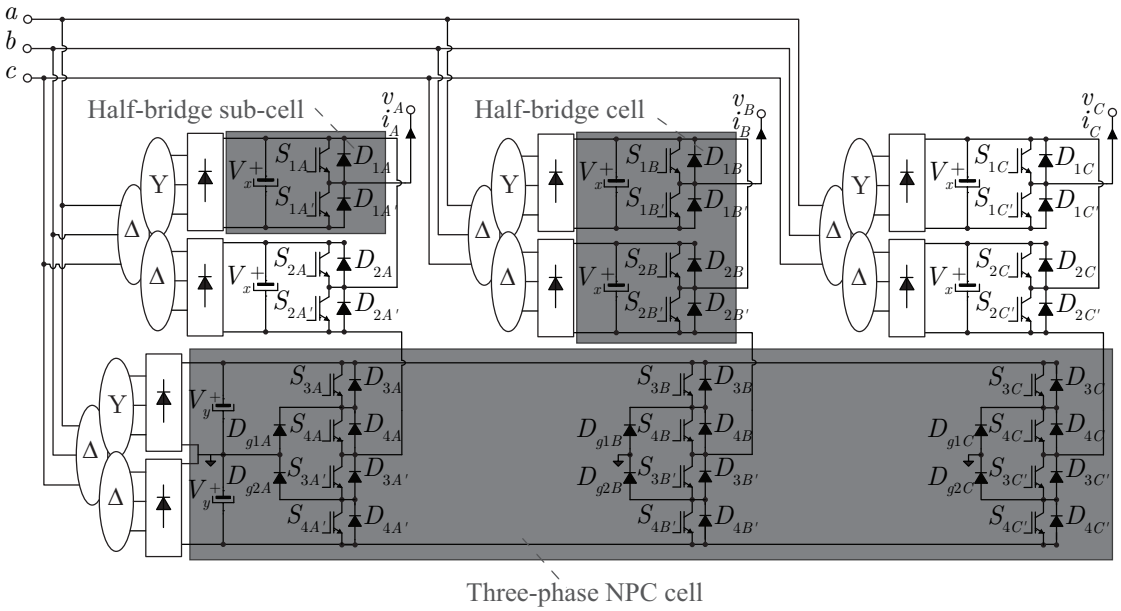

Fig. 1. Circuit schematic of the hybrid three-phase multilevel inverter employing single-phase half-bridge cells and a three-phase NPC inverter.

frequency and the half-bridge converters at high frequency. Thus, an efficiency increase and overall volume decrease are expected. The modulation strategies can be extended and used in hybrid multilevel inverters with a higher number of half-bridge converters in series, i.e., higher number of output voltage levels for the structure.

Section II is a description of the hybrid three-phase multilevel inverter structure, its operation states and output voltage ratios. The analysis of the proposed hybrid and space vector modulation schemes are presented in Section III. Finally, Section IV shows the experimental results.

II. HYBRID INVERTER

A. Structure

Figure 1 shows the hybrid three-phase multilevel inverter, that employs one three-phase NPC inverter and six half-bridge converters and eight isolated power supplies, where each half-bridge converter requires an isolated power supply and the three-phase NPC inverter demands the two isolated power supplies. In this case the power supplies are generated by isolation transformers with diodes rectifiers. Thus, one phase leg of the hybrid topology utilizes one phase leg of the three-phase NPC inverter and two half-bridge converters. The structure can be extended increasing the number of half-bridge converters and synthesizing more levels at the output voltage.

When compared, the structure presented in Figure 1 and one proposed in [21] have the same disavantage: both need of isolated power sources for each half-bridge converter and another for the three-phase inverter. However, the hybrid multilevel inverter, shown in Figure 1, reduces the active power processed by the half-bridge converters for high range of modulation indexes when compared to the inverter presented in [21], thus reducing the size of the dc source capacitors and rectifiers of the half-bridge converters [32].

B. Operation

The analysis of the hybrid three-phase multilevel inverter for four operation stages is shown in Figure 2, which shows only the half-bridge cells switching. The others operation stages are done switching the NPC cell too. Thus, the hybrid three-phase multilevel inverter has twelve operation stages.

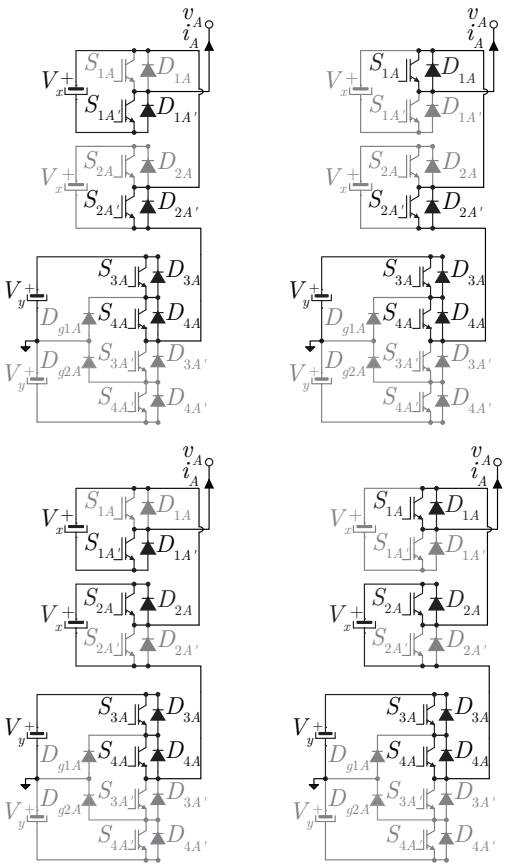

Fig. 2. Four operation stages for one phase-leg of the hybrid three-phase multilevel inverter.

TABLE I
Resulting Output Phase Voltage (v_o) as a Function of the dc Source Values V_x and V_y and of the Switching States

S_{1A}	S_{2A}	S_{3A}	S_{4A}	v_o	v_o (Case 1) $V_y = V_x = V_{cc}$	v_o (Case 2) $\frac{V_y}{2} = V_x = V_{cc}$	v_o (Case 3) $\frac{V_y}{3} = V_x = V_{cc}$
0	0	1	1	$+V_y - V_x$	0	$+V_{cc}$	$+2V_{cc}$
1	0	1	1	$+V_y$	$+V_{cc}$	$+2V_{cc}$	$+3V_{cc}$
0	1	1	1	$+V_y + V_x - V_x$	$+V_{cc}$	$+2V_{cc}$	$+3V_{cc}$
1	1	1	1	$+V_y + V_x$	$+2V_{cc}$	$+3V_{cc}$	$+4V_{cc}$
0	0	0	1	$-V_x$	$-V_{cc}$	$-V_{cc}$	$-V_{cc}$
1	0	0	1	0	0	0	0
0	1	0	1	$+V_x - V_x$	0	0	0
1	1	0	1	$+V_x$	$+V_{cc}$	$+V_{cc}$	$+V_{cc}$
0	0	0	0	$-V_y - V_x$	$-2V_{cc}$	$-3V_{cc}$	$-4V_{cc}$
1	0	0	0	$-V_y$	$-V_{cc}$	$-2V_{cc}$	$-3V_{cc}$
0	1	0	0	$-V_y + V_x - V_x$	$-V_{cc}$	$-2V_{cc}$	$-3V_{cc}$
1	1	0	0	$-V_y + V_x$	0	$-V_{cc}$	$-2V_{cc}$

*V_{cc} - dc-link voltages. **$o = A, B, C$

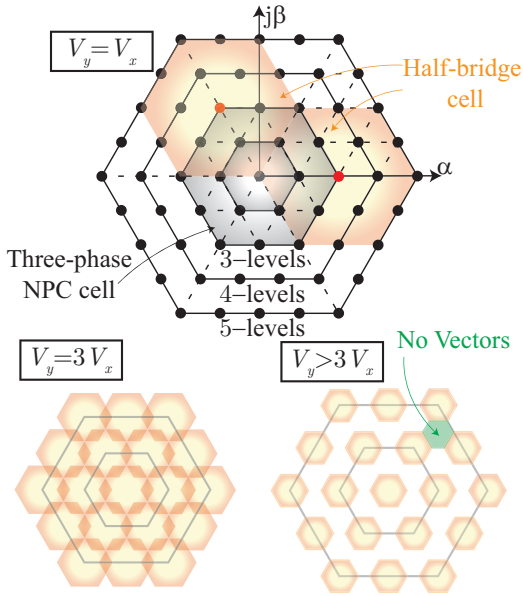

Fig. 3. Space vector diagram of the hybrid three-phase multilevel inverter for different ratios of the $V_y \neq V_x$, the space vectors resulting from the half-bridge cells are in orange, and the NPC cell are in gray.

The operating states and the dc voltage ratios define the step levels at output phase voltage, which is presented for phase A in Table I. Some assumptions are made for the analysis of the hybrid three-phase multilevel inverter operation: the devices are ideal, i.e., lossless; the dc source voltages are constant values and any parasitic element is neglected.

The number of levels at the output voltage for one phase changes according to the adopted modulation scheme, modulation index and dc source voltage values, V_x and V_y. In Table I the resulting output phase voltage is presented for all switching states and different dc source values. Where in Case 1 is assumed that $V_x = V_y$, i.e., symmetric dc sources are employed. Asymmetric dc sources are assumed in Cases 2 and 3, where $V_x = \frac{V_y}{2}$ and $V_x = \frac{V_y}{3}$, respectively. According to the "Case" operation, the hybrid multilevel can have five, seven or nine levels at the output phase voltages. For Case 1 the multilevel inverter has five levels at output phase voltages, in Case 2 it has seven levels at output phase voltages and nine levels are synthesized at output phase voltages for Case 3.

For the application of the hybrid multilevel inverters with asymmetrical dc sources is desirable the uniform condition of the voltage space vectors. It enables the utilization of the multilevel inverter without increasing the distortion of the output phase voltage waveform. Figure 3 shows the voltage space vector for different dc source ratios of the multilevel inverter. The voltage space vector is obtained applying the Clarke $\alpha\beta$ transform to the output voltages.

The uniform condition is achieved up to $V_y = 3V_x$, i.e., the converter has full PWM capability for relation. When the ratio of V_y is three times bigger than V_x the empty spaces appear at the space vector diagram. In other words, no vectors are synthesized in the empty spaces by the inverter and the uniform condition of the space vector diagram is lost.

In this work, the hybrid multilevel operates just as a five-level inverter, i.e., with symmetric dc sources (Case 1), with greater degrees of freedom for the inverter operation, and, thus, namely Five-level Symmetric Hybrid Inverter (5L-SHI).

III. MODULATION SCHEMES FOR THE 5L-SHI

Different modulation schemes in high frequency can be used to drive the 5L-SHI, such as: CB-PWM, hybrid modulation (HM) and SVM. To achieve a low-switching frequency in the three-phase NPC and a high-switching frequency in the half-bridge converters, two modulation schemes are explored: HM and SVM.

A. Hybrid Modulation Scheme

The HM has features of operation in low-switching frequency in the three-phase NPC inverter, i.e., at the output voltage frequency, and of high-switching frequency in the half-bridge converters, i.e., at the carrier frequency. In Figure 4 is shown the hybrid modulation used in the 5L-SHI.

Considering a reference waveform of the output phase voltage V_{ref} as

$$V_{ref} = M_a \sin(\omega_o t) \tag{1}$$

where:

M_a - modulation index ($0 \leq M_a \leq 1$);

ω_o - output angular frequency.

Comparing the desired waveform of the output phase voltage to the carrier signals leads to the command pulses at

high-switching frequency for the half-bridge cells. The low-frequency switching signals for the NPC switches are given by comparing the desired waveform of the output phase voltage with the three dc source ratios, in the case given by dc ratios $\pm\frac{1}{2}$ and 0, as shown in Figure 4.

B. Space Vector Modulation Scheme

The SVM is a complex technique where the number of output converter levels increases the computation cost and makes its application in real-time mode difficult. Some authors such as [27], [33]–[35] proposed methods that can be processed quickly by a digital signal processor. The modulation algorithm proposed in [27] processes all the calculations of the duty cycle and the definition of the best switching states in the first sextant. It is possible due to the symmetry in the space vector diagram, thus, reducing the computation cost and simplifying of the definition of the optimal switching states.

The trajectory of the rotating voltage reference mapped on the space vector diagram is given by the *gh* transformation:

$$\begin{bmatrix} V_g \\ V_h \end{bmatrix} = \frac{(n-1)}{\sqrt{3}V_{cc}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} V_{ref_A} \\ V_{ref_B} \\ V_{ref_C} \end{bmatrix} \tag{2}$$

where:

V_{cc} - bus voltage;

$V_{g,h}$ - signals reference in *gh* coordinates.

So, the switching states of the multilevel inverter for the first sector in the *gh* transformation are shown in Figure 5.

The mathematical efforts to find the nearest three vectors at the reference vector and its respectively duty cycle are simplified in the *gh* coordinates. As shown in Figure 5, for the first sector, the vectors have an integer *gh* coordinate. By the way, the reference vector is located inside of the parallelogram that the vertexes are formed by rounding up and down V_g and V_h, given by

$$\begin{aligned} \overrightarrow{V}_{ul} &= \begin{bmatrix} \text{ceil}\,(V_g) \\ \text{floor}\,(V_h) \end{bmatrix}, \quad \overrightarrow{V}_{lu} = \begin{bmatrix} \text{floor}\,(V_g) \\ \text{ceil}\,(V_h) \end{bmatrix}, \\ \overrightarrow{V}_{uu} &= \begin{bmatrix} \text{ceil}\,(V_g) \\ \text{ceil}\,(V_h) \end{bmatrix}, \quad \overrightarrow{V}_{ll} = \begin{bmatrix} \text{floor}\,(V_g) \\ \text{floor}\,(V_h) \end{bmatrix}. \end{aligned} \tag{3}$$

So, the parallelogram can be divided into two triangles and the vertexes are formed by three vectors. The three nearest vectors are, $\overrightarrow{V}_{uu}$, $\overrightarrow{V}_{lu}$, $\overrightarrow{V}_{ul}$, if $Su > 0$ and $\overrightarrow{V}_{ll}$, $\overrightarrow{V}_{lu}$, $\overrightarrow{V}_{ul}$, if $Su < 0$, where

$$Su = V_g + V_h - \left(V_{ul,g} + V_{ul,h}\right). \tag{4}$$

Then, the three nearest vectors are found and the duty cycle are defined by:

$$\begin{aligned} d_{ul} &= V_g - V_{ll,g} \\ d_{lu} &= V_h - V_{ll,h} \\ d_{ll} &= 1 - d_{ul} - d_{lu} \end{aligned} \tag{5}$$

if $Su < 0$, and by

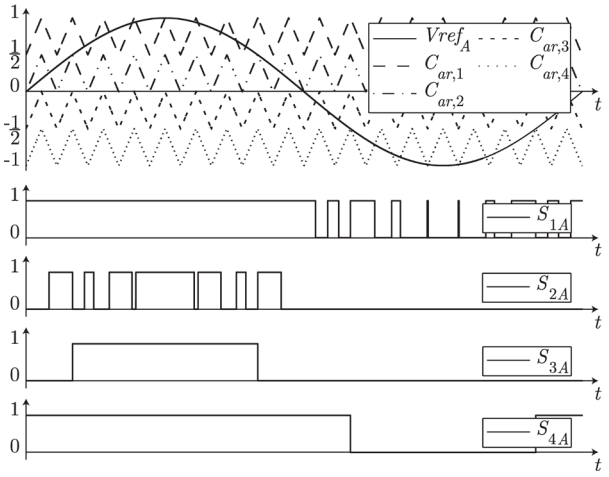

Fig. 4. HM for the 5L-SHI and the resulting switching patterns.

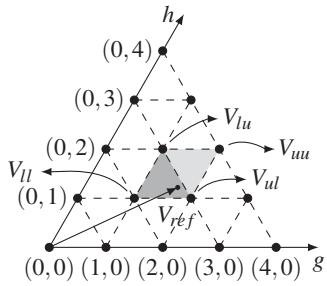

Fig. 5. Space vectors for the 5L-SHI in *gh* coordinates for the first sector.

$$\begin{aligned} d_{ul} &= V_{uu,g} - V_g \\ d_{lu} &= V_{uu,h} - V_h \\ d_{ll} &= 1 - d_{ul} - d_{lu} \end{aligned} \tag{6}$$

if $Su > 0$.

With the three nearest vectors and their duty cycles defined, the best switching state must be chosen. Generally, switching states are defined previously, as in this work, or based on currents and voltages of the multilevel inverter [27], or defined by a fixed sequence [34]. The selection of the switching state for the 5L-SHI is done as follows:

- The dc sources of the multilevel inverter cell should not be employed at the same time, preventing unnecessary losses by them.
- The transition through switching states should be realized with minimum switching events, just one switching event always as possible.

Two types of the switching sequence for the SMV are presented in this paper, the switching sequence with seven segments (SVM-7) and five segments (SVM-5). The switching sequence with seven segments is a symmetric sequence and divides the switching time T_s into seven parts, as shown in Figure 6 where, T_a, T_b and T_c are the switching times for each switching event.

This distribution of the switching sequence in the switching time T_s improves the quality waveform of the output phase voltage, and, consequently, decreases the THD.

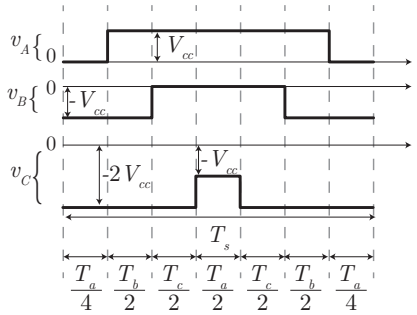

Fig. 6. The switching sequence with seven segments.

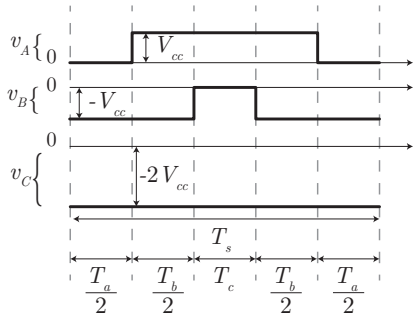

Fig. 7. The switching sequence with five segments.

Another symmetric switching sequence that can be employed is the five segments, as shown in Figure 7. The SVM-5 has a lower number of switching events than the SVM-7 and HM strategies in a time period T_s, resulting in lower switching losses in the power semiconductors. To verify semiconductors losses for each modulation schemes, the methodology proposed in [36] is applied. So, the conduction losses in the semiconductors are defined by:

$$P_{c,S/D} = V_{TO} I_{S/D,avg} + r_T I^2_{S/D,rms} \tag{7}$$

where:
V_{TO} - semiconductor drop voltage;
r_T - series semiconductor resistance;
$I_{S/D,avg}$ - average current in the semiconductor;
$I_{S/D,rms}$ - rms current in the semiconductor.

The switching losses in the semiconductor are defined by the dissipated energy in each switching

$$E\left(i_{S/D}\right) = k_0 + k_1 i_{S/D}\left(\omega_o t\right) + k_2 i^2_{S/D}\left(\omega_o t\right) \tag{8}$$

where:
$k_{0,1,2}$ - constants of the energy losses;
$i_{S/D}\left(\omega_o t\right)$ - rated current in the semiconductor.

So, the switching losses in a fundamental period in the semiconductors are given by:

$$P_{sw}\left(i_{S/D}\right) = \frac{K_c}{2\pi} \int_0^{2\pi} f_c E\left(i_{S/D}\left(\omega_o t\right)\right) d\left(\omega_o t\right) \tag{9}$$

where:
K_c - switching-loss factor;
f_c - switching frequency (carrier frequency).

In Figure 8, the semiconductors losses in the 5L-SHI is verified with all modulation schemes. The switching losses have been estimated with the parameters from Table II.

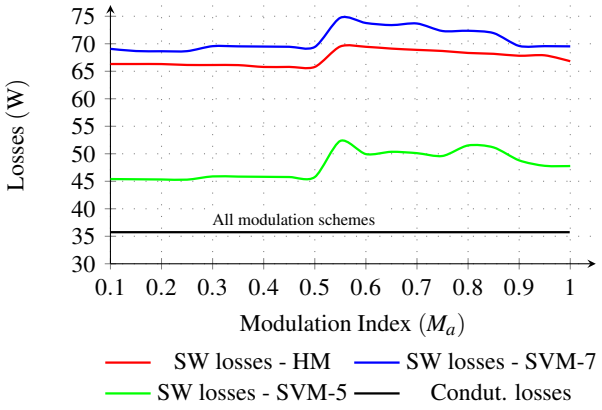

Fig. 8. Semiconductor losses in the 5L-SHI for different modulation schemes.

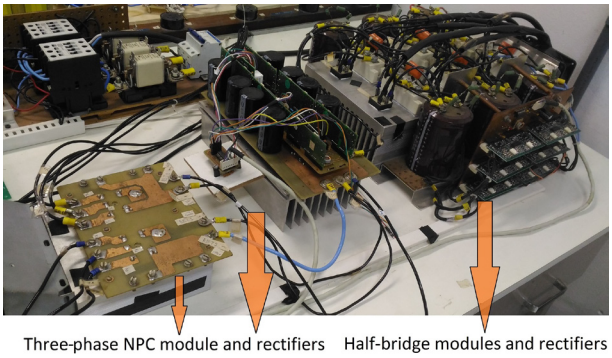

Fig. 9. Hardware structure of the 5L-SHI.

Figure 8 shows that the SVM-5 has lower results for switching losses than the SVM-7 and HM strategies for all modulation indexes. A little difference is perceived in the switching losses between the SVM-7 and HM, which can be explained by the fact that the SVM-7 has more than one switching event in some transitions of the switching states. It is important to notice that, for modulation indexes up to 0.5 just the half-bridges converters are switching, for modulation indexes higher than 0.5 the NPC cell starts to switch in low frequency, for all modulation schemes. When the NPC cell switches the half-bridge cells switches too. So, the semiconductor switching increase $4\% - 10\%$ for modulation indexes higher than 0.5, increasing the switching losses as shown in Figure 8. On the other hand, the inverter conduction losses do not change for all modulation schemes, but the conduction losses are different in each semiconductor for each modulation scheme.

IV. EXPERIMENTAL RESULTS

The 5L-SHI is verified by an experimental prototype shown in Figure 9. The prototype is composed of three-phase transformers to promote isolation of the dc source (rectifiers) for the half-bridge cells and the three-phase NPC. These half-bridge IGBT modules are rated for 600 V and 75 A. The NPC inverter cell is implemented with a Semikron IGBT module (SK50MLI066) and rated for 600 V and 60 A. The parameters of the inverter are described in Table II.

The HM, SVM-7 and SVM-5 are done with a Digital Signal Processor (DSP), model TMS320F2812. For HM

TABLE II
Experimental System Parameters for 5L-SHI.

SYSTEM PARAMETERS	
$V_{RMS} = 380$ V	supply voltage (line-to-line)
$f_r = 60$ Hz	supply frequency
$V_y = V_x = 400$ V	dc-link voltage
$f_c = 5760$ Hz	switching frequency
$f_o = 60$ Hz	output voltage frequency
$L_o = 93.3$ mH	load induction
$R_o = 77\ \Omega$	load resistance

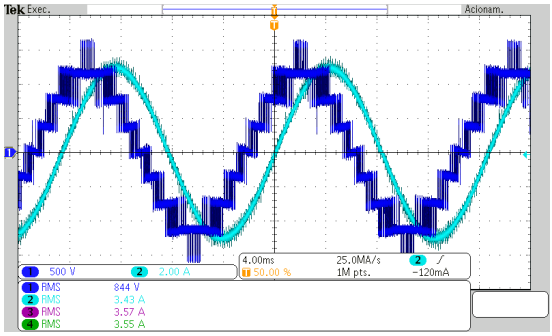

Fig. 10. Output waveform of the line voltage and phase current of the 5L-SHI with HM strategy, $M_a = 0.9$ (500 V/div) and (2 A/div).

the gate signals for the half-bridge cells are generated in an open-loop scheme and use the DSP's event manager PWM (EVA-PWM). This event manager configures the DSP PWM modules, where the switching frequency of the PWM modules is set at 5760 Hz. On the other hand, the gate signals for the NPC switches are generated by I/O output pins by comparing the sinusoidal reference V_{ref} with $\pm 1/2$ and 0. In the SVM, all gate signals are generated by I/O output and it uses the DPS's event manger to manage the switching event.

Figure 10 shows the output line voltage v_{AB} and output current i_A for HM strategy for modulation index $M_a = 0.9$. In the experimental waveform, the nine levels at the output line voltage v_{AB} are verified and the lowest value of the THD, approximately 15.2%. For all the experimental results are just presented a output line voltage and a output phase current, once, the experimental results for the others output line voltages e output phase currents are similar.

The results of the SVM-7 are shown in Figure 11, and the nine steps at all output line voltages are well defined and the output phase current is practically sinusoidal. The SVM-7 has similar switching events compared to the HM and consequently similar switching losses and THD, approximately 15.4%. The similar switching events are due to the requirement imposed for the SVM-7.

Figure 12 shows the output line voltage v_{AB} and the output current i_A for SVM-5 with modulation index $M_a = 0.9$. The experimental results show the nine steps at output line voltage and the lowest value of the THD, approximately 15.7%

The active power flow at the 5L-SHI can be verified in Figure 13 for the entire range of modulation indexes, ensuring the safe operation of the 5L-SHI with unidirectional power sources. It is important to emphasize that the most part of the active power is processed by the three-phase NPC cell for high modulation indexes, which enables the reduction of the

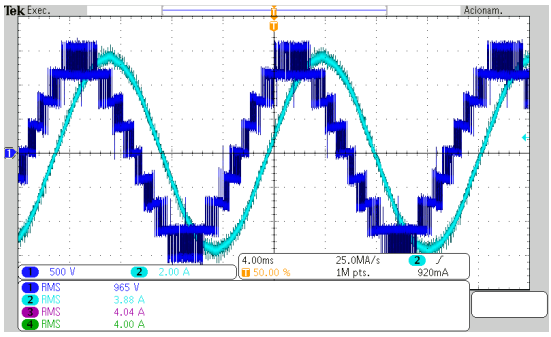

Fig. 11. Output waveform of the line voltage and phase current of the 5L-SHI with SVM-7 strategy, $M_a = 0.9$ (500 V/div) and (2 A/div).

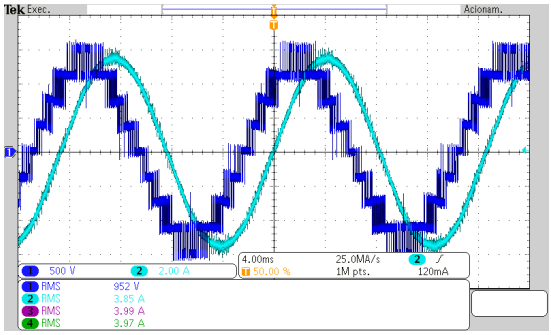

Fig. 12. Output waveform of the line voltage and phase current of the 5L-SHI with SVM-5 strategy, $M_a = 0.9$ (500 V/div) and (2 A/div).

capacitor size in the voltage dc source of the half-bridge cells.

The quality of the output line voltage waveform between the HM and SVM can be compared using THD analysis, as shown in Figure 14. A small difference in the THD analysis between the modulation schemes and the good results for modulation index up to 0.3, justify and enables a wide range of applications of the 5L-SHI using of the three modulation scheme. The THD analysis of the experimental results and of the simulation results of the output waveform have great similarity, with differences lower than 5% between experimental and simulation results.

It is important to emphasize that the SVM is more complex than the HM. While the HM can be done with some command lines in C language, the SMV, due to the real-time math operations, demands more time and more command lines, requiring a better hardware structures. However, power inverters usually uses powerful DSPs to command all the protections, switches and the auxiliary functions and this restriction does not impact in the project cost or its application.

V. CONCLUSIONS

This paper has presented two modulation schemes to drive the five-level symmetric version of the hybrid multilevel inverter (5L-SHI). The HM and the SVM provide benefits for the inverter such as, low-frequency switching in the NPC cell, which allows to decrease the semiconductor losses employing semiconductors with low conduction losses in the NPC cell. Unidirectional dc sources can be employed for both modulation schemes and in high modulation indexes the most part of the active power that flows through the inverter is processed by the dc source of the NPC cell, which leads a size reduction of the capacitors and rectifiers

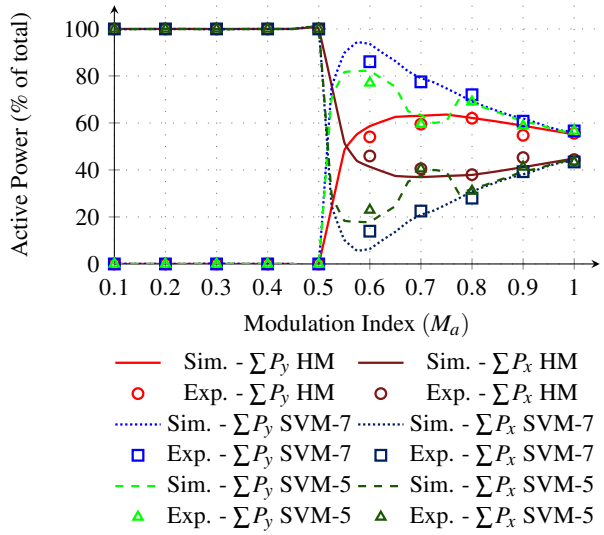

Fig. 13. Active power handled by the dc sources V_y and V_x in the 5L-SHI.

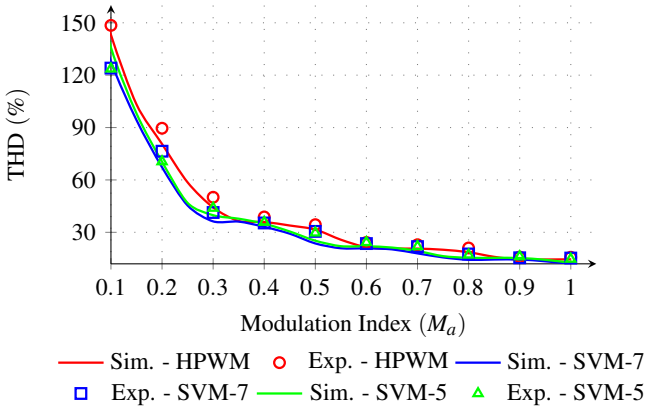

Fig. 14. THD analysis of the output line voltage waveform: simulation and experimental results.

of the half-bridge cells. The HM scheme has a simple implementation and it is easily implemented in a DSP. The SMV is more complex and its math operations requires better DSP than the HM. However, that is not a problem, once multilevel inverters already use powerful DSPs for the inverter management, and in high-power inverters the DSPs are not the costliest components. So, the SVM is an alternative to lead the multilevel inverters. The results of the THD are similar for all modulation schemes, especially for high index modulation. However, the SVM-5 has the best results for switching losses of the inverter compared to the HM and the SMV-7. This difference is due to the fact that the SMV-5 presents fewer switching events than the SVM-7 and the HM. Both modulation schemes have good results and enables a wide range of applications of the 5L-SHI.

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BIOGRAPHIES

Marcos Vinicius Bressan received the B.S. and M.S. degree in electrical engineering from the Santa Catarina State University, Brazil, in 2012 and 2014, respectively. He is currently pursuing the Ph.D. degree in the same University.

Since 2012, he is a power electronics researcher in the Electrical Power Processing Group - nPEE. His research interest includes multilevel converters, multilevel modulations and control systems.

Marcelo Lobo Heldwein (S'99 - M'08 -SM'13) received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianopolis, Brazil, in 1997 and 1999, respectively, and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH Zurich), Zurich, Switzerland, in 2007.

From 1999 to 2003, he worked with industry, including research at the Power Electronics Institute, Brazil and Emerson Network Power, Brazil and Sweden. He was a Postdoctoral Fellow at the ETH Zurich and at the UFSC from 2007 to 2009. He is currently an Adjunct Professor with the Department of Electronics and Electrical Engineering, UFSC. His research interests include power electronics, advanced power distribution, and electromagnetic compatibility.

Dr. Heldwein is a Member of the Brazilian Power Electronic Society

Alessandro Luiz Batschauer (S'09 - M'11) was born in Balneário Camboriú, Brazil, in 1977. He received the B.S., M.Sc. and Ph.D degrees in electrical engineering and from Federal University of Santa Catarina (UFSC), FlorianópolisSC, Brazil, in 2000, 2002 and 2011, respectively.

Since 2002, he has been with Department of Electrical Engineering, Santa Catarina State University. His fields of interest include high-frequency switching converters, power quality, multilevel converters and impedance source converters.

Mr. Batschauer is currently a member of the IEEE and Brazilian Power Electronic Society (SOBRAEP).