Digital Implementation of Three-Phase Rectifier with Deadbeat Controller

Alisson Dias Junqueira, Lourenço Matakas Jr., Wilson Komatsu
Dept. of Electrical Energy and Automation Engineering - PEA
University of São Paulo - USP
Av. Prof. Luciano Gualberto, trav. 3, no. 158 – 05508-900 - São Paulo, SP – BRAZIL
Phone: +55 (11) 3091-5483 - Fax: +55 (11) 3091-5719 - e-mail: alisson@pea.usp.br

***Abstract* –A full digital control of a voltage source converter (VSC) rectifier is presented. The behavior of the AC and DC sides were modeled and used for the design of the AC current tracking controller and DC voltage regulator. The AC current control, based on the deadbeat strategy is presented in a simple and intuitive way. The DC side PI controller is designed based on the linearized model of the converter. A simple and efficient Phase Locked Loop (PLL) based on the deadbeat strategy is presented. The performance of the complete system is verified by numerical simulation and experimental results, validating the proposed model and control strategy. Effect of parameter mismatch is also discussed.**

I. INTRODUCTION

The growing use of non-linear loads in the electric power system (e.g. diode rectifiers) has increased the concern with the quality of the electrical energy. For low power, one-phase applications, the "full bridge diode rectifier + boost converter" topology has proved to be a good performance low cost solution [6]. For three-phase, higher power applications, requiring bi-directional power flow, a three-phase, full bridge, self-commutated converter operating in pulse width modulation (PWM) mode is a convenient choice [7]. Typical applications include rectifiers for AC drives, telecommunication equipments, etc.

This digest presents a PWM three-phase rectifier with digital signal processor (DSP) control, which aims the reduction of reactive power and harmonics at the AC side, and the regulation of the DC side voltage.

Section II describes the mathematical modeling of the three-phase VSC (voltage source converter), considering the AC and DC sides of the converter.

Many authors, including ref. [14], consider the deadbeat approach as a pole placement problem in the z domain, where all closed loop poles are placed in $z=0$. Reference [13] showed the deadbeat poles ($z=0$) as the solution of an optimal control problem, whose cost function has zero weighting factor to the inputs.

Some authors ([9][10][11][12]), develops the deadbeat approach for the second order plants (LC filter), and takes into account the instantaneous variation of the converter output voltage during a switching cycle. This paper applies the deadbeat strategy to the first order plant (L filter), and uses an intuitive and simple approach to obtain the controller equation. In this case, the converter output is considered constant and equal to its local average during the sample interval. No previous knowledge of discrete control theory is required.

The design of the DC control loop is carried out by linearizing the converter model and applying a PI controller plus a pre-filter strategy to accomplish the desired transient performance.

Sinusoidal signal, synchronized with the mains voltage are obtained by a simple and efficient PLL based on [2].

The performance of the control algorithms is verified by simulations (using MatLab) and by an experimental setup using a low power converter.

The control algorithms were implemented by using a dedicated DSP (digital signal processor) specially designed for power electronic applications.

II. MODELING OF VSC

A. AC side

Fig. 1 shows the VSC rectifier and its connection to the mains (three phase/three wire system) through equivalent inductors (L) (filter + transformer inductance). Terminal G_2, not present in the real converter, is used here in order to simplify the equivalent circuit modeling.

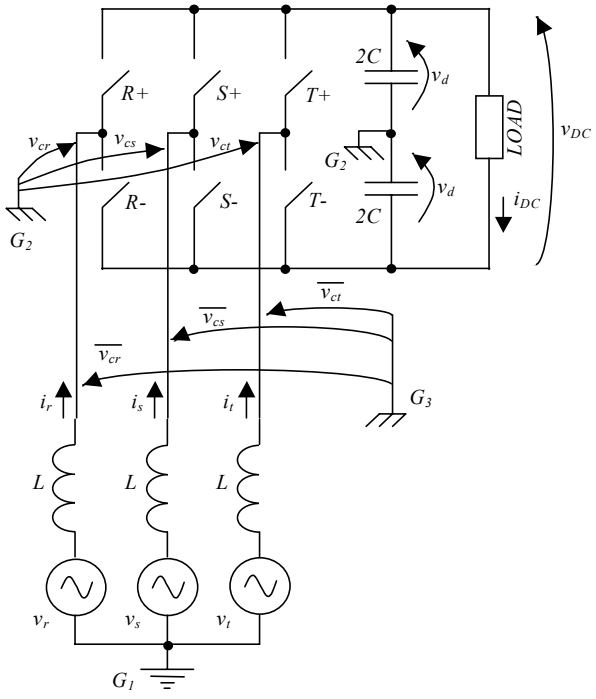

Fig. 1: Three-phase VSC model.

Fig. 2 introduces the simplified AC side model of the VSC, where the converter is modeled as three, wye connected ideal voltage sources. The sum of the three

individual mains voltages (v_r, v_s, v_t) is considered to be null (eq. 1).

$$v_r + v_s + v_t = 0 \quad (1)$$

The sum of the equivalent voltages at converter's AC side ($\overline{v_{cr}}, \overline{v_{cs}}, \overline{v_{ct}}$), defined by eq. 3.3 is also null (eq. 2).

$$\overline{v_{cr}} + \overline{v_{cs}} + \overline{v_{ct}} = \begin{bmatrix}1 & 1 & 1\end{bmatrix} \cdot \overline{\mathbf{v}_c} = \begin{bmatrix}1 & 1 & 1\end{bmatrix} \cdot \mathbf{B} \cdot \mathbf{v}_c = 0 \quad (2)$$

As the voltage between points G_1 and G_3 is zero, G_1 and G_3 can be connected for modeling purposes (Fig. 2).

Equation (3), in matrix form, can be obtained from Fig. 2.

$$\frac{d\mathbf{I}}{dt} = \frac{1}{L} \cdot \left(\mathbf{V} - \overline{\mathbf{V}_c}\right) = \frac{1}{L} \cdot \left(\mathbf{V} - \mathbf{B} \cdot \mathbf{V}_c\right) \quad (3)$$

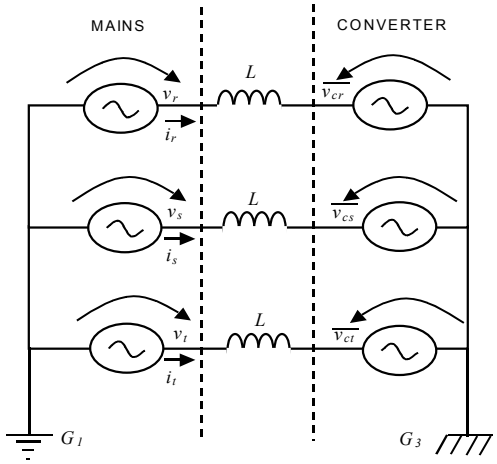

Fig. 2: Simplified AC side model.

The matrixes in eq. (3) are defined in equations 3.1 to 3.5:

$$\mathbf{I} = \begin{bmatrix} i_r \\ i_s \\ i_t \end{bmatrix} \quad (3.1), \qquad \mathbf{V} = \begin{bmatrix} v_r \\ v_s \\ v_t \end{bmatrix} \quad (3.2), \qquad \mathbf{B} = \frac{1}{3} \cdot \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \quad (3.3),$$

$$\mathbf{V}_c = \begin{bmatrix} v_{cr} \\ v_{cs} \\ v_{ct} \end{bmatrix} \quad (3.4) \quad \text{and} \quad \overline{\mathbf{V}_c} = \begin{bmatrix} \overline{v_{cr}} \\ \overline{v_{cs}} \\ \overline{v_{ct}} \end{bmatrix} = \mathbf{B} \cdot \mathbf{V}_c \quad (3.5)$$

The converter output voltages v_{cr}, v_{cs}, v_{ct} can assume the values $-v_d$ and $+v_d$ ($v_d = v_{DC}/2$ is the voltage on each capacitor drawn in Fig. 1). This results in eq. 3.6:

$$\mathbf{V}_c = \begin{bmatrix} v_{cr} \\ v_{cs} \\ v_{ct} \end{bmatrix} = \begin{bmatrix} m_r \\ m_s \\ m_t \end{bmatrix} \cdot v_d \quad (3.6)$$

The instantaneous modulation indexes m_r, m_s and m_t assume the values –1 or +1, and are written in a compact matrix forming eq. 3.7.

$$\mathbf{m} = \begin{bmatrix} m_r \\ m_s \\ m_t \end{bmatrix} \quad (3.7)$$

Eq. 4 results from (3), (3.6) and (3.7).

$$\frac{d\mathbf{I}}{dt} = \frac{1}{L} \cdot \left(\mathbf{V} - \mathbf{B} \cdot \mathbf{m} \cdot v_d\right) \quad (4)$$

B. DC side

Figure 3 presents the simplified model of DC side of a VSC. The PWM converter is represented by the current sources $\frac{m_r}{2} \cdot i_r$, $\frac{m_s}{2} \cdot i_s$ and $\frac{m_t}{2} \cdot i_t$, and the DC load by a current source i_{DC}. The voltage v_{DC} is the total DC link voltage ($v_{DC} = 2v_D$).

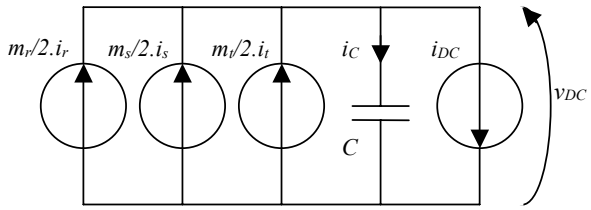

Fig. 3. Simplified model of VSC, at DC side

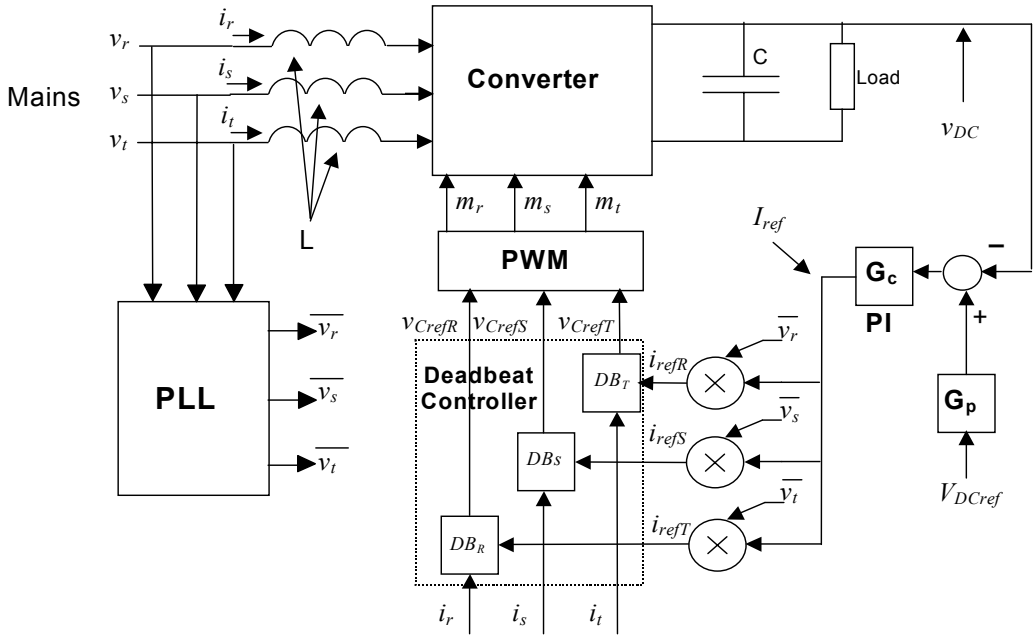

Fig. 4. Block diagram of system: converter and control blocks.

Equation (5) results from the circuit in Fig. 3, and equations 3.1 and 3.7.

$$\frac{dv_{DC}}{dt} = \frac{1}{C} i_C = \frac{1}{C}\left(\frac{m_r}{2} \cdot i_r + \frac{m_s}{2} \cdot i_s + \frac{m_t}{2} \cdot i_t - i_{DC} \right) = \\ = \frac{1}{C}\left(\frac{1}{2} \mathbf{I}^t \cdot \mathbf{m} - i_{DC} \right) \quad (5)$$

III. Control Strategy

A. General outline

The objective of the control strategy is to obtain sinusoidal AC currents in phase with the AC voltages (unitary power factor). DC side voltage is boosted above AC side peak voltage, and is regulated at the reference v_{DCref}.

For the AC side current tracking, a deadbeat control strategy was used [5][7][8][9][12]. The DC side voltage control adopts a proportional-integral controller (PI). There are, thus, AC current and DC voltage control loops [1][2][4][5][6][10][11].

Fig. 4 schematically exhibits the previously described blocks, and also the PLL block, which generates reference sinusoidal signals $\overline{v_r}$, $\overline{v_s}$, $\overline{v_t}$ with amplitude equal to one, synchronized with mains voltages v_r, v_s, v_t. The PLL block generates a pulse train synchronized with the mains, which are used by the sample/hold and PWM blocks [2].

B. Current loop

The AC current control strategy, based on the deadbeat approach, is illustrated in Fig. 5 for the one phase case. The controller aim is to nullify the error in the $(k+1)^{th}$ sampling instant, independent of the error in the previous k^{th} instant.

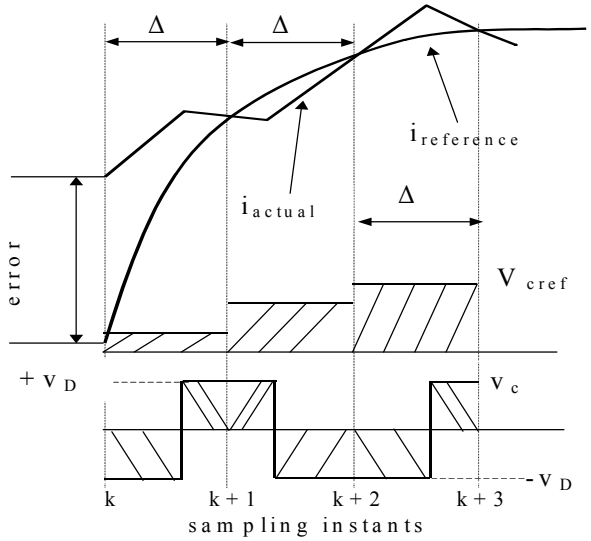

Fig. 5. Deadbeat behavior diagram.

In order to obtain the deadbeat behavior, it is necessary to impose $v_c(k)$ at the k^{th} sampling time, resulting in eq. (6).

$$i(k+1) = i_{ref}(k+1) \quad (6)$$

Eq. (7) can be written for each one of the phases.

$$\frac{di}{dt} = \frac{1}{L} \cdot \left(v - \overline{v_c} \right) \quad (7)$$

Integration of eq. (7) results in eq. (8).

$$\int_{i(k)}^{i(k+1)} di = \frac{1}{L} \cdot \int_{t(k)}^{t(k+1)} (v - \overline{v_c}) d\tau \quad (8)$$

If the mains voltage can be considered constant during the time interval Δ, the left side of (8) can be written, as shown in eq. (9).

$$i(k+1) - i(k) = \frac{1}{L} \cdot (v(k) \cdot \Delta - v_{cref}(k) \cdot \Delta) \quad (9)$$

The variable Δ is the sampling period.

Substituting eq. (6) in eq. (9), results in eq. (10).

$$i_{ref}(k+1) = i(k) + \frac{1}{L} \cdot (v(k) - v_{cref}) \cdot \Delta \quad (10)$$

From eq. (10), v_{cref} can be written as shown in eq. (11).

$$v_{cref}(k) = -\frac{L}{\Delta} \cdot \left(i_{ref}(k+1) - i(k) \right) + v(k) \quad (11)$$

The AC side model presented in Fig. 2 suggests the use of three independent current controllers for the three phases. An analysis of eq. (3), with the non-diagonal matrix B, shows the existence of a coupling between the three phases. A change in v_{cr}, for example, will affect the other two phases. It happens because the converter equivalent voltages $\overline{v_{cr}}$, $\overline{v_{cs}}$ and $\overline{v_{ct}}$, responsible for imposes the line currents are different from the original set of converter voltages v_{cr}, v_{cs} and v_{ct}. The line currents waveform will be slightly different from the ones shown in Fig. 5, but will be coincident at the sampling time [14]. This fact make possible the use of three independent dead beat controllers in spite of the existing coupling between the three phases.

Thus, one has three reference voltages v_{CrefR}, v_{CrefS}, v_{CrefT} updated twice each switching cycle and applied to a PWM generator with asymmetric sampling.

C. DC voltage loop

The DC voltage control loop (Fig. 4) is implemented with the DC voltage feedback through a PI controller, which generates a reference current I_{ref}, multiplied by the voltage references generated by the PLL block ($\overline{v_r}$, $\overline{v_s}$, $\overline{v_t}$) providing the reference currents (i_{refr}, i_{refs}, i_{reft}) for the deadbeat controller. Thus, the DC voltage controller acts on the amplitude of the AC side current (Fig. 4).

The open-loop transfer function relating the output voltage v_{DC} and the reference current i_{ref} can be obtained from Fig. 2 and 3. Equation (12) is obtained based on the instantaneous power relationship.

$$v_r \cdot i_r + v_s \cdot i_s + v_t \cdot i_t = i_r \cdot L \cdot \frac{di_r}{dt} + i_s \cdot L \cdot \frac{di_s}{dt} + \\ + i_t \cdot L \cdot \frac{di_t}{dt} + v_{DC} \cdot C \cdot \frac{dv_{DC}}{dt} + v_{DC} \cdot i_{DC} \quad (12)$$

Considering sinusoidal and low ripple AC currents in phase with the sinusoidal mains voltages, results in eq. (13.1, 13.2 and 13.3).

$$\mathbf{v} = V \cdot \mathbf{x} \quad (13.1)$$

$$\mathbf{i} = I_{ref} \cdot \mathbf{x} \tag{13.2}$$

Where:

$$\mathbf{x} = \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - \frac{2\cdot\pi}{3}) \\ \cos(\omega t + \frac{2\cdot\pi}{3}) \end{bmatrix} \quad \text{and} \quad x \cdot x^t = 3/2 \tag{13.3}$$

The parameters V and I_{ref} are the peak value of the mains voltage (v_r, v_s, v_t) and the reference currents $i_{refr}, i_{refs}, i_{refr}$.

The non-linear transfer function in eq. 14 is obtained from eq. (12) and eq. (13).

$$V \cdot \mathbf{i}^t = V \cdot I_{ref} \cdot 3/2 = C \cdot v_{DC} \cdot \frac{dv_{DC}}{dt} + v_{DC} \cdot i_{DC} \tag{14}$$

Linearization is applied around steady state operation point $(\overline{v_{DC}}, \overline{I_{ref}})$. The signals v_{dc} and I_{ref} are rewritten according to eq. (15).

$$\begin{aligned} v_{DC} &= \overline{v_{DC}} + \Delta v_{DC} \\ I_{ref} &= \overline{I_{ref}} + \Delta I_{ref} \end{aligned} \tag{15}$$

The linearized transfer function is given by eq. (16):

$$G(s) = \frac{\mathrm{K}}{\mathrm{T}\cdot s + 1} = \frac{V_{DC}(s)}{i_{ref}(s)} \tag{16}$$

Where:

$$\mathrm{T} = \frac{C \cdot \overline{v_{DC}}}{i_{DC}} \tag{16.1}$$

$$\mathrm{K} = \frac{V \cdot \mathbf{x}^2}{i_{DC}} \tag{16.2}$$

Equation (16.3) describe the transfer function of the PI controller $G_C(s)$.

$$G_C(s) = K_P + \frac{K_I}{s}, \tag{16.3}$$

Considering the pre-filtering function $G_P(s)$ (eq. 17.1), the closed-loop transfer function of the system is given by eq. (17).

$$G_T(s) = \frac{s\cdot K\cdot K_P + K\cdot K_I}{s^2 + s\cdot\left(\frac{1+K\cdot K_P}{\mathrm{T}}\right) + \frac{K\cdot K_I}{\mathrm{T}}} \cdot G_P(s) = \frac{V_{DC}(s)}{V_{DCref}(s)} \tag{17}$$

The PI controller constants, K_P and K_I are chosen in order to obtain optimum ITAE performance [16]. The closed-loop transfer function zeros are eliminated by introducing the pre-filtering $G_P(s)$ (Fig. 4). $G_P(s)$ is given by eq. (17.1).

$$G_P(s) = \frac{1}{s\cdot K\cdot K_P + K\cdot K_I} \tag{17.1}$$

Applying a settling time value equal to two main cycles and damping ratio of 0.7, the close-loop transfer function result is eq. (18).

$$G_T(s) = \frac{1}{s^2 + s\cdot 239{,}4 + 29241} \tag{18}$$

D. PLL block

PLL block generates three sinusoidal references $(\overline{v_r}, \overline{v_s}, \overline{v_t})$ in phase with each one of the reference voltages v_r, v_s and v_t (measured at the AC side of the converter) [2]. PLL block also synchronizes the sampling and switching pulses and, together with the deadbeat controller, guarantees null phase displacement between current and voltage signals at the AC side. Fig. 6 illustrates PLL operation for one phase.

For a given fixed number of sampling pulses per cycle of the mains voltage (PPC), the PLL block forces the first sampling pulse (CA=0) to be coincident with the rising zero crossing of the reference AC voltage (Fig. 6), and inserts "PPC' equally spread sampling pulses per mains cycle. At the beginning of each cycle (CA=0) the algorithm calculates the error, according to eq. 19.

$$error = |PPC - CA| \tag{19}$$

"CA" is the sampling pulse number counter. CA is reset after counting "PPC" pulses. With this error information, the PLL recalculates the next sampling period width Δ that forces the next pulse with CA=0 to be coincident with a positive zero crossing of the mains voltage, ensuring synchronization.

The PLL algorithm is applied only for the phase *r*. Its corresponding sinusoidal output $\overline{v_r}$ is obtained through a

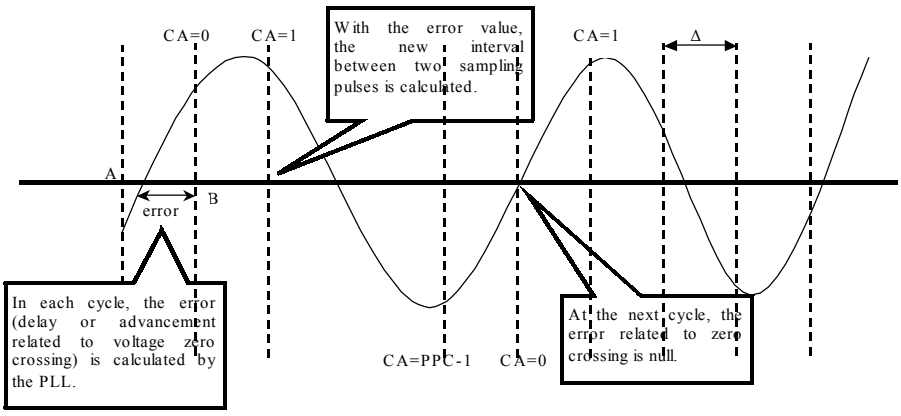

Fig. 6. PLL operation diagram.

look up table. In this work, the signals $\overline{v_s}$ and $\overline{v_t}$ are calculated to make the set $\overline{v_r}, \overline{v_s}, \overline{v_t}$ equally displaced waveforms. The mains phase sequence must be measured during the initialization process of the control program.

IV. NUMERIC SIMULATION

The system was simulated using MATLAB. The following results show simulation with DC capacitor initially charged with nominal DC voltage and inductors with null current at initial instant.

Simulations were carried with:

- DC voltage: $v_{DC}=350(V)$
- DC load: $R=350(\Omega)$
- DC capacitor: $C=400(\mu F)$
- Line frequency: $f=60(Hz)$
- RMS line voltage: $v_{AC}=220(V)$
- PWM frequency: $f_{PWM}=6(kHz)$
- Line inductors: $L=165(mH)$
- Asymmetric sampling

Fig. 7 shows AC currents and Fig. 8 shows voltage and current at one of the AC phases (phase *r*).

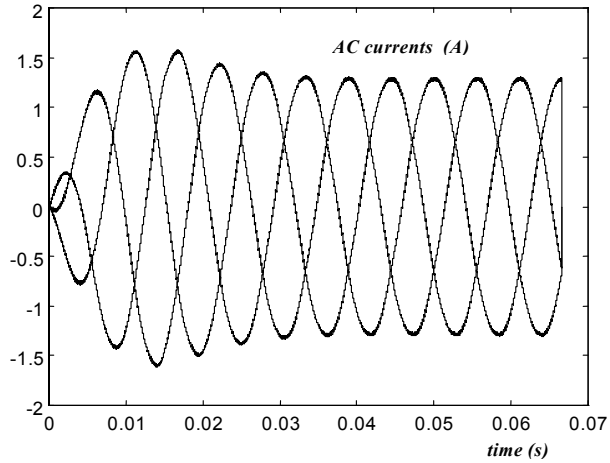

Fig. 7. Currents i_r, i_s and i_t , AC side (simulation).

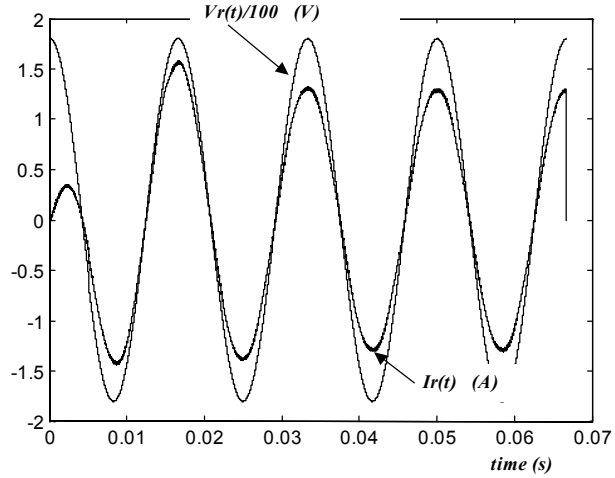

Fig. 8: Voltage (V/100) and current, phase r (simulation).

System behavior with plant disturbances was also simulated. Fig. 9 shows voltage and current waveforms at phase *r*, with the system exposed to disturbances. Fig. 10 shows the result of these same disturbances at the output DC voltage. Five perturbation stages can be distinguished: A. System is energized; B. 10% over voltage step at AC side; C. returns to the nominal AC voltage; D. DC load is removed (load rejection); and E. full load is reintroduced.

Overshoots at v_{DC} due to full load insertion are lower than 3%. Transient at v_{DC} vanish in periods shorter than two main cycles, as specified in item III-C.

It is worth noticing in Fig. 9 the AC current reverse during period D, returning the energy stored in the capacitor after a load rejection to the mains.

Fig. 9 also shows that the disturbances caused by AC voltage fluctuation are adequately compensated.

Fig. 11 shows harmonic content for AC line current *ir(t)*. One can see harmonic components around hundred times AC frequency, which corresponds to switching frequency. The harmonic amplitudes are around one percent of the fundamental current.

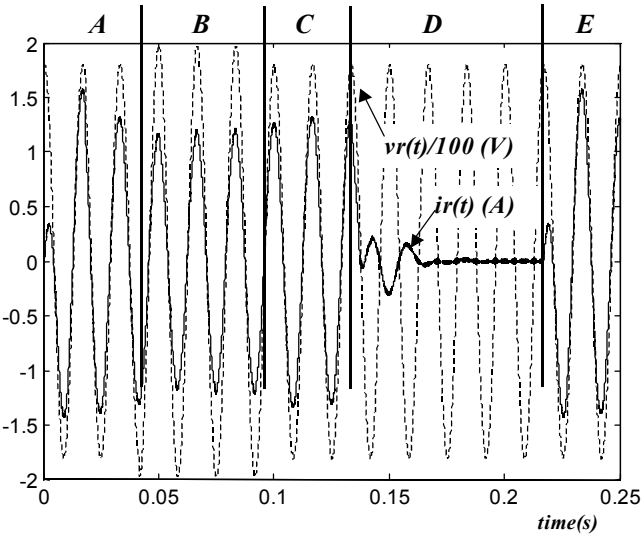

Fig. 9. Waveforms of voltage (V/100) and current in r phase, with disturbance (simulation).

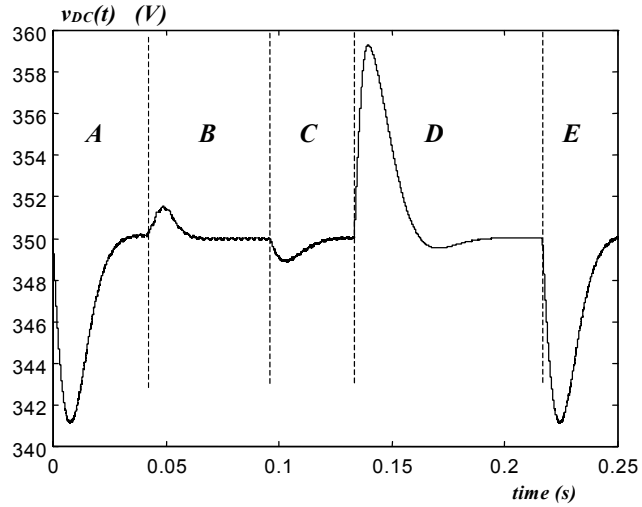

Fig. 10. Waveform of DC voltage in the output rectifier, with disturbance (simulation).

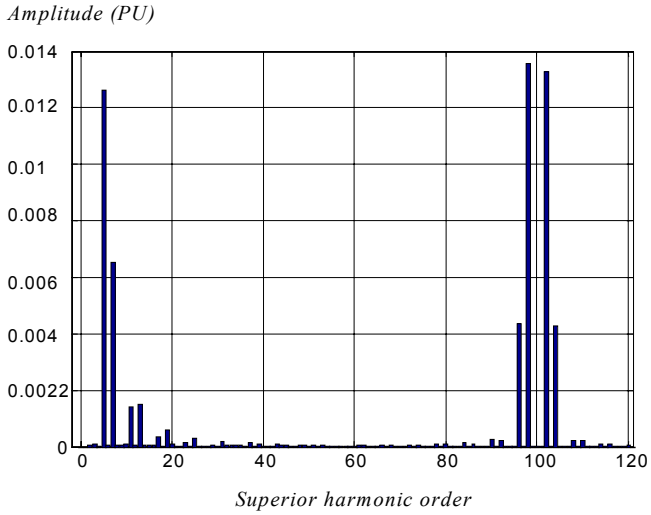

Fig.11: Harmonic content of current ir(t) (simulation – fundamental component (1 PU amplitude) is not shown).

V. INFLUENCE OF PARAMETER MISMACHES

There are two possibilities for parameter mismaches [8]. The first one occurs when a LC line filter is included between the mains conecting point and the rectifier (including the original inductance L) to minimize the AC current ripple. If the AC voltages are measured at the connecting point, the LC filter acts as a non modeled dynamic, that was not taken into account in equation (3), and will deteriorate the performance of the dead-beat controller.

The second case occurs when the equivalent inductance L assumes the value L_{DB} in the dead-beat algorithm, and L_A is its actual value. Reference [8] concludes that the closed loop system is instable for $L_{DB}/L_A > 2$.

Figures 12a, 12b and 12c show the behavior of the system for the limit case $L_{DB}/L_A = 2$. The line current *ir(t)* will not track the reference current, presenting amplitude and phase error (Fig. 12a). The DC loop is active, as can be seen in Fig. 12b, compensating the error of the V_{DC}, in spite of the error introduced by the current loop. Fig. 12c shows the displacement between v and *i*, decreasing the power factor (PF) to 0.9607.

Reference [8] also analyses the case where the AC voltage is estimated, requering no voltage sensor. For this case, instability is reached for $L_{DB}/L_A > 1.2$. Changes or differences between L_A and L_{DB} are more critical for this case.

In this paper, the mains voltage are measured at the input of the 'inductor L + rectifier' set. Even if a LC filter is included, the measuring point must not change. So the model shown in Fig. 2 is still valid, and the current loop will be robust.

Inductor resistance can also be taken into account. For a practical case, the quality factor Q ($Q = \omega L/R$) of the inductor can be considered around 10. For 60Hz mains, the time constant is $L/R = 26{,}5ms$, that is 156 times greater than the switching period (*0,1667ms*). For the above discussed values, the inductor can be considered as a pure inductance for the deadbeat algorithm.

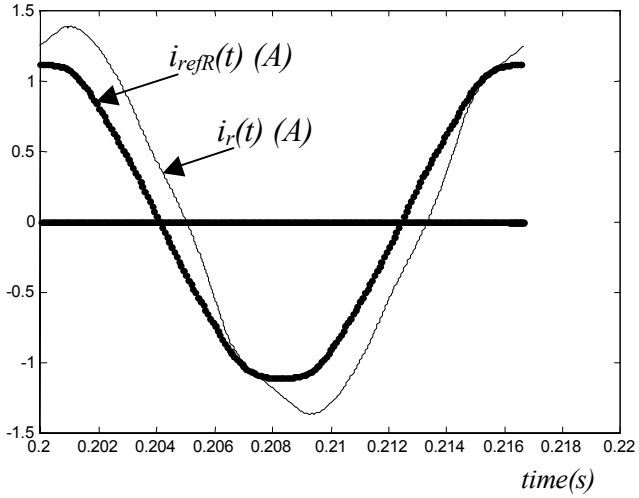

Fig. 12a. Reference current i_{refR} and current, phase *r*, with maximum mismatch in the inductor (simulation).

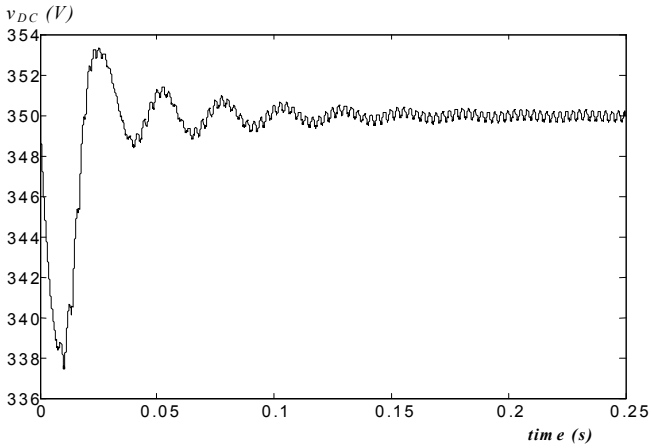

Fig. 12b. Waveform of DC voltage in the output rectifier, with maximum mismatch in the inductor (simulation).

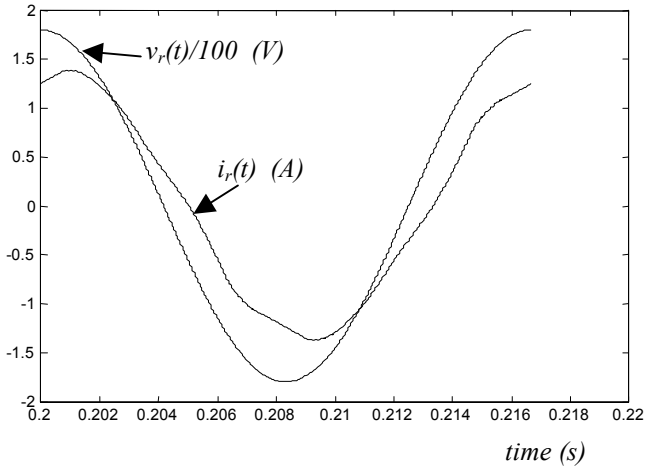

Fig. 12c. Phase *r*, voltage (v/100) and current, with maximum mismatch in the inductor (simulation).

VI. EXPERIMENTAL SETUP

The control algorithm was implemented in a DSP (Analog

Devices ADMC-401 [3], 16 bits, fixed point, 26MHz clock), specially designed for power electronics applications. This DSP includes as special features, an internal three-phase PWM generator and analog to digital (A/D) and digital to analog (D/A) converters.

Two AC line voltages and two AC line current are measured, allowing the calculation of the third line voltage and line current. Measurements are done with Hall effect voltage and current sensors (LEM LV25-P and LA25-NP).

The three-phase bridge converter, "in-house" developed, employs MOSFET transistors (IRF 840) and IRF2110 drivers.

This section introduces some experimental results.

Experimental values are:

- DC voltage: $v_{DC}=350(V)$
- DC load: $R=400(\Omega)$
- DC capacitor: $C=400(\mu F)$
- Line frequency: $f=60(Hz)$
- Line voltage: $v_{AC}=220(V)$
- PWM frequency: $f_{PWM}=6(kHz)$
- Line inductors: $L=100(mH)$
- Symmetric sampling

As in the simulated cases, no additional filter was included in the circuit of Fig. 1.

Fig. 13 show DC voltage, AC line voltage and AC line current waveforms. One can observe AC voltage distortion due to relatively low line regulation at the point of common coupling, as well as high frequency noise due to the lack of AC filter.

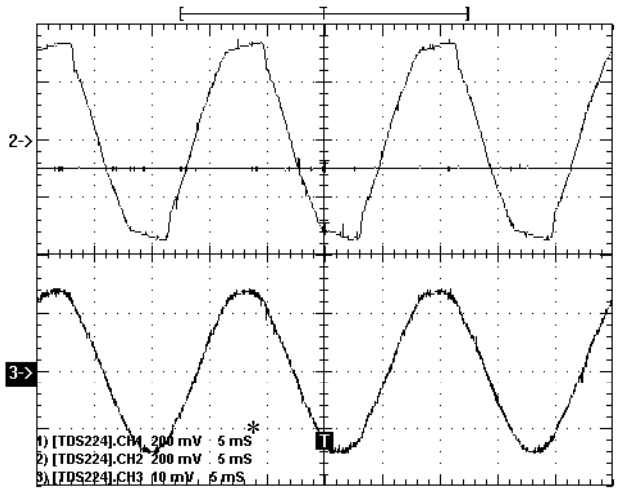

Fig. 13. Experimental waveforms of DC voltage (CH1-center) phase voltage (CH2-up) and line current (CH3-down). (Scales: CH1: 100V/div; CH2: 100 V/div; CH3: 1A/div). *

DC load variation was done changing load from $R=490(\Omega)$ to $R=360\ (\Omega)$ and vice-versa (Figs. 14 and 15). Test conditions show negligible DC voltage variation with load (partial) insertion and (partial) rejection.

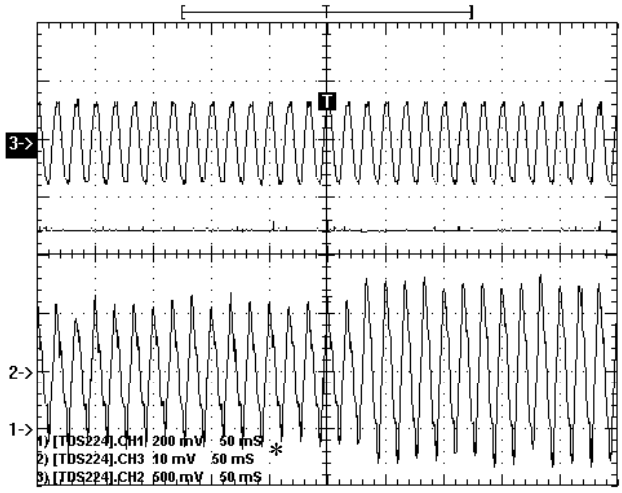

Fig. 14. Experimental waveforms of AC phase voltage (CH3-up), DC voltage (CH1-center) and line current (CH2-down), during a DC load insertion. (Scales: up: 250V/div; center: 100 V/div; down: 1A/div). *

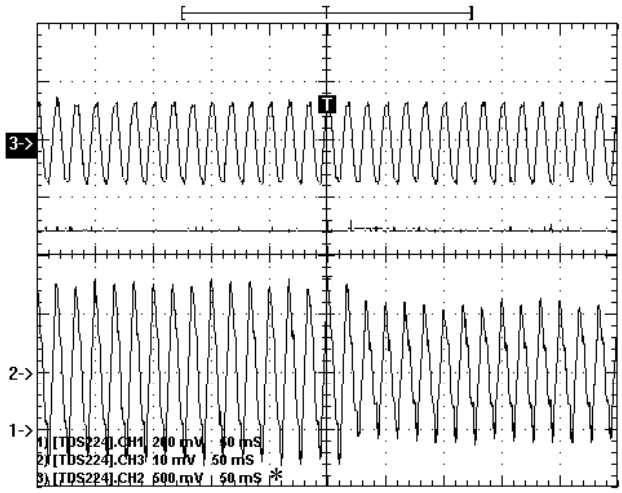

Fig. 15. Experimental waveforms of AC phase voltage (CH3-up), DC voltage (CH1-center) and line current (CH2-down), during a DC load partial rejection. (Scales: up: 250V/div; center: 100 V/div; down: 1A/div).*

Figs. 16 and 17 show complete DC load insertion and rejection (load value $R=400\ (\Omega)$). As Fig. 13 shows, it is difficult to see the effect on DC voltage variation. One can see that with no load current there is AC current, imposed by the voltage control loop in order to keep DC voltage constant, feeding converter (low) losses.

* The legend of the experimental results (*) does not show the real amplitudes, because the measurements were done with differential probes (voltages – Tektronix P5200) and current probes (Tektronix A6303 and A6303).

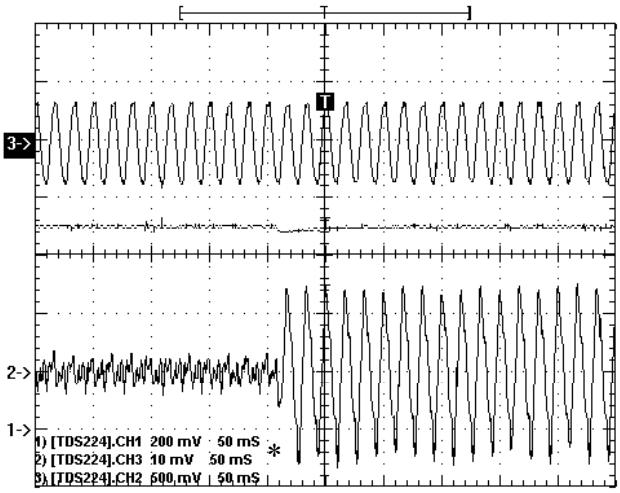

Fig. 16. Experimental waveforms of AC phase voltage (CH3-up), DC voltage (CH1-center) and line current (CH2-down), during a DC load connection. (Scales: up: 250V/div; center: 100 V/div; down: 1A/div).*

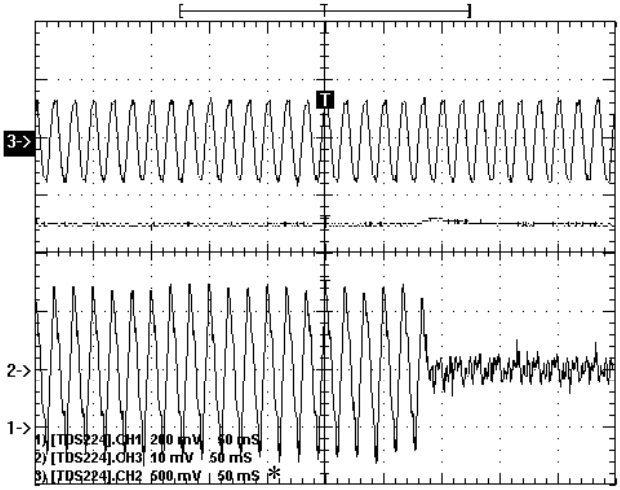

Fig. 17. Experimental waveforms of AC phase voltage (CH3-up), DC voltage (CH1-center) and line current (CH2-down), during a DC load connection. (Scales: up: 250V/div; center: 100 V/div; down: 1A/div).*

VII. CONCLUSIONS

A three-phase PWM rectifier with deadbeat current loop was presented. A simplified non-linear model was shown for the AC/DC converter. An intuitive approach was used for determining the deadbeat algorithm, which was shown to be robust even to large parameter mismatch. The linearized model of the converter was used for the design of the DC control loop. The fixed parameters PI controller showed good performance even for large transient in the load.

The parameters of linearized model depend on the operating point, affecting the performance and stability margin. This matter demands further analyses and will be treated in a future paper.

Also, an improved behavior of the AC current ripple can be easily obtained by the use of space vector modulation, which would require the deadbeat algorithm to be computed in the space vector domain.

It's well known that the space vector behavior can be obtained by adding a special zero sequence signal to the three references of the triangular PWM. A coming paper will show the merits of working in the *r,s,t* domain, with simple control algorithms, instead of working in the space vector domain.

A simple PLL, based on the deadbeat strategy, is designed and implemented in this paper.

REFERENCES

[1] Buso, S. "*Digital Control of Power Converters"* (Lecture notes), in http://www.dsce.fee.unicamp.br/~antenor/Digital.html;

[2] Matakas, L. Jr, Masada, E., Morizane, T., Koseki, S. "Full Digital Control of Power Electronics Converter Using Transputers" *Proceedings of the 4th Transputer/Occam International Conference*, June/92, Tokyo, Japan;

[3] ADMC401 Evaluation Kit – (http://www.analog.com/);

[4] Duarte, J.L.; Wintjens, J.A.A.; Rozenboom, J. "Advantages of a Fully Digitized Preconditioner". In: *International Conference on Power Quality: End-use Applications and Perspectives* – PQA'94, 3., Amsterdam, 1994. Proceedings. Amsterdam, KEMA, 1994, Vol.1.

[5] Komatsu, W.; Kaiser, W.; Matakas, L."PWM Current Source Converter with Deadbeat Control". In: *International Power Electronics Conference*, Tokyo, 2000. Proceedings. Tokyo, IEEJ, 2000, Vol.2, p.911-917;

[6] Qiao C.; Smedley, K.M.; "A Topology Survey of Single-Stage Power Factor Corrector with a Boost Type Input-Current-Shapper" In: *Applied Power Electronics Conference* 2000, Proceedings. Vol.1; p.460-467.

[7] Kazmierkowski, M.P.; Malesani, L. "Current Control Techniques for Three-Phase Voltage-Source PWM Converters: A Survey". *IEEE Transactions on Industrial Electronics*, Vol. 45, No. 5, October 1998. p. 691-703.

[8] Buso, S.; Malesani, L.; Mattavelli, P. "Dead-Beat Current Control for Active Filters". *IEEE* 1998.

[9] Kawamura, A.; Haneyoshi, T.; Hoft, R. G. "*Deadbeat Controlled PWM Inverter with Paràmeter Estimation Using Only Voltage Sensor*" *IEEE Transactions on Power Electronics*, Vol. 3, No. 2 April 1988.

[10] Kawamura, A.; Yokoyama, T. "Comparison of Five Different Approaches for Real Time Digital Feedback Control of PWM Inverters". *IEEE*, 1990.

[11] Kawamura, A.; Yokoyama, T. "Comparison of Five Control Methods for Digitally Feedback Controlled PWM Inverters". *EPE*, Firenze, 1991.

[12] Kawabata, T.; Miyashita, T.; Yamamoto, Y. "Dead Beat Control of Three Phase PWM Inverter" *IEEE Transactions on Power Electronics*, Vol. 5, No. 1, January 1990.

[13] Miguchi, Y.; Kawamura, A.; Hoft, R. "Optimal Pole Assignment for Power Electronics Systems". *Annual IEEE Power Electronics Specialists Conference*, Toulouse, 1985.

[14] Matakas Jr., L. "High Power, High Performance Parallel Connected Multiconverters: Analysis and Control" In: *11º Congresso Brasileiro de Automática*, São Paulo, SP. 1996, CBA.

[15] Astrom, K.; Wittenmark, B. *"Computer Controlled Systems – Theory and Design"* 2nd ed. Prentice-Hall International Editions. 1990.

[16] Dorf, R.; Bishop, R. *"Modern Control Systems"* 8ª ed. Addison-Wesley. 1998

BIOGRAPHICAL DATA

Lourenço Matakas Jr. obtained his undergraduate (1983) and graduate degrees (1989 and 1998) at the University of São Paulo. He worked as an Assistant Professor at the university of Tokyo and is now at the University of São Paulo, Catholic University of Sao Paulo, and Sao Judas University. His research areas are high power factor rectifiers, modeling and control of power converters, implementation of high power converters, and application of power converters to power systems.

Wilson Komatsu obtained his undergraduate degree in 1987, and graduate degrees (1992 and 2000) at the University of São Paulo. He is now an Assistant Professor at the University of São Paulo. His research areas are HVDC, modeling and control of power converters, implementation of high power converters, and application of power converters to power systems.

Alisson Dias Junqueira received the B.S. degree in electrical engineering from the University of São Paulo, Brazil in 2000. He is currently a post-graduating student in electrical engineering from the University of São Paulo.