

# REPETITIVE-BASED CONTROL FOR SELECTIVE ACTIVE FILTERS USING DISCRETE COSINE TRANSFORM

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**Abstract** -- This paper proposes selective harmonic current compensation using a closed-loop repetitive controller. The controller is based on measuring the line currents. It performs the compensation of specific harmonics selected by a DCT (Discrete Cosine Transform) digital filter, which is self-adjusted to track utility frequency deviations by means of a Phase Locked Loop (PLL) system. Compared to conventional solutions, this approach allows full compensation of selected harmonics, even if the active filter has limited bandwidth. This method also requires a simpler algorithm than, e.g., the synchronous frame harmonic regulators and its complexity is independent of the number of compensated harmonics. Moreover, it is more appropriate for DSP implementation and less sensitive to rounding and quantization errors when finite word length or fixed-point implementation is required. Simulations and experimental results confirm the theoretical expectations.

**Keywords** – Active filters, Discrete Cosine Transformation, Harmonic compensation, Phase-Locked Loop, Repetitive control, Selective Filtering.

## I. INTRODUCTION

The interest on Active Power Filters (APF) strategies capable of performing selective harmonic current compensation has increased in the last few years, especially for those applications where the harmonics produced by the loads are slowly varying [1-4]. Essentially, in the absence of severe dynamic requirements, control accuracy can be increased since the delay of the current control [6] can be compensated and instabilities or interactions [7,8] with possible dynamic components of the load can be reduced. Moreover, selective harmonic control reduces active filter's rating, since the compensation capability is only used to eliminate the desired harmonic components and could be used to ensure that individual [5] or total harmonic current distortion of a specific load does not exceed pre-defined recommended limits.

This paper proposes a new closed-loop selective harmonic compensation method. It uses the measurement of line currents and a repetitive-based control technique [10-14] to

achieve a very precise reference tracking in the presence of periodic distortion. In order to achieve compensation of only the selected frequencies and to provide a leading-phase needed for improving stability margin, a modified scheme using DFT (Discrete Fourier Transform) based filters, is proposed. A PLL system is used to provide frequency deviation immunity for such digital band-pass filters.

Moreover, it will be shown that this solution has some properties similar to those obtainable with closed-loop synchronous-frame regulators [1-4]. However, the proposed solution provides a more efficient algorithm, whose complexity is independent on the number of harmonics to be compensated and it features less sensitivity to rounding and quantization effects with a structure that suits very well Digital Signal Processors (DSPs) implementation, even if limited wordlength or fixed point arithmetic are used. Simulation and experimental results demonstrate the outstanding performance of the proposed solution.

## II. ACTIVE FILTERS USING REPETITIVE CONTROLLER

The diagram of Fig. 01 describes the proposed selective compensation method, using a closed loop repetitive-based structure. Following the scheme, line current references ( $i_s^{ref}$ ) are first evaluated using a conventional dc-link voltage regulation and supply voltages  $v_s$  (filtered by transfer function  $F_1$ , if necessary).

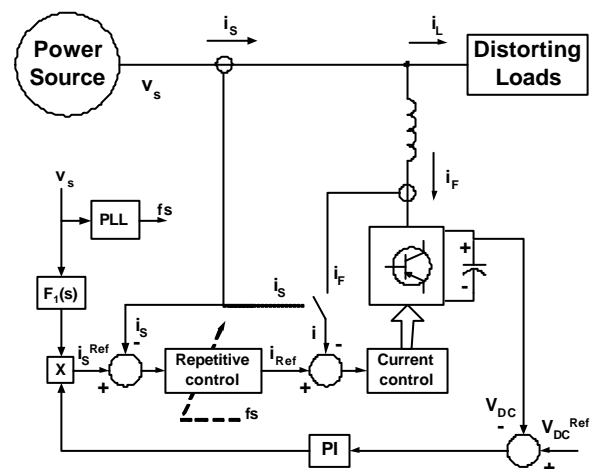


Fig. 01 – Diagram of a shunt APF using selective harmonic compensation based on repetitive control.

Manuscript received October 20, 2003. Revised March 02, 2004.

Recommended by Editor in Chief, Prof. Carlos Alberto Canesin.

Then, a repetitive controller is used for precise tracking of the selected frequencies. The output of this regulator gives the current references ( $i^{ref}$ ) for the active filter current control, which can be performed either on the active filter currents ( $i=i_F$ ) or on the line currents ( $i=i_S$ ). The former case is the preferable choice, mainly for over-current protection purposes, while the latter avoids the use of sensors for the active filter currents  $i_F$ .

Fig. 02 shows the basic structure of the proposed repetitive-based controller. The concept of repetitive control theory [10-14] is originated from the internal model principle [9,13,14], so that the controlled output tracks a set of reference inputs without steady-state errors if the model, that generates these references, is included in the stable closed-loop system.

For example, if the system is required to have a zero steady-state error to sinusoidal input, then the model of the cosine function (i.e.  $s/(s^2 + \omega_s^2)$ ), being  $\omega_s$  the corresponding angular frequency) should be included in the plant transfer function. In order to implement a repetitive control system, a periodical actuating signal must be generated and a possible digital implementation, which has already been applied to UPS and PWM converters [10-12], is shown in Fig. 2a, where  $N$  is the number of samples within one fundamental period. However, the scheme of Fig.2a usually leads to instability since it amplifies many high-order harmonics (theoretically up to the Nyquist frequency), while the system to be controlled has usually a limited bandwidth. For this reason a careful design of filter  $G_F(s)$  is needed in order to ensure stable operation [10].

Selective harmonic compensation presents different requirements if compared to the scheme of Fig. 2a, which provides compensation of all harmonic components. Moreover, leading-phase may allow stable operation and the compensation of high-order harmonics, even if the active filter presents limited bandwidth.

In order to ensure selective filtering and an adjustable leading phase, this paper proposes the use of "moving" or "running" DFT (Discrete Fourier Transforms) filters with a window equal to one fundamental period, such as:

$$F_{DCT}(z) = \frac{2}{N} \sum_{i=0}^{N-1} \left( \sum_{h \in N_h} \cos \left[ \frac{2\pi}{N} h(i + N_a) \right] \right) z^{-i}, \quad (1)$$

where  $N_h$  is the set of selected harmonic frequencies and  $N_a$  the number of leading steps determined by stability analysis. Indeed, (1) can be seen as a Finite Impulse Response (FIR) pass-band filter of  $N$  taps with unity gain at all selected harmonics  $h$  and it is also called Discrete Cosine Transform (DCT) filter [15]. One advantage of (1) is that the compensation of more harmonics does not represent any increase in the computational complexity (only a change on the filter coefficients without any additional calculation) and the leading-phase can be tuned at the design stage by parameter  $N_a$ . Finally, in order to implement a repetitive scheme for the selected harmonics, a delay of  $N_a$  steps is then needed in the feedback path to recover zero phase-shift

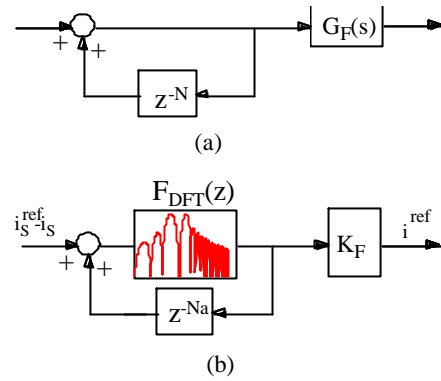


Fig. 02 - (a) General implementation of repetitive-based control; (b) proposed solution for active filter applications.

of the loop gain ( $F_{DCT}(z) z^{-N_a}$ ) at the desired frequencies, as described in Fig. 2b.

### III. ANALYSIS OF THE PROPOSED CONTROL

#### A. Regulator frequency response

Considering the simple case where only three frequencies have been selected: the fundamental, the 5<sup>th</sup> and 7<sup>th</sup> components, Fig. 03 reports the frequency response of the DCT filter. It is possible to notice that only at these three frequency components the gain is almost unity, the small differences being due to the superposition of spectral residuals.

Assuming that the transfer function between the current references  $i^{ref}$  and the line currents  $i_S$  is unitary, the Bode diagram of the open loop gain has been reported in Fig. 4, for  $K_F=1$  and  $N_a=0$ . As expected, the gain is theoretically infinite for the selected frequencies ensuring zero steady-state errors for these components. Moreover, the phase-shift of the open loop gain is zero, since  $N_a$  and the phase shift of the compensated process are zero in such example.

#### B. Transient response

Parameter  $K_F$  strongly determines the controller dynamic response, as it will be outlined in section E. In order to understand the performance of the proposed controller for active filter applications, a reference signal  $i_s^{ref}$  was simulated including the fundamental component (1pu), the 5<sup>th</sup> and 7<sup>th</sup> components, both with 50% amplitude of the fundamental. The results are reported in Fig. 05, which shows that the residual error is almost zero after one cycle.

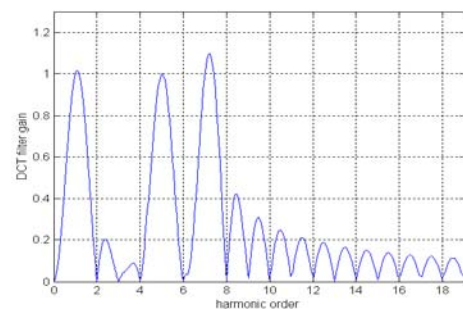


Fig. 03 – DFT frequency response using  $N_h=\{1,5,7\}$  and  $N_a=0$ .

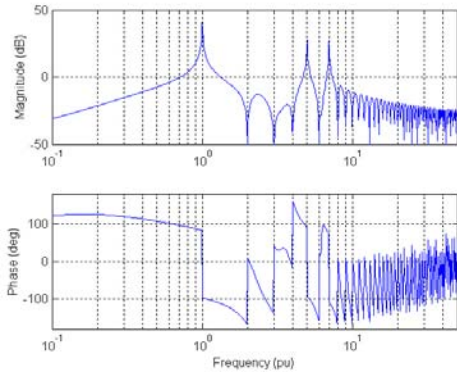


Fig. 04 – Bode diagram of open loop gain using  $N_h=\{1,5,7\}$ ,  $N_a=0$  and  $K_F=1$ .

### C. Supply frequency tracking based on digital PLL model

Since the proposed repetitive control is based on the compensation of the DCT frequency selection and considering that such filter uses a moving window based on the fundamental period, it is evident that the control is sensitive to supply frequency variations, as reported in [2].

Even if previous results [2,17] have shown that such performance is still good for active filter applications, a Phase-Locked-Loop (PLL) algorithm, that precisely tracks supply frequency variations is advisable in practical implementations. Thus, the authors propose the use of a fully digital PLL, which uses two line voltage measurements ( $V_{ab}$ ,  $V_{cb}$ ), as depicted in Fig. 06.

Summarizing, such PLL structure uses a proportional-integral (PI) controller to track the system angular frequency ( $\omega=2\pi f$ ) and a digital integrator to transform the evaluated angular frequency ( $\omega$ ) into the angular phase function  $q = \omega t$ . The digital PLL model also considers the sampling delay function, which represents the sampling process (sampling time  $T_s$ ). So, the approach is based on using the measured line voltages as the PLL input signals and two digital feedback signals ( $ua$  and  $uc$ ). Such internal signals are synthesized from the final evaluated angular frequency  $\omega$  or phase angle ( $q=\omega t$ ) and used to calculate the PLL instantaneous error.

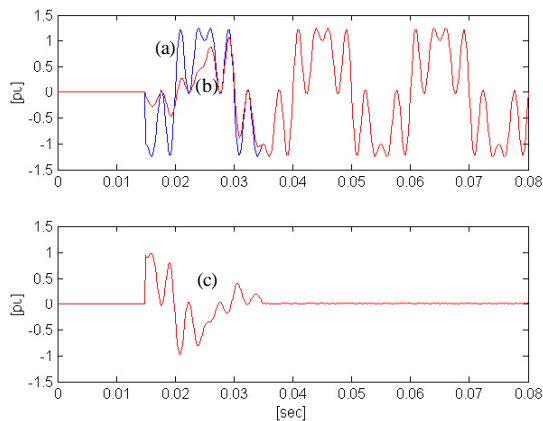


Fig. 05 – Transient response of the repetitive control structure: (a) reference  $i_s^{ref}$ , (b) output variable  $i_s$ , (c) error signal ( $i_s^{ref} - i_s$ ).

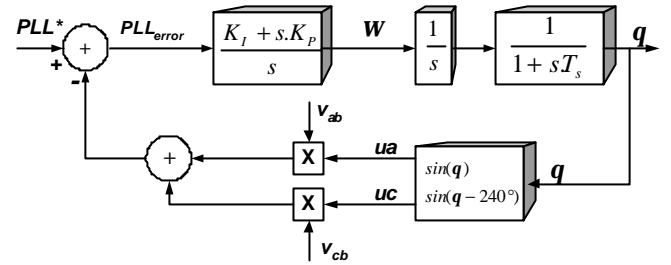


Fig. 06 – Generalized Power System PLL Model.

If the PLL reference is set to zero, the PLL tracking system will force the internal digital signals (and the phase angle) to be exactly orthogonal to the input voltages. Hence, the PLL system precisely evaluates the frequency ( $\omega$ ) and phase-angle ( $q - 90^\circ$ ) information of the input utility voltages. Thus, the PLL allows adjusting the sampling frequency ( $f_s$ ) to be a multiple of the supply frequency, so that the number of samples within a line period is always the same. This provision ensures that the frequency response of the digital filter (DCT) is not sensitive to supply frequency variations and the active filter compensation remains ideally 100% efficient for the selected harmonic components.

More details about the PLL design methodology and the digital implementation are discussed in [16]. Results in Section IV illustrate the PLL tracking performance.

### D. Similarity with synchronous frame harmonic control

The recent interest in selective harmonic compensation has produced several different control strategies [1-5]. However, starting from different points of view, it is roughly possible to summarize the proposals as a set of band-pass filters, where each filter realizes the compensation for a selected harmonic. So, it is possible to analyze the similarities between the proposed solution and the closed-loop synchronous frame harmonic control.

Considering a generic regulator, which includes the sum of pass-band filters, tuned to the selected frequencies:

$$R_h(s) = \sum_{h \in N_h} \frac{2K_{lh}s}{s^2 + (h\omega_s)^2} \quad (2)$$

The same regulator can also be written as [2]:

$$R_h(s) = K_F \sum_{h \in N_h} \frac{F_h}{1 - F_h},$$

where

$$F_h(s) = \frac{2\xi_h h\omega_s s}{s^2 + 2\xi_h h\omega_s s + (h\omega_s)^2} \quad K_F = \frac{K_{lh}}{\xi_h h\omega_s}, \quad (3)$$

being  $\xi_h$  the arbitrary damping factors for pass-band filter  $F_h$ , and  $N_h$  the set of selected harmonic frequencies. From (2) we observe that each of the original band-pass filters can be seen as a unity positive feedback of a band-pass filter  $F_h$  having unity gain and zero phase at the selected frequency  $h$ . Following this straightforward consideration and taking into account that  $\xi_h$  can be chosen as small as desired, (2) could be further approximated - only valid around the selected frequencies - by the following expression:

$$R_h(s) = K_F \sum_{h \in N_h} \frac{F_h}{1 - F_h} \approx K_F \frac{\sum_{h \in N_h} F_h}{1 - \sum_{h \in N_h} F_h}, \quad (4)$$

as long as all pass-band filters are very selective (i.e.  $F_{h1} * F_{h2} \ll F_{h1}, F_{h2}$ ). This is particularly true if we consider the moving or running DCT filters with a window equal to one fundamental period, such as:

$$F_{dh}(z) = \frac{2}{N} \sum_{i=0}^{N-1} \cos\left[\frac{2p}{N} h i\right] z^{-i}, \quad (5)$$

which realizes zero gain at the non-selected frequencies. One of the major advantages of (5) and approximation (4) is that the compensation of more harmonics does not add any increase in the computational complexity since

$$\sum_{h \in N_h} F_{dh}(z) = \frac{2}{N} \sum_{i=0}^{N-1} \left( \sum_{h \in N_h} \cos\left[\frac{2p}{N} h i\right] \right) z^{-i}. \quad (6)$$

Therefore, only a change on the coefficients of the FIR filter is needed for the compensation of more harmonics without any additional calculation. As a result, only a positive feedback of (5) is needed to perform an approximated frequency response of the harmonic control regulator  $R_h$ . This is the control structure proposed in Figs. 01-02, showing the similarity between the proposed solution and closed-loop synchronous frame harmonic control. However, this solution offers some important advantages, since the computational complexity is independent of the compensated harmonics and the control algorithm is much less sensitive to quantization and rounding errors for fixed-point implementation, as verified experimentally. Finally, the similarity between the proposed solution and closed-loop synchronous frame harmonic control can be easily extended introducing the leading steps  $N_a$ , which corresponds to a leading angle  $f_h$  (at the selected frequencies) for the pass-band filters.

#### E. Design criteria

Considering Fig. 02-b, the proposed control design is very simple, since it requires only the selection of the harmonics to be compensated, the design of gain  $K_F$  and the leading steps  $N_a$ . Regarding to the parameter  $K_F$ , the similarities with the synchronous frame control are used to explain its design. Indeed, each band-pass filter can be seen as an integrator in the reference frame rotating at frequency  $h$  [2] and thus, under the assumption of unity transfer function between  $i$  and  $i_s$ , the integrator gain  $K_{Ih}$  gain can be chosen

$$K_{Ih} = \frac{2.2}{n_{ph} T_S}, \quad (7)$$

where  $(n_{ph} T_S)$  is the desired response time (evaluated between 10% and 90% of a step response) for the generic harmonic  $h$ ,  $n_{ph}$  is number of fundamental periods  $T_S$ . Then, following the approximation of the previous section and using the same integral term  $K_{Ih}$  for all harmonics, we found out that  $K_F$  can be approximated by:

$$K_F \approx \frac{K_{Ih}}{0.32 w_s}. \quad (8)$$

Indeed, using  $K_F=1$ , we have a response time of 1.1 supply periods. Finally, parameter  $N_a$  should be chosen so as to provide a leading phase, which compensates the delay for the current control. It has been found experimentally that the leading of 2-3 sampling periods gives good results, although this number is directly related to the achievable bandwidth of the current control. After this preliminary design, a stability analysis is needed in order to verify that the overall closed-loop system has a proper phase margin especially for the higher harmonic frequencies.

## IV. EXPERIMENTAL RESULTS

The proposed solution has been experimentally tested based on the system of Fig. 1 and the parameters of Table I.

Regarding the digital implementation, due to the lower complexity and quantization sensitivity of this strategy, the digital controller has been performed by a single fixed-point DSP (ADMC401 by Analog Devices). The overall control algorithm (using PLL and the DCT based on 200 samples) requires only 55 $\mu$ s using a non-optimized assembly code, so that the control complexity is perfectly compatible with the implementation on commercial fixed point  $\mu$ C/DSP units.

The internal current control for the active filter has been implemented using the active filter currents (i.e.  $i=i_F$  in Fig. 01) and the same performance is expected in case the internal current control is implemented using directly the line currents (i.e.  $i=i_S$  in Fig. 01).

As far as the VSI current control is concerned, a proportional-integral (PI) algorithm has been chosen, with a design bandwidth of 1kHz and 70° phase margin. Regarding to the dc-link voltage regulation, a PI control has been used as well, designed with 10Hz bandwidth and 60° phase margin.

The first verification was done on the harmonic compensation of an uncontrolled rectifier. Using the PI current control, Fig. 7 shows the phase voltage, source  $i_S$  and load  $i_L$  currents, respectively. The spectra of the load and line currents are reported in Fig. 08 and Fig. 09, respectively. Note that there is only a small attenuation of the load harmonics, mainly due to the delay of the digital current control.

**Table I – Power system and control parameters.**

DC Link Voltage	450V
Filter Inductor $L_F$	4mH
Nominal Switching Frequency	12kHz
Line voltage (phase-phase)	220V <sub>rms</sub>
Nominal Load Power	5kVA
Selected frequencies ( $h$ ) - Case 1:	1 <sup>st</sup> , 3 <sup>rd</sup> , 5 <sup>th</sup> , 7 <sup>th</sup> , 9 <sup>th</sup> , 11 <sup>th</sup> , 13 <sup>th</sup> , 17 <sup>th</sup> , 19 <sup>th</sup>
Selected frequencies ( $h$ ) - Case 2:	1 <sup>st</sup> , 3 <sup>rd</sup> , 5 <sup>th</sup> , 7 <sup>th</sup> , 9 <sup>th</sup> , 11 <sup>th</sup> , 13 <sup>th</sup> , 17 <sup>th</sup> ...29 <sup>th</sup>
Current control definitions	1 kHz bandwidth, 70° phase margin
Required response time (number of line periods)	1
Leading sampling steps ( $N_a$ )	2
Gain $K_F$	1

It is worth noting that the residual harmonic distortion in Fig. 08 is not due to inverter saturation since the  $di/dt$  capability of the inverter could be able to perform the required compensation. In this condition, the evaluated load current THD is 24.9%, while the source current THD using the PI control is reduced to 12.3%, which is still significantly high.

As a comparison, we have tested the proposed control in the same conditions and the results are reported in Figs. 10-15.

In Fig. 10 the compensation of all odd harmonics up to the 19<sup>th</sup> harmonic was imposed and it is possible to note an improvement in the line current waveforms. Looking at the spectrum of line currents in this condition, which is reported in Fig. 11, it is possible to note that all selected frequencies have been well compensated, as theoretically foreseen. So, the THD is reduced to 3.2%, which attends most of international recommendations and standards.

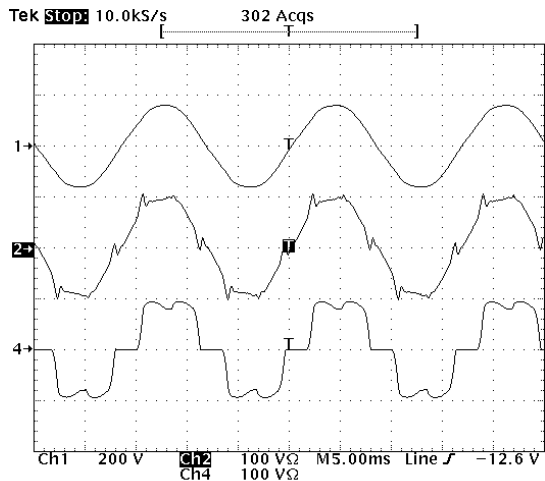


Fig. 07 – Line voltage  $v_S$  (200V/div), line current  $i_S$  (10A/div) and load current  $i_L$  (10A/div) using conventional PI control.

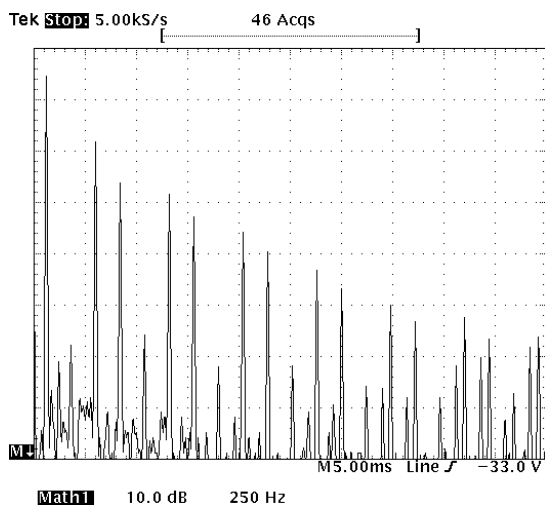


Fig. 08 - Spectrum of the load currents (10dB/div - 250Hz/div).

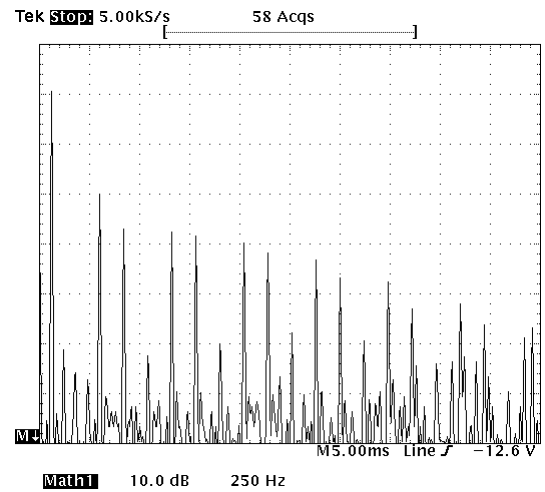


Fig. 09 - Spectrum of the source currents (10dB/div - 250Hz/div), using conventional PI control.

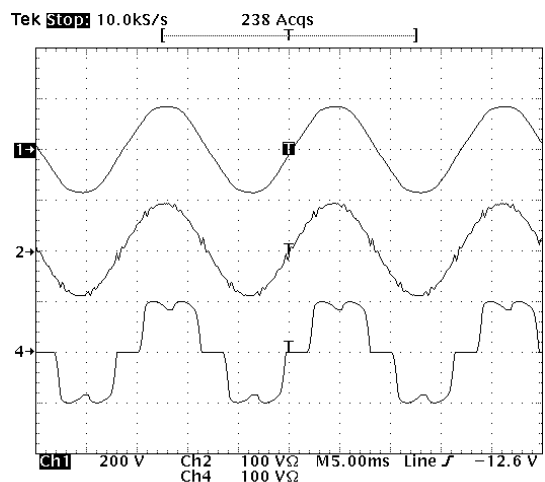


Fig. 10 – Line voltage  $v_S$  (200V/div), line current  $i_S$  (10A/div) and load current  $i_L$  (10A/div) using the selective control (Case 1).

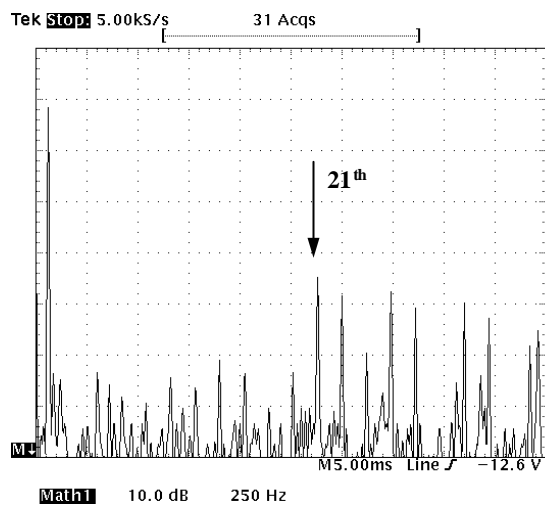


Fig. 11 - Spectrum of the source currents (10dB/div - 250Hz/div), using selective control (Case 1).

Considering an extended bandwidth, all odd harmonics up to the 29<sup>th</sup> harmonic, the results of the selective compensation are still better, as depicted in Fig. 12 and 13. The THD in such case is reduced to 1.8%.

Fig. 14 presents the dynamic response of the active filter if started when the load is running. Note that it takes approximately three fundamental cycles to completely compensate the load currents and such delay is mostly due to the PI regulator in the DC side. Moreover, the settling time under load variation is less than four fundamental cycles, as discussed in a previous work [17] and depicted in Fig. 15.

Since the PLL system has been used to precisely track the power system's frequency and this information is used to the on line adaptation of the sampling frequency, Fig. 16 shows the input voltage (lower trace) and its fundamental waveform (upper trace), which is digitally generated by the PLL, during a frequency step (continuous trace) from 50Hz to 60Hz. Note the line period changing from 20ms to 16.66ms (16.8ms due to the oscilloscope resolution). Such response is strictly dependent of the input voltage distortion and PLL internal gains. Such test was carried out using a programmable AC power source.

Regarding to the harmonic compensation and based on the comments of section II, it is almost evident that if no filtering ( $F_1$ ) were used in the measured voltages ( $v_s$ ), the compensation results will be associated with the utility voltage's condition. It means that, if voltage waveforms were not perfectly sinusoidal, the currents distortion could not be minimized, even using the proposed repetitive control. However, in such conditions it is still possible to use an adaptative band-pass filter ( $F_1$ ) or even the PLL to select just the voltage's fundamental component and ensure the ideal harmonic compensation reference.

The results of this former case will be quite similar to the *sinusoidal source current synthesis* discussed in [18], but in this case using all the advantages of the selective harmonic compensation method.

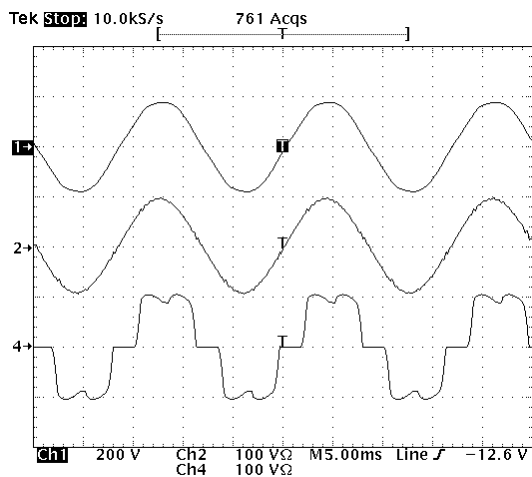


Fig. 12 – Line voltage  $v_s$  (200V/div), line current  $i_s$  (10A/div) and load current  $i_L$  (10A/div) using the selective control (Case 2).

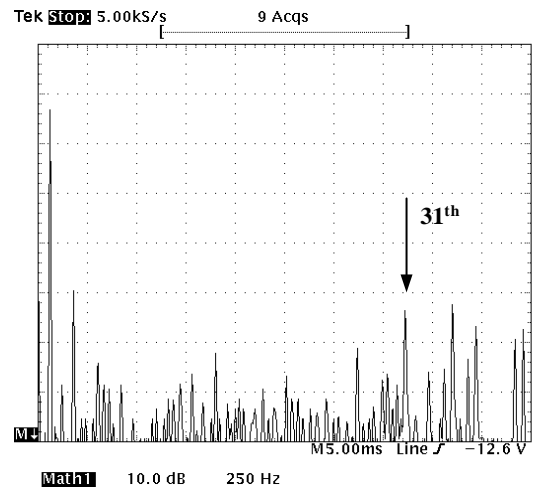


Fig. 13 - Spectrum of the source currents (10dB/div - 250Hz/div), using selective control (Case 2).

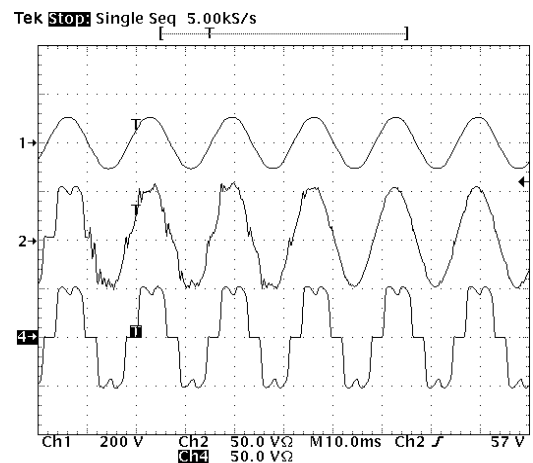


Fig. 14 – Line voltage  $v_s$  (200V/div), line current  $i_s$  (5A/div) and load current  $i_L$  (5A/div) during active filter initialization (10ms).

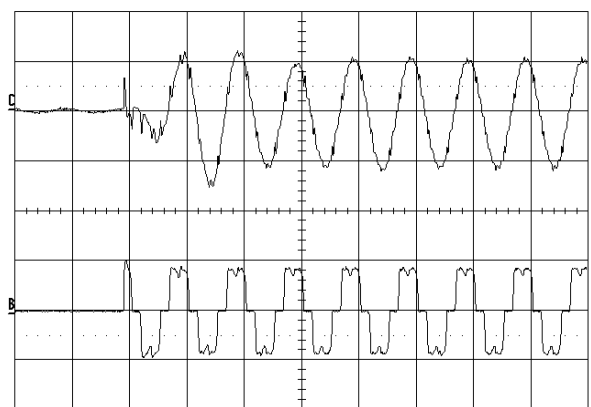


Fig. 15 – Load turn-on using the proposed solution: line current  $i_s$  (10A/div) and load current  $i_L$  (10A/div).

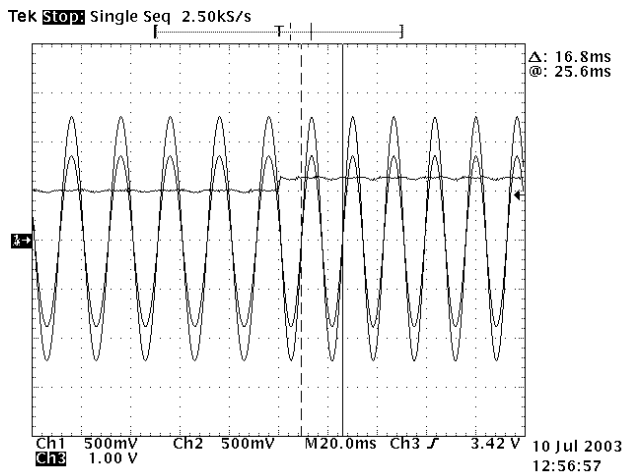


Fig. 16 – PLL response during a frequency step from 50 to 60Hz.

#### IV. CONCLUSIONS

This paper proposes a selective harmonic compensation method using a closed-loop repetitive controller. The selective compensation reference has been provided using a modified DCT-based filter and a digital PLL tracking system. Such approach allows full compensation of selected frequencies, even if the active filter has limited bandwidth.

Compared to synchronous frame harmonic regulators, recently proposed for active power filters, this method requires a simpler algorithm, whose complexity is independent on the number of compensated harmonics. Furthermore, the proposed algorithm is less sensitive to rounding and quantization errors and it suits very well fixed point DSP implementation.

Experimental results on a 5.5kVA prototype confirm the theoretical expectations.

#### ACKNOWLEDGEMENT

Support for this research comes from FAPESP (99/11882-5), CAPES (BEX2165/01-5) and Analog Devices.

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