PROPOSAL OF A TIMER CONTROLLER WITH CONSTANT SWITCHING FREQUENCY AND POWER FACTOR CORRECTION

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Abstract – **The proposal of this paper is to introduce a new control technique for power factor correction in ac-dc converters. It combines the advantages of conventional hysteresis control strategy and the prominent characteristics of constant switching frequency. The fundamental idea consists of determining the ideal time interval that exists between the moment when the input current crosses with the reference current and the converter commutation. Thus the input current can oscillate simetrically around the reference current with constant frequency of operation. The operating principles, theoretical analysis and simulation results on a single-phase Boost converter are presented to validate the proposal.**

Keywords - **constant switching frequency, low harmonic distortion, power factor correction.**

I. INTRODUCTION

One notices when one looks at Electrical Engineering applications, the growing number of nonlinear loads such as diode or thyristor rectifiers, switch-mode power supplies and adjustable speed drives, generate harmonic currents causing various problems to other equipment connected to the point of common coupling. Typical problems are overheated machines, transformers and power cables, current flow in the neutral conductor, flicker effects, and malfunctioning of sensitive devices. The reduction of the harmonic contents and also the high power factor are desirable aspects in ac-dc converters, as they have the potential for reducing harmonic sources which is a good operational characteristic from the point of view of power quality [1].

For such aspects, several standards have been proposed to normalize and limit harmonic pollution, such as IEEE Std 519 and IEC 61000-3-2. Throughout the years, switching techniques have been introduced to static converters in order to minimize such disturbances, with two strategies becoming popular i.e. PWM and hysteresis modulation. The hysteresis control introduces a minor error in the average input current and provides better dynamic response than the PWM control, but an inherent drawback is the variable switching frequency. Therefore the control circuit has to be designed for a large band, otherwise it will cause low frequency harmonics [2].

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In light of this limitation, this paper introduces a novel control technique that allows ac-dc converters to operate with constant switching frequency, except when the reference current crosses with zero reference, and with the advantages of a common hysteresis control strategy, the THD and harmonic content are less than other techniques that operate with constant switching frequency.

II. TIME CONTROLLER WITH POWER FACTOR CORRECTION

The basic idea of the proposed technique is to determine the ideal time interval between the switch commutation and the moment when the input current, IL, crosses the reference current, Iref. With these intervals, it is possible to build a timer circuit to control the commutation of switches with constant frequency, so that the triangles **abc** and **cde** have the same area and the medium value of IL, Fig. 1, will be Iref. Fig. 1 shows the behavior of the input current along an incremental time interval, where the reference current is practically constant, which is possible since the switching frequency is much greater than the line frequency.

This type of strategy can be applied to most single-phase ac-dc converters, without any essential change to the original topology [3]. For this study, a conventional hard-switched Boost converter operating in continuous conduction mode is chosen due to simplicity, as it has only two operating stages.

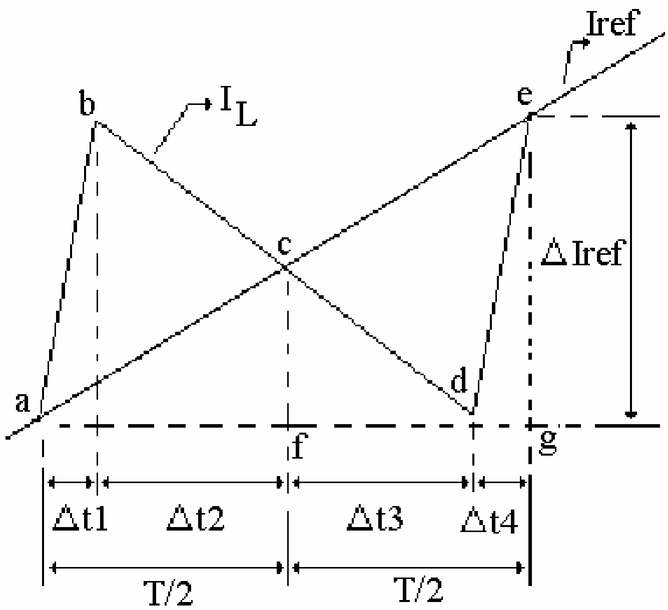


Fig. 1. Current profile along a switching period.

III. MATHEMATICAL ANALYSIS

In order to analyze the proposed control strategy, the circuit shown in Fig. 2 must be considered, where it can be seen that the full bridge converter operation can be defined in two distinct stages. Voltage V_x in the first and second stages is defined as V_{x1} and V_{x2}, respectively. Such values depend on the type of the converter in question. For the full-bridge topology, voltages V_{x1} and V_{x2} will be respectively V_o and $-V_o$. For the boost converter, voltages V_{x1} and V_{x2} will be V_o and null, respectively. However, independent of the topology, voltage V_{x1} will always be greater than the input voltage, and voltage V_{x2} is less than the input voltage or null. Additionally, if the switching frequency is considered much greater than the line frequency, the behavior of the inductor current can be described according to Fig. 1, which corresponds to an ideal situation i.e. triangles ABC and CDE have the same area. To obtain this, it is necessary to determine time intervals Δt_1 and Δt_3, which correspond to the exact moments when the switch is commutated. Intervals Δt_1 and Δt_3 are determined as a function of the circuit parameters, in order to maintain constant switching frequency.

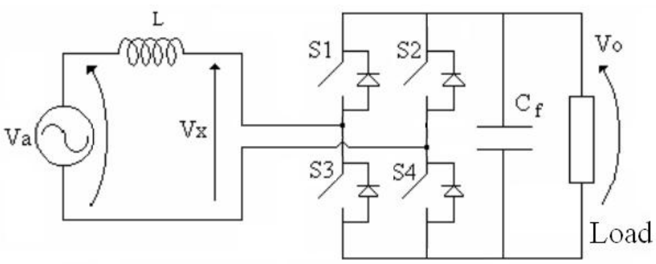


Fig. 2. Full Bridge converter with two operating stages.

Expressions (1) and (2) represent the increasing and decreasing rates of the input current, respectively.

$$I_L = \frac{\int (-V_{X2} + V_a)dt}{L} \tag{1}$$

$$I_L = \frac{\int (-V_{X1} + V_a)dt}{L} \tag{2}$$

Within these aspects, the output voltage is constant and the reference current variation is considered linear. In addition to this, the increasing and decreasing rates of the inductor current can be considered constant. Therefore triangles ABC and CDE have the same area and the following expressions are valid:

$$\Delta t_2 \cong \Delta t_3 \tag{3}$$

$$\Delta t_1 \cong \Delta t_4 \tag{4}$$

Where:

Δt_1 – represents the time interval where the current derivative is positive, from the crossing point with the reference current to the instant of commutation;

Δt_2 – represents the corresponding time interval where the current derivative is negative from the instant of commutation to the crossing point with the reference current;

Δt_3 – represents the corresponding time interval where the current derivative is negative from the crossing point with the reference current to the instant of commutation;

Δt_4 – represents the corresponding time interval where the current derivative is positive from the instant of commutation to the crossing point with the reference current.

Intervals Δt_1 and Δt_3 determine the moment to commutate the switches. Time interval Δt_1 can be calculated from (5) and (6).

$$\Delta t_1 + \Delta t_2 = T/2 \tag{5}$$

Considering, in fig. 1, that triangle AFC is similar to triangle AGE, the inductor current variation in a T/2 time interval is

$$\int_{t}^{t+\Delta t_1} \frac{(-V_{X2} + V_a)dt}{L} + \int_{t+\Delta t_1}^{t+T/2} \frac{(-V_{X1} + V_a)dt}{L} = \frac{\Delta I_{ref}}{2} \tag{6}$$

Where:

ΔI_{ref} is the reference current variation in a switching period;

T is the switching period.

Assuming that current I_{ref} is linear along the switching period, ΔI_{ref} can be calculated as:

$$\Delta I_{ref} = T\frac{dI_{ref}}{dt} \tag{7}$$

Finally, from the previous expressions, the generic equation to interval Δ_{t1} is given as:

$$\Delta_{T1} = \frac{T}{2(V_{X1} - V_{X2})}\left(V_{X1} - \frac{2}{T}\int_{t}^{t+T/2} V_a dt + \frac{L\Delta I_{ref}}{T}\right) \tag{8}$$

The same procedure can be used to calculate Δt_3. The Full Bridge converter equation (8) can be simplified as follows:

$$\Delta t_1 = \frac{T}{4V_0}\left(V_0 - V_a + L\frac{dI_{ref}}{dt}\right) \tag{9}$$

Analogously, Δt_3 can be obtained from (10).

$$\Delta t_3 = \frac{T}{4V_0}\left(V_0 + V_a - L\frac{dI_{ref}}{dt}\right) \tag{10}$$

From time intervals Δt_1 and Δt_3, it is possible to develop a circuit that allows one switch to be controlled (or more switches, in some topologies) with constant frequency, emulating hysteresis band. Therefore the behavior of the input current is represented in Fig. 3, where time intervals Δt_1 and Δt_3, maintain the input current between two reference waveforms. Analogously to the hysteresis control, these two reference currents can be calculated from equations (11) and (12), respectively.

$$I_{ref(\text{up})} = \frac{1}{L}\int_0^{\Delta_{T1}} \left(V_0 + V_a - L\frac{dI_{ref}}{dt} \right) dt + I_{ref} \quad (11)$$

$$I_{ref(low)} = \frac{1}{L}\int_0^{\Delta_{T3}} \left(-V_0 + V_a - L\frac{dI_{ref}}{dt} \right) dt + I_{ref} \quad (12)$$

The reference current is the same parameter in expressions (11) and (12), which can be simplified and adequately represented as (13) and (14), respectively.

$$I_{ref(\text{up})} = \frac{1}{L}\left(V_0 + V_a - L\frac{dI_{ref}}{dt} \right)\Delta_{T1} + I_{ref} \quad (13)$$

$$I_{ref(low)} = \frac{1}{L}\left(-V_0 + V_a - L\frac{dI_{ref}}{dt} \right)\Delta_{T3} + I_{ref} \quad (14)$$

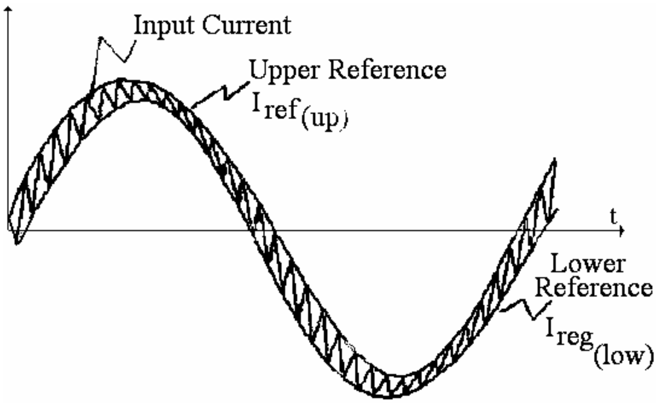


Fig.3. Input current behavior.

IV. BOOST CONVERTER

The single-phase boost converter shown in Fig. 4 has just two operating stages. When S_1 switch is off, the voltage across the filter inductor is (V_a-V_o), otherwise it is V_a. The simplified control circuit used in a Boost converter is shown in fig. 4 too.

For this converter, the expressions corresponding to time intervals Δt_1 and Δt_3 i.e. (9) and (10) can be written as:

$$\Delta_{T1} = \frac{T}{2V_0}\left(V_0 - \frac{2}{T}\int_t^{t+T/2} |V_a| dt + \frac{LdI_{ref}}{T} \right) \quad (15)$$

$$\Delta_{T3} = \frac{T}{2V_0}\left(\frac{2}{T}\int_t^{t+T/2} |V_a| dt - \frac{LdI_{ref}}{T} \right) \quad (16)$$

Both equations can be approximated to expressions 17 and 18, respectively:

$$\Delta_{T1} = \frac{T}{2V_0}\left(V_0 - |V_a| + \frac{LdI_{ref}}{T} \right) \quad (17)$$

$$\Delta_{T3} = \frac{T}{2V_0}\left(|V_a| - \frac{LdI_{ref}}{T} \right) \quad (18)$$

Time intervals Δt_2 and Δt_4 can be calculated analogously, but they are not necessary in the control development, because they are not directly involved in the process itself.

Figure 5 shows the main control block. The operation of this circuit is quite simple. The objeticve is to impose an ideal situation i.e. triangles ABC and CDE must have the same area, so the IL current will oscilate simetrically around the reference current Iref. With this, it will be possible to obtain small THD and harmonic content in the imposed current. First, it is necessary to create the reference current signal Iref. In fig. 4 it can be seen that Iref is a function of Va that provides the sinusoidal waveform to Iref, as well as a function of the output voltage error, to enable the control to regulate the output voltage. The block X is a multiplier. The process to obtain Iref is similar to the process used in Unitrode IC 3854.

Also, It is necessary to create two voltage signals, $V_{\Delta t1}$ and $V_{\Delta t3}$, fig. 4. These signals are proportional to rectfied input voltage Va, to output voltage Vo, and to the differential Iref current. Adding these three signals, in a way shown in fig. 4, $V\Delta t_1$ and $V\Delta t_3$ signals are obtained. The parameter K2 is proportional to inductor L and constant K1, and the K1 value is chosen to keep voltages $V_{\Delta t1}$ e $V_{\Delta t3}$ within the voltage band used for the circuit control. Therefore parameter K1 can be defined as:

$$K_1 \approx \frac{T}{2V_o L} \quad (19)$$

Considering the "**a**" point in fig. 1, when the inductor current IL crosses with the reference current Iref in ascendant direction, at this moment, switch S1 is on, and the output comparator 1 turns to high level, "1", so the AND gate 1 turns to "1" too. The AND gates 2 and 4 remain at low level, and the comparator 3 is off, as shown in fig. 6.

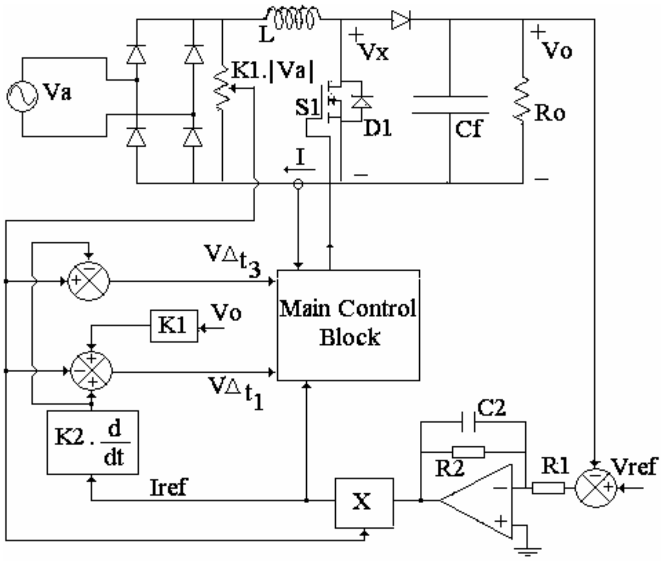


Fig. 4. Simplified block diagram using timer control applied to a boost converter.

The high level in AND gate 1 sets the OR gate to level "1", enabling the ramp generator. The ramp generator creates a voltage ramp with inclination ($2V_o/T$), until this voltage reaches $V_{\Delta t1}$. When Vramp > $V_{\Delta t1}$, the outputs of comparator

2 and AND Gate 3 turn to "1". The $\overline{Q}$ output "flip-flop" turns to "0", turning off the S1 switch. This finishes the Δt1 time interval, as shown in fig. 6, where PS1 is the S1 gate pulse.

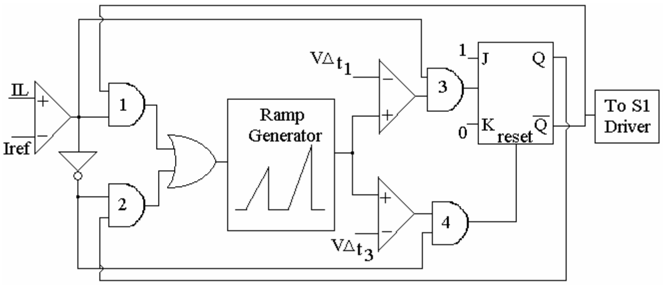


Fig 5. Block diagram of the main control circuit.

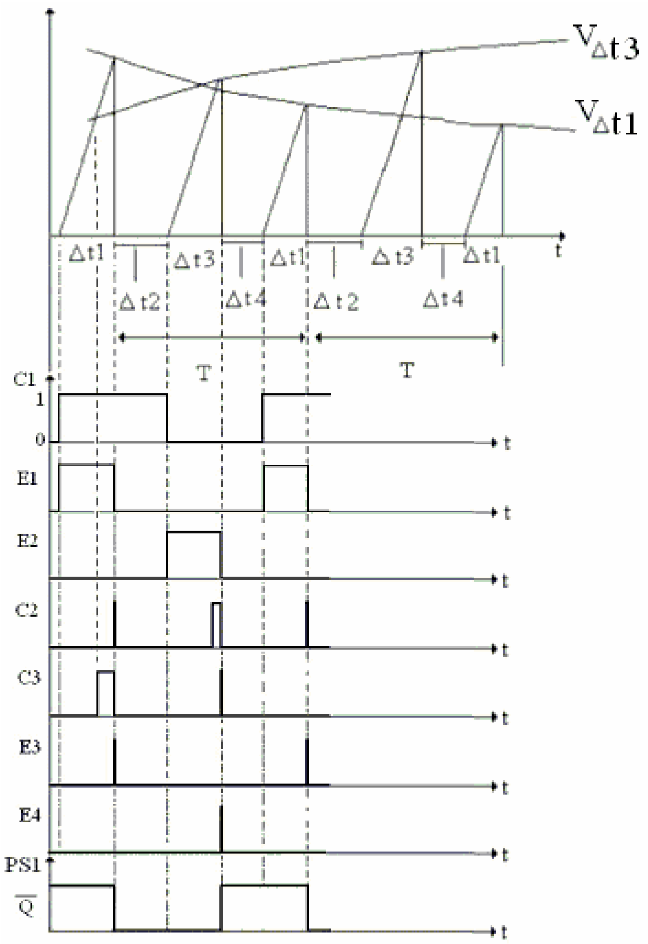


Fig 6. VΔt_1 and VΔt_3 waveforms and logic signal control.

Following this, $\overline{Q}$ = 0 leads the output of the AND gate 1 to "0", resetting the OR gate, and turning off the ramp generator. With Switch S1 off, the inductor current decreases until it crosses again with the reference current, in "C" point, fig. 1. So time interval Δt2 finishes and Δt3 time interval begins. Comparator 1 goes to "0". This transition disables AND gates 1 and 3, disabling comparator 2. The AND gate 2 goes to "1", enabling AND gate 4 to follow the comparator 3 state logic.

With IL < Iref, the OR gate output goes to "1" again, enabiling the ramp genetor. When the voltage ramp reaches $V_{\Delta t3}$, Vramp > $V_{\Delta t3}$, the outputs of comparator 3 and AND Gate 4 turn to "1" and the $\overline{Q}$ output "flip-flop" turns to "1", enabling the S1 switch and thus turning off the ramp generator. This finishes the Δt3 time interval and begins Δt4. After this moment, the inductor current increases until it crosses with the reference current, finishing Δt4 time interval and beginning a new switching cycle.

The ramp generator circuit is shown in fig. 7.

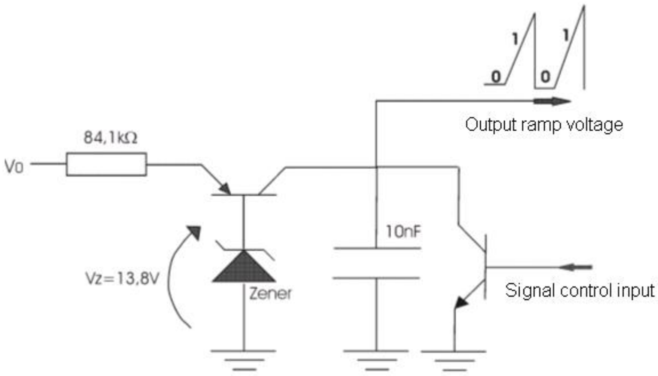


Fig 7. Ramp generator circuit.

This circuit determines the switching frequency. The VΔt_1 and VΔt_3 voltages values determine the voltage ripple in the capacitor. The switching frequency can be calculated in eq. 20.

$$f_s = \frac{I_c}{2 \times C \times \Delta V_c} \tag{20}$$

V. SIMULATION RESULTS

Simulation tests were performed on a Boost converter to demonstrate the control strategy. Conventional hysteresis control was also implemented to establish an eventual comparison between both techniques. One must mention that in both cases the average switching frequency is basically the same. The parameters employed in the tests are specified in Table I.

Table I
Parameters set used in simulation tests

Parameter	Value
Input voltage	V_i=127Vrms
Output voltage	V_0=250Vdc
Filter inductor	L_f=1.73mH
Filter capacitor	C_f=1000μF
Load current	I_o=5.5A
Switching frequency	f_s=20kHz
Switch S_1	IRFP460
Diodes	MUR1560

Fig. 8 shows the input current waveform.

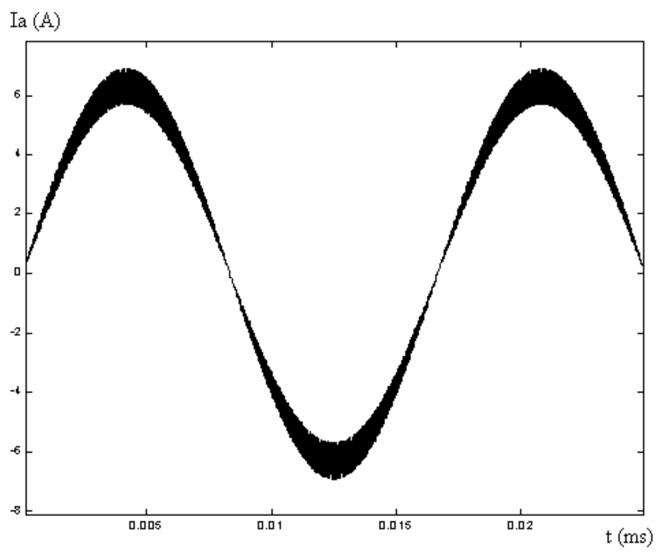
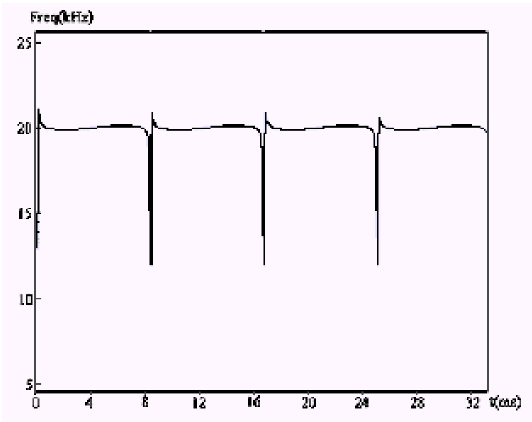
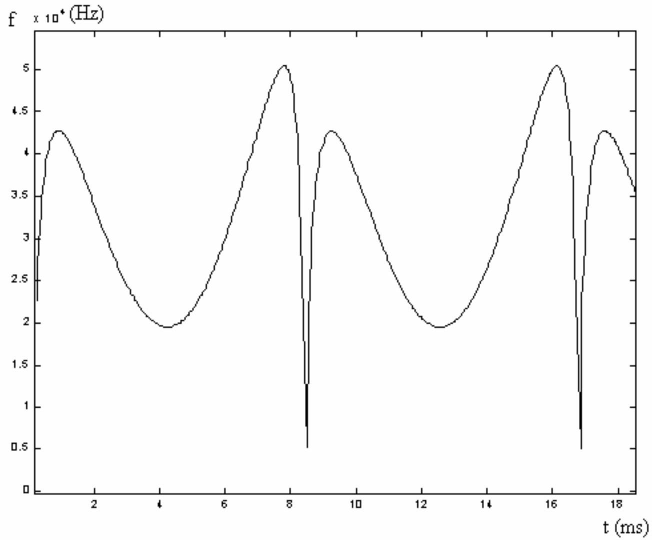


Fig 8. Input current waveform.



(a) Proposed Timer technique.



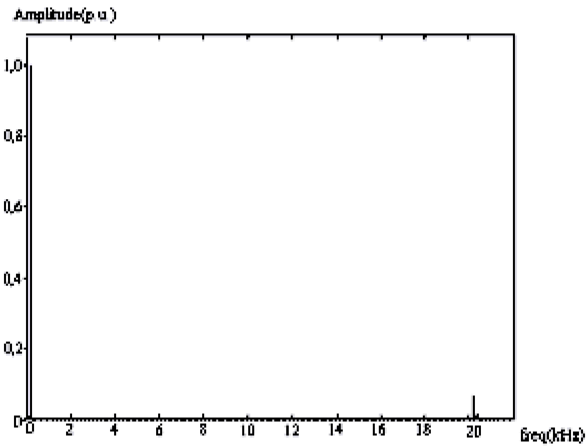
(b) Conventional hysteresis technique.

Fig. 9. Switching frequency oscillation.

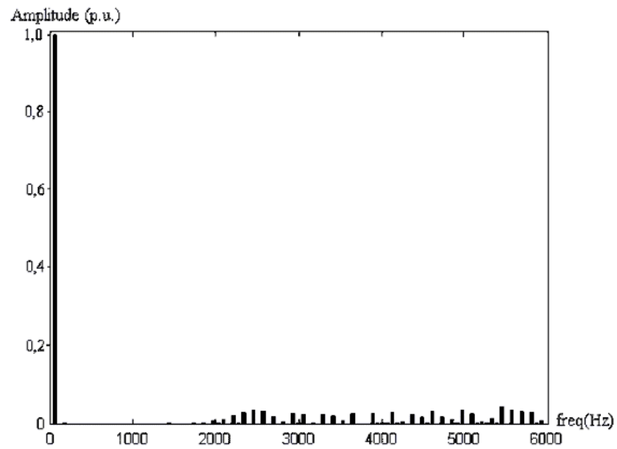
Fig. 9 (a) and (b) compare the switching frequency oscillation in a Boost converter operating with the proposed technique and the conventional hysteresis strategy, respectively. In fig. 9 (a) the inductor current growth depends on the input voltage. When this voltage crosses with zero, and a new growth stage of the reference current begins, the inductor current di/dt is less than the reference current di/dt, so the switch S1 must be on until IL reaches Iref. In this case, the switching frequency will decrease. It can be seen that the frequency variation in the conventional histeresis is greater than the proposed technique, fig. 9 (b). This large frequency variation makes it more difficult to filter the harmonic content, and the filter in this case is heavier and voluminous.

Fig. 10 (a) and (b) compare the input current harmonics amplitudes in the frequency domain with both control techniques. It can be seen that in 10 (a) the harmonic content is centered at 20kHz and can be easily filtered.

In fig. 10 (b) the harmonics are distributed in a range of 2kHz to 6kHz. So, in this case, it is more difficult to filter the harmonic content, and a low pass filter must be used with a corner frequency of 600Hz.



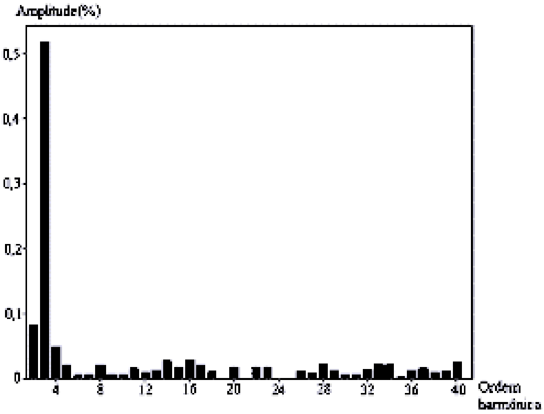
(a) Proposed Timer technique.



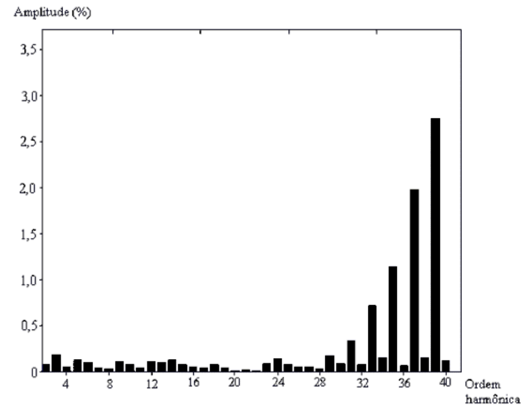
(b) Conventional hysteresis technique.

Fig. 10. Harmonic amplitudes in the frequency domain.

Fig. 11 (a) and (b) compare the harmonic content as a function of the harmonic order. In fig 11 (a) it can be seen that there exists a third harmonic, 180Hz, with an amplitude of 0.5% of the fundamental amplitude. The THD in fig. 11 (a) is 0.55%. In fig. 11 (b) the low frequency harmonics have low amplitudes, however the harmonic amplitudes increase rapidly a from the 22nd harmonic. The THD in fig. 11. (b) is 3.7%.



(a) Proposed Timer technique.



(b) Conventional hysteresis technique.

Fig. 11 Harmonic amplitude as a function of the harmonic order.

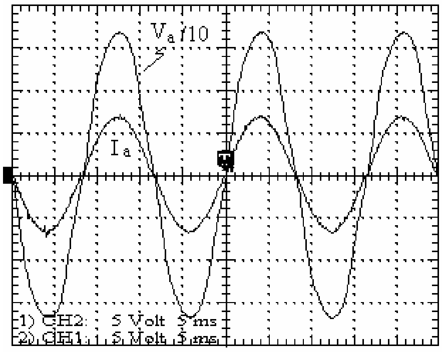
VI. EXPERIMENTAL RESULTS

A Boost converter was experimentally developed and evaluated. The parameters employed in these tests are specified in Table II.

Table II
Parameters set used in simulation tests

Parameter	Value
Input voltage	V_i=127Vrms
Output voltage	V_0=250Vdc
Filter inductor	L_f=1.73mH
Filter capacitor	C_f=1000µF
Load current	I_o=5.5A
Switching frequency	f_s=20kHz
Switch S_1	IRFP460
Diodes	MUR1560

Fig. 12 proves the existence of a power factor correction. One obeserves a quasi-sinusoidal waveform to the AC input current for an input power of 600W.



va(t): 5V/div; ia(t): 5A/div; Time: 5ms/div.

Fig. 12. Input voltage and input current waveforms.

Figs. 13 and 14 show the harmonic contents of the input voltage and input current, where voltage THD is 3.4% and current THD is 1.9%.

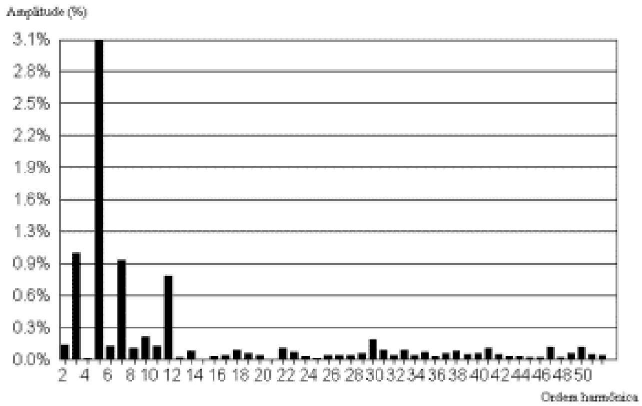


Fig. 13. Harmonic content of the input voltage.

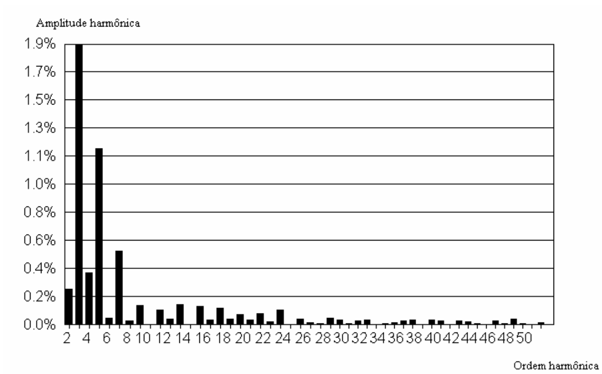
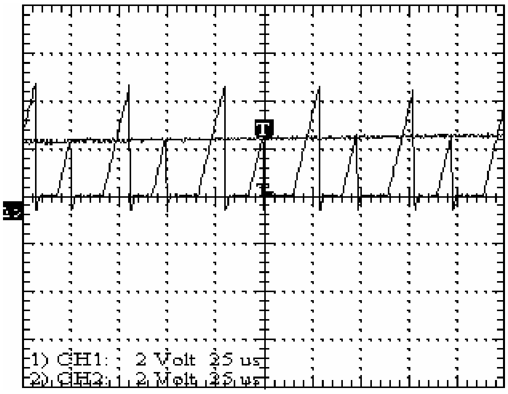


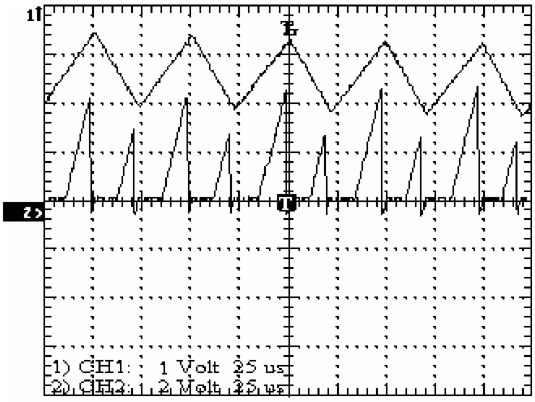
Fig. 14. Harmonic content of the input current.

Figs. 15 and 16 show details of output voltage and ramp voltage, and filter inductor current and ramp voltage, respectively. Fig. 16 shows clearly that the IL current increases linearly when $\Delta t3$ time interval finishes, and decreases linearly when $\Delta t1$ finishes.



Ch1: 200V/div; Ch2: 2V/div; Time: 25μ/div.

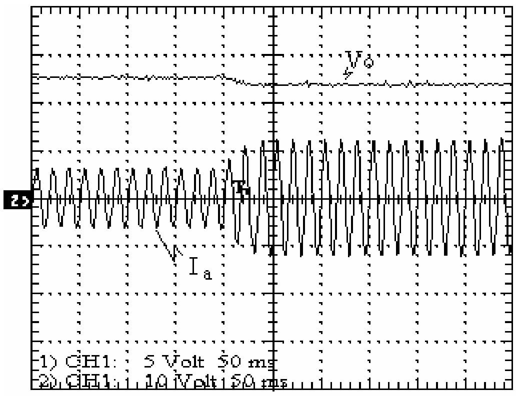
Fig. 15. Output voltage and ramp voltage.



Ch1: 2A/div; Ch2: 2V/div; Time: 25μ/div.

Fig. 16. Filter inductor current and ramp voltage.

Fig. 17 shows the converter dynamic response to a 500W to 1kW step load variation. In this figure the output voltage, Vo, and the input current Ia are shown.



Ch1: 100V/div; Ch2: 10A/div; Time: 50ms/div.

Fig. 17. Converter Dynamic response.

VII. CONCLUSION

This paper has presented a novel control technique that has the advantages of conventional hysteresis control and also constant switching frequency. The proposed control consists of a combination of the hysteresis control and PWM control, where constant switching frequency is obtained when a timer circuit is employed.

As can be seen from the experimental results, the switching frequency variation is small as expected according to the mathematical study. It is also possible to say that the frequency variation relative error decreases with the increase in switching frequency. As a result this effect could be negligible.

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BIOGRAPHIES

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