A NOVEL HIGH-POWER-FACTOR SINGLE-SWITCH ELECTRONIC BALLAST FOR COMPACT FLUORESCENT LAMPS

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***Abstract* – In this paper a high-power-factor electronic ballast for compact fluorescent lamps based on the class E amplifier and featuring low voltage stress across the switch is presented. The proposed ballast is obtained by integrating a buck-boost converter, used as power factor correction stage, and a class E amplifier with a parallel resonant tank, used as resonant inverter. The buck-boost converter is op-erated at constant frequency and constant duty cycle in discontinuous conduction mode (DCM) to obtain a high input power factor.**

***Keywords* - Buck-boost, class E amplifier, electronic ballast, high power factor, single stage.**

I. INTRODUCTION

Compact fluorescent lamps are becoming a very popular light source, since they are used mainly in home applications instead of incandescent lamps. The reason is that they present several advantages as higher luminous efficacy and longer life. Moreover, when compact fluorescent lamps are supplied using electronic ballast the resulting source of light is small, light and efficient.

However, the main disadvantage of compact fluorescent lamps is their high cost, especially when electronic ballast are incorporated to supply the lamp and the requirements of harmonic standards such as IEC-1000-3-2 must be fulfilled [1]. The higher initial cost is compensated by a higher efficiency and longer life in the long term, but it still makes difficult the marketing of electronic compact fluorescent lamps. This is why nowadays there exists a trend to reduce the cost of electronic ballast as much as possible, in order to make them competitive against the traditional electromagnetic ballasts.

One of the possibilities to decrease the cost is by reducing the number of electronic components used in the ballast, what can be achieved by the integration of several stages in only one.

Figure 1a shows a block diagram of a traditional electronic ballast for compact fluorescent lamps. As can be seen, a traditional electronic ballast consists of two stages. The first one is an active power factor correction stage supplied by the full bridge diode rectifier. This stage is used to correct the input power factor, so that the ballast is seen by the line as a resistive load; also, it generates a regulated DC output voltage which supplies the second stage. The second stage is the high frequency resonant inverter used to ignite the lamp and to stabilize the lamp current during normal running. The resonant inverter should supply the lamp with an alternating symmetric current to assure a uniform wear of both lamp electrodes.

The number of components used in the electronic ballast of Fig. 1a can be reduced by integrating the two stages in a single one, as shown in Fig. 1b. This single stage is used to both correct the input power factor and drive the fluorescent lamp. This integration technique has been studied in depth [2-6] with noticeable good results. Normally, a class D amplifier or half bridge inverter is used to implement the resonant inverter. Class D inverters are used to generate an square waveform, which once filtered is used to supply the lamp with a sinusoidal waveform. Both class D amplifier and half bridge inverter use two transistors in order to produce the square output waveform; one of them is not ground referenced, making necessary the use of an especial driver and increasing cost.

With the aim of reducing the ballast component count, several integrated topologies using a class E amplifier instead of a class D amplifier have been proposed [7-8]. Class E amplifier presents several advantages when compared to the class D one, as only one power switch, zero voltage switching, high efficiency and high frequency operation. However, the main disadvantage is the high voltage stress across the switch, which can be as high as four times the supply voltage.

In this paper a high-power-factor electronic ballast for compact fluorescent lamps based on the class E amplifier and featuring low voltage stress across the switch is presented.

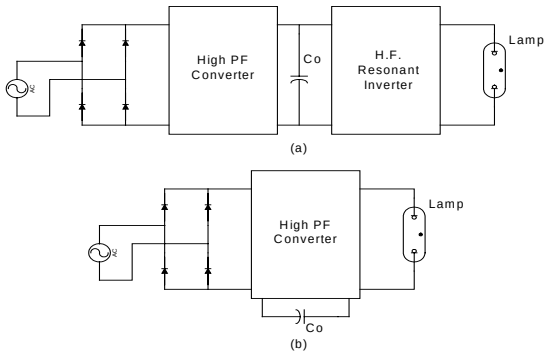

Fig. 1. Typical Electronic Ballast with high power factor. (a) Two stage ballast, (b) single stage ballast

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The proposed ballast is obtained by integrating a buck-boost converter, used as power factor correction stage, and a class E amplifier with a parallel resonant tank, used as resonant inverter [9-10]. The buck-boost converter is operated at constant frequency and constant duty cycle in discontinuous conduction mode (DCM) to obtain a high input power factor.

The switch voltage stress is reduced by operating with a duty cycle lower that 50%, thus the buck-boost converter works in buck mode and reduces the voltage across the switch. However, the use of a duty cycle lower than 50% in the class E amplifier produces asymmetric high-crest-factor current waveforms through the lamp. In the proposed ballast, this problem was overcome by using a transformer instead of the resonant inductor and supplying the lamp from the secondary of the transformer through a series inductor.

The resulting ballast is an integrated topology with active power factor correction, which supplies the lamp with a symmetric low-crest-factor current waveform. The power switch used is a MOSFET with a series diode. The entire switch presents zero voltage switching, but the MOSFET exhibits hard switching due the integration of the class E amplifier with the buck-boost converter. The main disadvantage of the proposed topology is the high current stress in the power switch.

Following the analysis, design and experimental results of the proposed topology are presented. Section II presents the topology derivation and analysis. In section III the design methodology is explained based on a design example. Section IV presents the experimental results obtained from a prototype for a 32W compact fluorescent lamp. Finally, section V gives some conclusions summarizing the possibilities of the proposed topology.

II. DERIVATION AND ANALYSIS OF THE PROPOSED ELECTRONIC BALLAST

A. Derivation of the proposed electronic ballast

The proposed electronic ballast comes from the integration of a buck-boost converter and a class E amplifier with only one inductor and one capacitor in the load network. This resonant inverter was selected based on the good characteristics of this topology: uses only one transistor and a parallel RLC resonant tank and the single switch is ground referenced. Therefore, an especial drive is not necessary. Furthermore, the switch turn-on and turn-off transitions are performed at zero voltage. This type of class E amplifier was presented in [9] and analyzed in [10]. As presented in [9] the class E amplifier with only one inductor and one capacitor in the load network can be implemented in several ways, as shown in Fig. 2. Topology shown in Fig. 2a is equivalent to that shown in Fig. 2b, since in an AC analysis the DC voltage source VCD behaves as a short circuit. Topology shown in Fig. 2c is similar to that in Fig. 2b but using a transformer instead of an inductor. A topology similar to that shown in Fig. 2c was used to supply high intensity discharge (HID) lamps in [11]. In [11] the topology shown in Fig. 2c is analyzed considering the effect of the transformer leakage inductance, but the relationship between the transistor duty cycle and load voltage and current was not clearly established. Besides, according to [10], this topology presents an asymmetric load current waveform with high crest factor. The presence of leakage inductance slightly improves the lamp current crest factor (CCF). However, the use of the leakage inductance is not very reliable to improve the lamp CCF. The solution comes from incorporating an additional inductor in series with the load, which integrates the leakage inductance effect and improves the CCF.

The topology proposed to drive the lamp is shown in Fig. 3a. This topology is very similar to that presented in [11], only an extra inductor is placed in series with the lamp in order to improve the lamp CCF. The circuit shown in Fig. 3a is equivalent to the class E amplifier with only one inductor and one capacitor in the load network presented in [9] and [10]. Figures 3b, 3c and 3d illustrate the simplification process used to obtain the equivalent circuit. The first step is shown in Fig. 3b, where the series circuit L_S-R_L is substituted by a parallel circuit L_{sep}-R_{Lep}. In Fig. 3c this parallel circuit is converted to the transformer primary side. Finally, the resulting circuit is simplified in Fig. 3d to give a class E amplifier with only one inductor and one capacitor in the load network.

In order to reduce the lamp current crest factor the resonant inverter should be operated with a duty cycle lower than 50%. According to [10], this condition also allows to reduce the voltage stress in the switch.

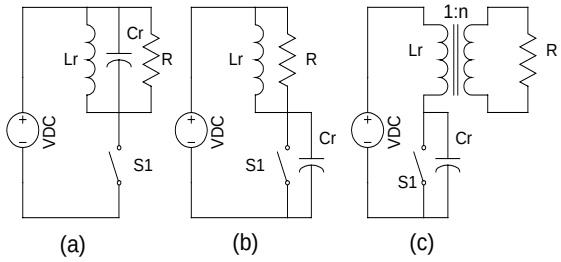

Fig. 2. (a) Class E amplifier with only one inductor and one capacitor in load network; circuits (b) and (c) are electrically equivalent to (a) because the ac voltage in VDC is zero.

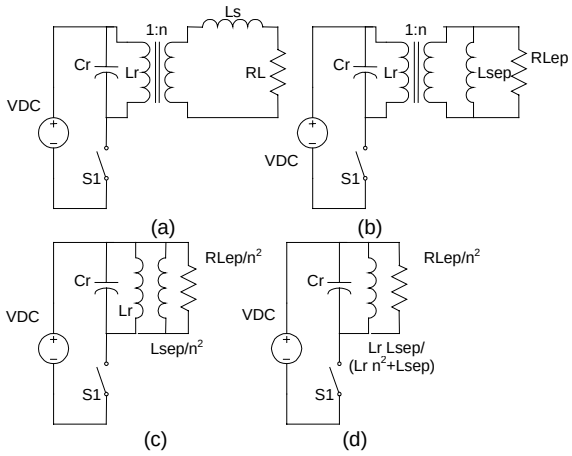

Fig. 3. (a) Proposed inverter to drive the lamp , (b), (c) and (d) show the simplification of the proposed inverter to a class E amplifier with only one inductor and capacitor in load network

The proposed ballast integrates the power factor correction stage and the resonant inverter by sharing the only switch existing in each topology. This gives several restrictions that should be taken into account in order to select the correct topology for the power factor correction stage. Thus, the selection was made based on the following conditions: duty cycle lower than 50 %, low voltage stress in the switch and high input power factor.

Based on previous conditions the selected topology is the buck-boost converter. This converter provides a high input power factor and when operated with duty cycle lower than 50% the output voltage is lower than the input voltage, thus reducing the voltage stress in the switch.

The integration of the buck-boost converter and the proposed inverter is illustrated in Fig. 4. Figure 4a shows the two stage configuration and Fig. 4b shows how the two stages can be integrated in a single one by sharing the power switch. The integration is performed taking into account that both switches M1 and M2 in Fig. 4a are connected to ground and can be operated synchronously. A diode in series with the switch is added to avoid current circulating from the rectified AC voltage to the filter capacitor C_f, through the circuit Lr-Cr. The use of diode D3 shown in Fig. 4b provides half wave ZVS in the switch M1-D2. If diode D3 is removed the commutations in the switch will be ZVS with full wave, so the use of this diode is optional.

In order to achieve low voltage stress in the switch and improve the lamp CCF, the proposed ballast should operate with $D=t_{on}/T<0.5$. As stated in [1], in a class E amplifier with only one inductor and one capacitor in load network, the voltage stress in the switch is proportional to the duty cycle and the distortion of the load waveforms is lower for the higher duty cycles. On the other hand, for duty cycles lower than 0.5 the buck-boost converter behaves as a step-down converter and therefore the DC input voltage of the class E amplifier is lower than line voltage. In this way, the proposed circuit can be supplied from American or European line voltages providing admissible voltage stress in the switch.

B. Analysis of the proposed ballast.

Figure 5 shows the equivalent circuits for the different operation intervals of the proposed ballast and Fig. 6 shows the operating waveforms of the proposed converter for a duty cycle of 20%. In figure 6 Vg is the voltage across M1 gate, V_{DD} is the voltage across D2-M1, V_D is the M1 drain voltage, V_L is the lamp voltage, i_{Lr} is the current through Lr, i_{Cr} is the current through Cr, i_{D2} is the current through D2 and i_{Lf} is the current through the buck-boost inductor Lf.

The operating of the circuit within a switching period is the following:

0<t<t1. M1 gate voltage is high. M1 is on and voltage across M1-D2 is equal to zero (Fig. 5a). Then vCr(t)=vCf(t) and iCr(t)=0. The current through inductor Lr increases linearly with VCf and Lf current does the same with rectified line voltage. During this time interval current through M1 is given by the addition of Lr and Lf currents. Current through diode D2 is equal to Lr current.

t1<t<t2. M1 gate voltage goes low and M1 opens (Fig. 5b). Cr and Lr resonate and icr(t)=iLr(t). Voltage across M1-D2 starts from zero and is equal to $v_{Cr}(t)+v_{Cf}(t)$. M1 exhibits a hard switching and its voltage is equal to the addition of the line rectified voltage and the voltage across Lf ($v_{cf}(t)$). Since the buck-boost converter operates in DCM, all the energy stored in Lf has been transferred to capacitor Cf at the end of this time interval $i_{Lf}(t2)=0$.

t2<t<T. Inductance Lf is reset and $v_{Lf}(t)=0$. Therefore, voltage across M1 is equal to the rectified line voltage. Voltage capacitor Cr decreases until equaling $v_{Cf}(t)$, and thus voltage across M1-D2 equals zero (Fig. 5c).

As can be seen in Fig. 6, all the time the class E amplifier is supplied with a nearly constant voltage and consequently there is no low frequency modulation of the lamp current. Besides, lamp voltage and current are symmetric waveforms. Therefore, a low lamp CCF is attained.

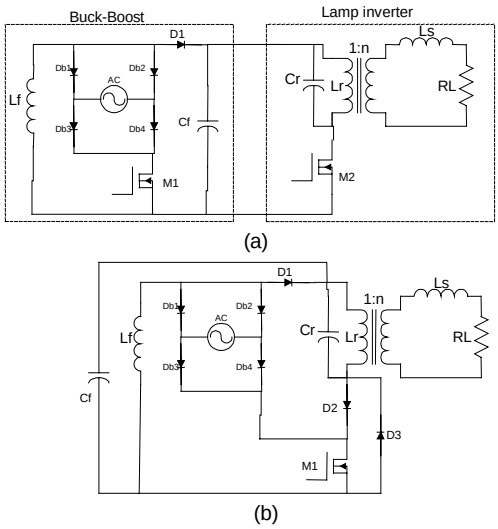

Fig. 4. Integration of the proposed ballast. (a) Two stage configuration, (b) Proposed integrated ballast.

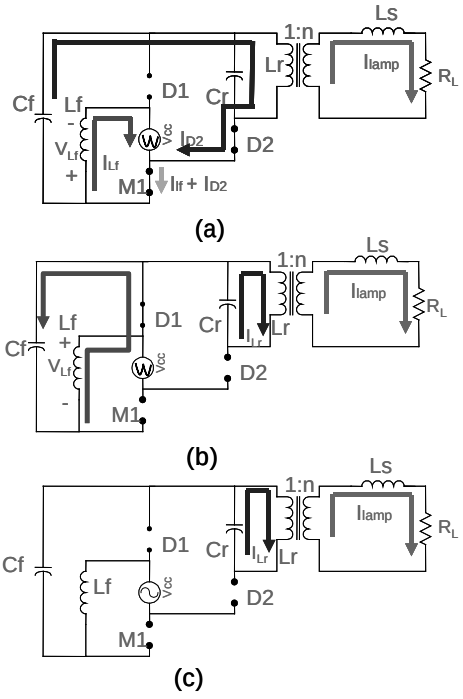

Fig. 5. Equivalent circuits of the proposed electronic ballast. (a) Interval t1-0, (b) interval t2-t1, (c) interval T-t2.

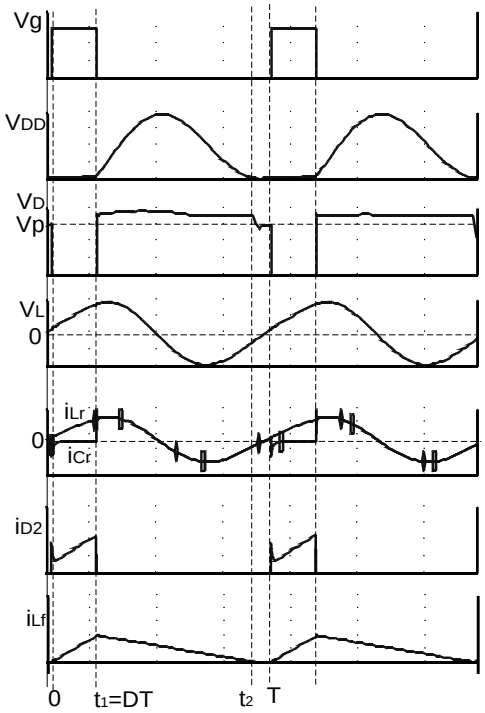

Fig. 6. Voltage and current waveforms of the proposed ballast.

Table I. Maximum stress voltage in the switch for different duty cycles.

D	k(D)	Vsmax (Buck-Boost)	Vsmax (Class E amplifier)	Vsmax/Vacp (Proposed topology)
0.1	2.09	1.111	0.232	1.111
0.2	2.318	1.250	0.580	1.250
0.25	2.474	1.333	0.825	1.333
0.3	2.66	1.429	1.140	1.429
0.4	3.145	1.667	2.097	2.097
0.5	3.849	2.000	3.849	3.849

C. Maximum voltage stress in the switch

The maximum voltage stress in the switch will be equal to the that existing in each semistage when operated independently. In each stage, the maximum voltage stress depends on the duty cycle, and this dependence is different for each semistage. For a buck-boost converter operated in discontinuous conduction mode the maximum voltage stress is the following:

$$V_{s\max bb} = \frac{Vac_p D}{1-D} + Vac_p = \frac{Vac_p}{1-D} \quad (1)$$

D being the switch duty cycle and Vac_p the peak line voltage.

The function between the maximum voltage stress in the switch, the input voltage and the duty cycle is more complex for the class E inverter loaded with a parallel resonant tank. In [10] this function is presented, which can be expressed as follows:

$$\frac{V_{s\max}}{V_{cc}} = k(D)$$

Table I shows the value of k(D) for different values of the duty cycle. Since the power factor correction converter is a buck-boost type, the voltage V_{cf} used to supply the class E amplifier will be the following:

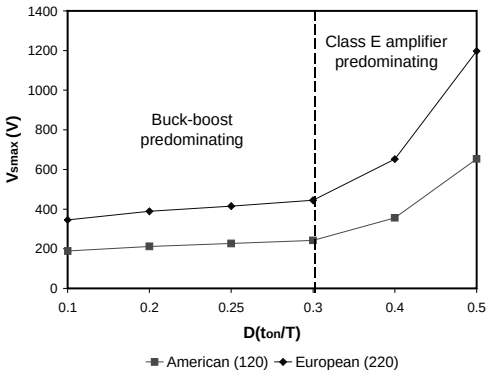

Fig. 7. Maximum voltage stress in the single switch of the proposed ballast in function of the duty cycle and for American and European line voltage.

Table I shows the value of k(D) for different values of the duty cycle. Since the power factor correction converter is a buck-boost type, the voltage V_{cf} used to supply the class E amplifier will be the following:

$$V_{Cf} = \frac{Vac_p D}{1-D} \quad (2)$$

where V_{cf} is the voltage across Cf capacitor. Therefore, the maximum voltage stress in the class E amplifier switch can be calculated as follows:

$$V_{s\max} = \frac{k(D) D Vac_p}{1-D} \quad (3)$$

Table I shows the maximum voltage stress for different duty cycles in both a buck-boost converter operating in discontinuous conduction mode and a class E amplifier with a parallel resonant tank. As can be seen, when duty cycle lower than 0.3 the voltage stress is higher in the buck-boost converter and when the duty cycle is greater than 0.4 the higher voltage stress is given by the class E amplifier. Table I also shows the voltage stress in the switch of the proposed topology.

As conclusion, the proposed ballast represents a feasible solution to the high voltage stress existing in the switch of a zero-voltage-switching class E amplifier, which is the main drawback of this topology when supplied from a high input voltage. In the proposed topology the voltage stress in the switch is quite lower than that obtained from a conventional class E amplifier. For example, for a duty cycle of 20% and European line voltage (Vca_p=220 Vrms) the maximum voltage stress in the switch would be V_{smax}=389 V. In order to achieve a similar operation with a traditional ZVS class E amplifier, the duty cycle should be equal to 50% and the switch voltage stress would be $V_{smax}=3.56Vca_p$=1107 V. Therefore, a 68.5% reduction of the switch voltage stress is achieved. The main disadvantage of the proposed ballast is the lost of ZVS commutations in the single switch.

Fig. 7 shows the switch voltage stress as a function of the duty cycle for American voltage (120 Vrms) and for European voltage (220 Vrms). As can be seen, in order to achieve switch voltage stresses lower than 500 V an operation with duty cycle below 0.3 is recommended.

D. Maximum current stress in the switch

The maximum current stress in the switch is given by the addition of the maximum current stresses in the buck-boost

converter and the class E amplifier. Assuming a unity input power factor, the maximum current stress in the buck-boost converter is given by:

$$I_{s\max bb} = \frac{2\sqrt{2}I_{acrms}}{D} \quad (4)$$

where I_{acrms} is the rms current absorbed by the circuit through the line.

For the class E amplifier with a parallel resonant tank, the maximum current stress in the switch is given by [10]:

$$I_{s\max ce} = \frac{2I_{cc}}{D} \quad (5)$$

Icc being the continuous current absorbed by the class E amplifier, which can be expressed as:

$$Icc = \frac{P_{in}}{Vcc} \quad (6)$$

where: Pin is the input power of the class E amplifier and Vcc is the voltage supplying the class E amplifier. In the proposed topology the voltage Vcc is given by (2). Therefore, combining (2), (5) and (6) and assuming a 100% efficiency and a unity power factor, the maximum switch current in the class E amplifier is obtained as follows:

$$I_{s\max ce} = \frac{\sqrt{2}I_{acrms}(1-D)}{D^2} \quad (7)$$

Finally, by adding (4) and (7) the maximum switch current stress is obtained for the proposed topology:

$$I_{s\max} = \frac{\sqrt{2}I_{acrms}(1+D)}{D^2} \quad (8)$$

The current I_{acrms} can be calculated as follows:

$$I_{acrms} = \frac{P_{in}}{V_{acrms}} \quad (9)$$

Fig. 8 shows the maximum current stress in the switch of the proposed topology as a function of the duty cycle, for both American and European line voltage and for an input power of 32W. As can be seen in this figure, for a duty cycle of 20%, the maximum current stress in the switch is approximately equal to 6.1 A in Europe and 11.3 America.

III. DESING EXAMPLE AND EXPERIMENTAL RESULTS

In this section the design of a prototype used to verify the behavior of the proposed topology is presented as an example. Also, some experimental results are presented to evaluate the possibilities of the proposed topology.

The input data are the following: line voltage Vac=127 Vrms, lamp is a 32W compact fluorescent lamp with an equivalent resistance of 123 Ω. Assuming an efficiency of 80%, the input power of the circuit will be P_{in}=40 W. Although the whole switch M1-D2 presents ZVS, the MOSFET M1 exhibits hard switching, and thus the selected switching frequency is f_s=150 kHz. The duty cycle at nominal operating point is chosen to be equal to 20%, thus obtaining both low lamp CCF and low switch voltage stress. Using the previous data, the DC bus voltage can be calculated with (2), obtaining Vcf=45 V.

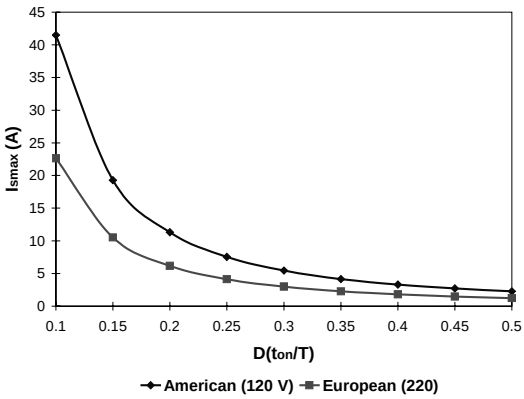

Fig. 8. Maximum current stress in the single switch of the proposed ballast as a function of the duty cycle, for American and European line voltage (Pin=32 W).

The design of the power stage is performed based on the following procedure:

1) Design of the buck-boost converter. In order to calculate the inductance Lf the following equation for the buck-boost converter operating in DCM is used [6]:

$$Lf = \frac{D^2 Vac_p^{\,2}}{4 f_s P_{in}} = \frac{0.2^2 180^2}{4(150000)(40)} = 54\mu H \quad (10)$$

Capacitor Cf is calculated using the following expression [6]:

$$V_{cfripple} = \frac{V_{cf}}{4\pi f_L R_i C_f} \quad (11)$$

f_L being the line frequency, R_i is the equivalent load of the buck-boost inverter and $V_{cfripple}$ is the voltage ripple in Cf. Taking into account that $R_i=V_{cf}^2/P_L=45^2/32=63.28$ Ω and for a voltage ripple equal to 10%, an electrolytic capacitor Cf=220uf /100V is selected.

2) Design of the class E amplifier with parallel resonant tank. The notation used to calculate the different elements was shown in Fig. 3. According to [10] for a duty cycle of 20% the equation used to calculate the nominal load resistance of a class E amplifier with only one inductor and one capacitor in load network ($Rn=R_{Lep}/n^2$) is: $Rn=0.7603V_{cf}^2/P_L=48.11$ Ω. The nominal inductive reactance of the load network is: XLn = XLr·XLsep/(XLr+Xlsep)=0.1653Rn=7.9578 Ω and the nominal capacitance is: Cn=5.3997/(Rn·2·π·f)=119.1 nF.

3) Calculation of Ls, Lr and Lr turn ratio. In Fig. 3a Cr corresponds to the nominal capacitance of a class E amplifier with only one inductor and one capacitor in load network, calculated in the previous paragraph. Lr is the transformer primary magnetizing inductance. Ls is the series inductor used to improve the current waveform through R_L. In order to calculate Ls and Lr, the relationship with the nominal values Ln and Rn must be calculated. This relationship is obtained transforming from two elements in series into two elements in parallel, as follows (see Fig. 3b):

$$XLs = \frac{XLsepR_{Lep}}{XLsep^2 + R_{Lep}^{\,2}} \quad (12)$$

$$R_L = \frac{XLsep^2 R_{Lep}}{XLsep^2 + R_{Lep}^2} \quad (13)$$

Transforming the equivalent parallel reactance of Ls XLsep to the primary, we obtain: XLsepr=XLsep/n^2. This reactance is in parallel with XLr (see Fig. 3c). The nominal inductance of a class E amplifier with only one inductor and one capacitor in load network is then obtained by simplifying the two parallel inductances in a single one (see Fig. 3d). Therefore:

$$XLn = \frac{XLrXLsepr}{XLr + XLsepr} \quad (14)$$

XLsep and XLr can be obtained from (12) and (13) respectively, as follows:

$$XLsep = \frac{R_{Lep}}{\sqrt{\frac{R_{Lep}}{R_L} - 1}} \quad (15)$$

$$XLr = \frac{XLseprXLn}{XLsepr - XLn} \quad (16)$$

Since R_{Lep}=Rn·n^2, then the ratio Rn·n^2/R_L must be higher than 1 in order to obtain a real value for XLsep from (15). This condition is not fulfilled for n=1 for the presented design. This is one the reasons for using a transformer instead of a single inductor Lr. Another important reason is that using n>1 the ignition voltage necessary to start the lamp discharge can be obtained without using extra circuitry. In this case, in order to achieve a suitable ignition voltage a value n=7 is selected. Then, using this value: R_{Lep}=(48.11)(49)=2537.52 Ω, and from (15) XLsep=574.15 Ω. Using (12) and (16): XLr=1215.31 Ω and XLs=542 Ω, and finally: Lr=26 μH y Ls=575 μH.

The switch used is a MOSFET IRF740, diodes D1 and D2 are MUR840 an diodes Db1-Db4 are BA159.

To start up the lamp, the switching frequency was varied from 15-150 kHz using one timer 555 and varying the frequency with a 2n2222 transistor placed instead of the resistor that fixed the frequency operation.

Due the buck-boost converter operate in discontinuous conduction mode an LC filter was employed to filter the component of high frequency. The values of the components of this filter are: Le=1 mH and Ce=20 nF.

The designed ballast was implemented in a laboratory prototype. The diagram of the implemented circuit is shown in Fig. 9. The implemented ballast is for instant start lamps with only one pin in both sides of the lamp. But is possible to adapt this design for rapid start lamps with two pins, it is possible adding an extra capacitor in parallel with the lamp. Experimental results obtained with the implemented prototype are shown in Figures 10-14.

Figure 10 shows the voltage and current waveforms in the lamp, which are symmetrical and nearly sinusoidal waveforms. The measured current crest factor was 1.5.

Fig. 11 shows the line voltage and current waveforms. The measured power factor was 0.99. Fig. 12 shows a comparison among the harmonics of the proposed ballast and the limits suggested by the international standard IEC-1000-3-2. As can be seen in this figure, all the harmonic of the proposed ballast comply with this standard.

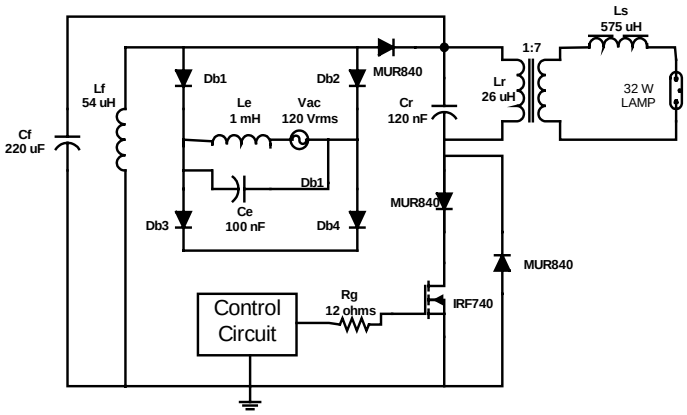

Fig. 9. Diagram of the implemented prototype.

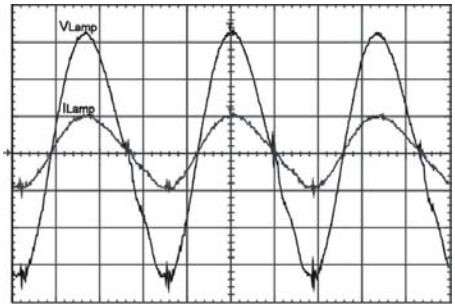

Fig. 10. Lamp voltage and current. 30 V/div, 0.5 A/div and 2 μs/div.

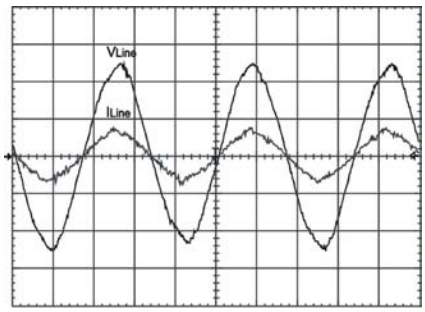

Fig. 11. Main voltage and current. 70 V/div, 0.5 A/div and 5ms/div

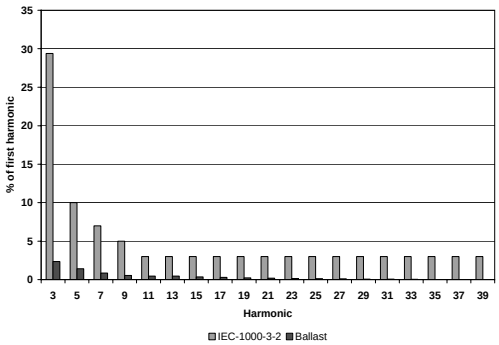

Fig. 12. Comparison among the harmonics of the proposed ballast and the limits suggested by the international standard IEC-1000-3-2

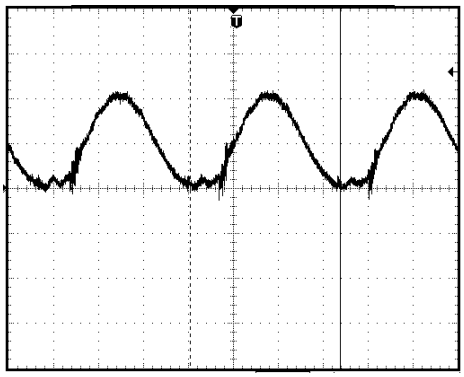

Fig. 13. Voltage waveform across D2-M1, 50 V/div and 2 μs/div.

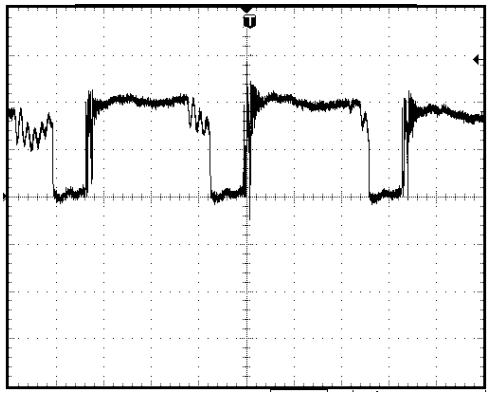

Fig. 14. Voltage waveform across M1. 100 V/div. and 2 μs/div.

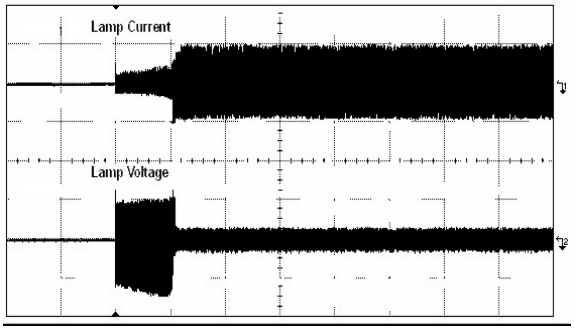

Fig. 15. Startup sequence of the lamp. 500 V/div, 0.5 A/div and 500 ms/div

Figure 13 shows the voltage waveform across switch D2-M1. As can be seen in this figure, the maximum voltage stress for this sample is 114V and the switch D2-M2 presents ZVS. Fig. 14 shows the voltage waveform across M1. In this figure the hard switching of the MOSFET can be seen. The maximum voltage stress obtained in M1 for this sample was 202V and the maximum current stress was 5.45 A. The measured efficiency was 80%.

Fig. 15 shows the startup sequence of the ignition of the lamp. This figure shows the lamp voltage and current during the startup of the lamp. As can be seen in this figure the lamp needs 500 ms approximately to ignite and the ignition voltage applied to the lamp is 505 V.

IV. CONCLUSIONS

In this paper a new single-stage single-switch electronic ballast featuring high input power factor, low lamp current crest factor, ZVS commutations and low switch voltage stress has been presented. The proposed electronic ballast is obtained by integrating a buck-boost converter and a class E amplifier with only one inductor and one capacitor in the load network. The asymmetric waveforms obtained in the class E amplifier with only one inductor and one capacitor in load network are improved by using an extra inductor in series with the load. The low voltage stress in the switch is obtained using duty cycles lower than 50%. Thus, the buck-boost converter operates in buck mode reducing the input voltage of the class E amplifier and consequently the switch voltage stress. Lamp ignition is achieved by using a transformer in place of the class E amplifier resonant inductor. The almost unity input power factor is attained operating the buck-boost converter in discontinuous conduction mode.

A design example has been also presented in this paper. Simulation and experimental results measured from a laboratory prototype based on the design example have been also included. The basic results are: lamp CCF 1.5, input power factor 0.99 and efficiency 80%. The main disadvantage of the proposed converter is the high current stress in the switch. However, as opposed to other electronic ballasts this topology can be used to supply fluorescent lamps from the high line voltage ratings using only one controlled switch.

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