A 300A DYNAMIC ELECTRONIC LOAD BASED ON MODIFIED BUCK+BOOST INTERLEAVED CONVERTER

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***Abstract* – This paper presents a novel DC dynamic electronic load applied at load regulation tests of switching-mode power supplies, operating at high-current levels. The proposed device is based on the use of a modified Buck+Boost interleaved converter, without the use of the boost diodes, and the output filters (capacitors). Therefore, the electronic load circuitry is very simple, effective and capable to provide high pulsed-current levels, featuring faster rise/fall times for transient testing on high speed DC to DC converters and DC power supplies. A prototype was implemented, in order to validate the proposed structure, operating at 10V-20V DC input voltage range, 190A-290A amplitude range of the input pulsed-current (nominal value is equal to 240A±20%), with adjustable pulse-width between 4ms (adjustable time-period of 200ms) until 6ms (adjustable time-period of 350ms). The main experimental results, obtained from the implemented prototype, are presented in order to demonstrate the feasibility of the proposed dynamic electronic load, which is capable of performing experimental tests of transient load regulation for switching-mode power supplies.**

***Keywords* – Interleaved converter, Dynamic electronic load, Pulsed-current, Dynamic tests.**

I. INTRODUCTION

The dynamic characteristics of dc to dc switching-mode power supplies involve their behavior as a result of non-steady loads, transients, and, in general, alternating currents that are superimposed on the dc output level.

If a voltage-regulated power supply is to be used with circuitry that generates pulses or spikes, it is not enough to specify low output impedance over an appreciable sine-wave frequency range. Switching transients can prevent realization of the output impedance, which prevails for a passive "clean" load. Switching-mode power supplies require a relatively long time to recover from the effects of abrupt load or line changes. Although specification criteria differ among manufacturers, the underlying philosophy is essentially similar. An abrupt change in load current provokes an oscillatory response that is generally characterized by overshoot and undershoots through the limits of the static-regulation band. The severity of the overshoot and undershoot, as well as the number of oscillations that are required to return to the regulation band, varies with different designs [1-2].

In this context, different types of electronic loads for testing power supplies have been developed and commercialized. They provide many functions including constant resistance, constant power, constant current and constant voltage modes, or a combination of these modes for static or dynamic tests, in order to facilitate the testing process for power electronics engineers [3-5].

In order to attend these features, this paper presents a novel Dynamic Load operating as an essential product to perform experimental tests of transient load regulation for switching-mode power supplies, specified by a manufacturer (Power Electronics Company-INDEL), capable of absorbing high pulsed currents with controlled magnitude, time-period and pulse-width.

II. THE PROPOSED CONVERTER

The initial challenge was to develop a group of loads with high input current capacity with both controlled pulse-width (tc) and magnitude (I), as shown in figure 1.

It should be noticed that several circuits were analyzed, in order to comply with the design restrictions imposed by the manufacturer. Among them, the simplest solution, but not efficient, is using a fixed value resistor (as a static load) added to several independent switches to allow that all of the resistors can be connected in parallel (as a dynamic load), as shown in figure 2.

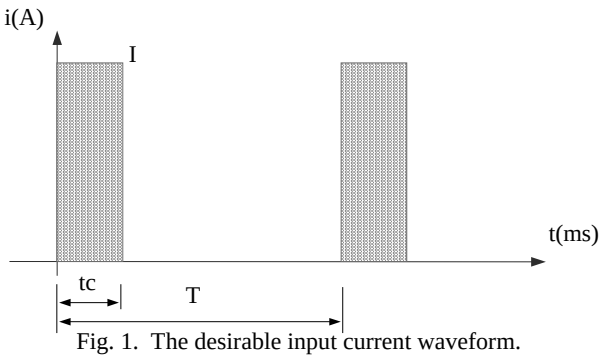

Fig. 1. The desirable input current waveform.

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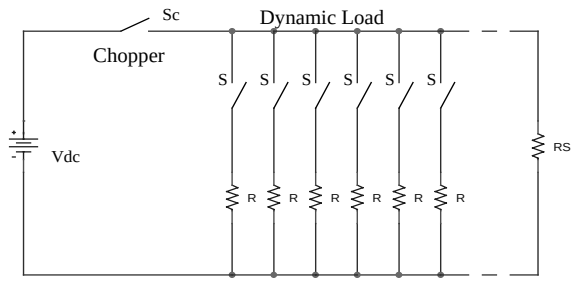


Fig. 2. Dynamic load based on switched resistors.

The dynamic electronic load should comply with the following specifications:

- DC voltage range operates between 10 and 20V.
- Nominal magnitude of the demanded current pulses equal to 240A, with continuous variation of ±20%, i.e., the amplitude of the pulsed-current is from 190A up to 290A, approximately.
- Adjustable pulse-width between 4ms and 6ms.
- Period among adjustable pulses between 200ms and 350ms.

The minimum value of the load can be implemented starting from a fixed value of resistance, while the variable portion of the current, added to the fixed value, should have continuous variation, in order to be represented by a variable load.

Therefore, as a first attempt, a Buck+Boost converter was considered for implementation, according to figure 3. In this proposed circuit, the minimum value of load (or static load) is defined for the conduction of the switch S1 through RS, during the time interval tc. The dynamic load (specified by C and RD) depends on the switching function of the boost converter. The input current of the converter (through the voltage source Vdc) has the same ripple that the current through the boost inductor. A high value of the inductance for this inductor guarantees low current ripple, however, it results in a high rise-time for the pulsed-current.

The interleaved power conversion refers to the strategic interconnection of multiple switching cells operating with identical switching frequency, where its internal turn-on instants are sequentially phased over equal fractions of a switching period. This arrangement reduces the net ripple amplitude and raises the effective ripple frequency of the overall converter without increasing switching losses or devices stresses. Therefore, an interleaved system can allow savings in filtration and in energy storage requirements, resulting in greatly improved power conversion densities without penalty for the efficiency [6].

In this context, in order to perform low current ripple, and insignificant influence in the rise time of the current, it was proposed an interleaved topology for the dynamic load, as shown in figure 4.

The main objective of this design is to produce a pulsed-current in the input of the proposed converter, with a shape closed to the figure 1. Thus, the output variables, including output voltage, have low importance to reach the announced purpose. On the other hand, considering the topology shown in figure 4, the high reverse recovery currents of the diodes D2 and D3 are very important stresses to the converter's design.

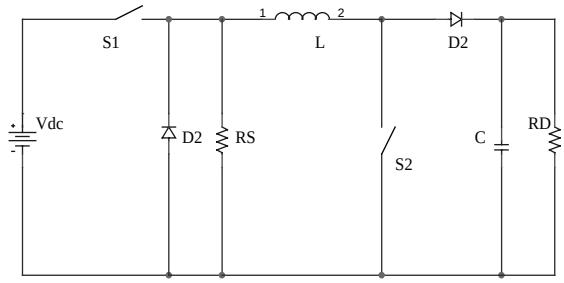


Fig. 3. Topology of the Buck + Boost converter.

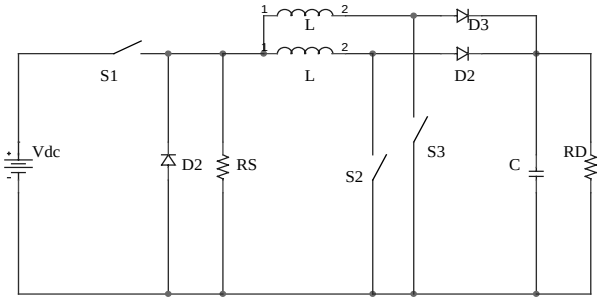


Fig. 4. Topology of the interleaved Buck + Boost converter.

In this context, a simple technique to solve the problems related to the reverse recovery currents of the diodes, considering the input current with fast fall-time, is to remove the two boost diodes and also to remove the output filter capacitor. Thus, the voltage over the resistor RD and its respective current become pulsed. Therefore, figure 5 shows the developed topology proposed for the electronic dynamic load, based on modified Buck+Boost interleaved converter.

The simple topology for the proposed electronic dynamic load, as shown in figure 5, is composed by the switches Sa and Sb, the inductors La and Lb, the resistors Ra and Rb, and the PWM command circuit, which perform the dynamic load characteristic. These devices are responsible to execute the peak current variations of ±20%, over its nominal value. This pulsed-current range is obtained by the variation of the voltage over the load resistors Ra and Rb, through the duty cycle control (D) of the switches Sa and Sb, respectively. Furthermore, the static load characteristic is performed by the switch Sp, the diode Dp, the resistor Rp, and one drive circuit, which include an optic coupler. The duty cycle control of the switch Sp allows to define the width and the frequency of the pulsed-current.

Despite a constant value of the input current conducting due to Rp, there is a variable portion for the dynamic load that also circulates through the switch Sp.

The diode Dp assumes the total peak current of the dynamic load, when Sp is turned off, until all the energy stored in La and Lb are dissipated in Ra and Rb, respectively. Although the demagnetization processes of the inductors are fast (with low value of average current), the diode Dp should be specified considering its repetitive peak current value.

III. EXPERIMENTAL RESULTS

It should be noticed that, considering that the converter involves high pulsed-current and low voltage values, several switches with low on-resistance were connected in parallel,

as well as the load resistors (Rp, Ra, and Rb), as shown in figure 5.

The main components, designed and used in the implemented prototype, are listed below:

(a) Static Load:
- Sp : 5 x MOSFET IRF1104
- Dp : 1 x Schottky Diode 81CNQ045
- Rp : 7 x 1Ω/60W
- Optic coupler : HP2211

(b) Dynamic Load:
- Sa : 2 x MOSFET IRF1104
- Sb : 2 x MOSFET IRF1104
- Ra = Rb : 5 x 1Ω/60W
- La = Lb = 10μH, 8 turns of 50 x 22AWG wire, Core: EE65-26
- PWM : LM3525

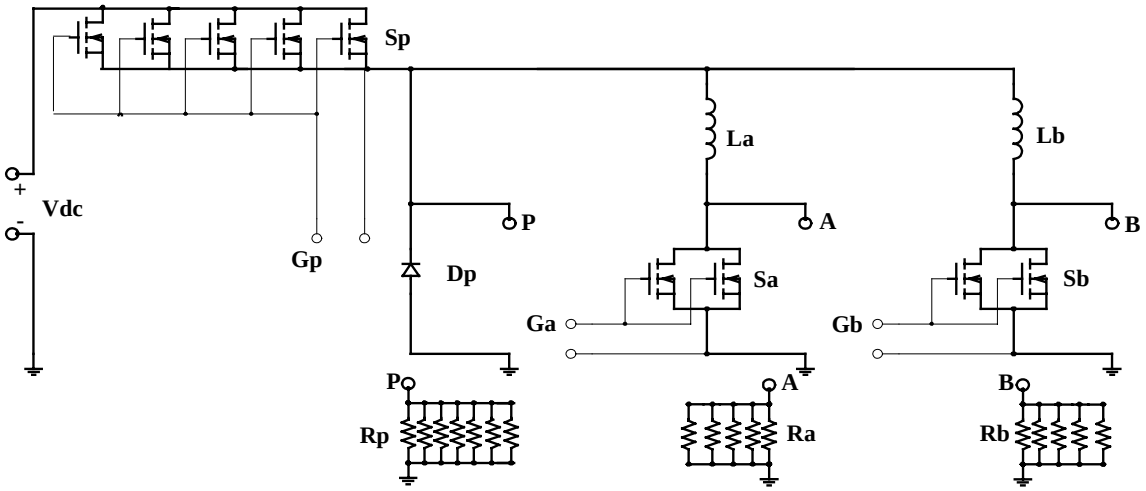


Fig. 5. The proposed converter for the dynamic electronic load.

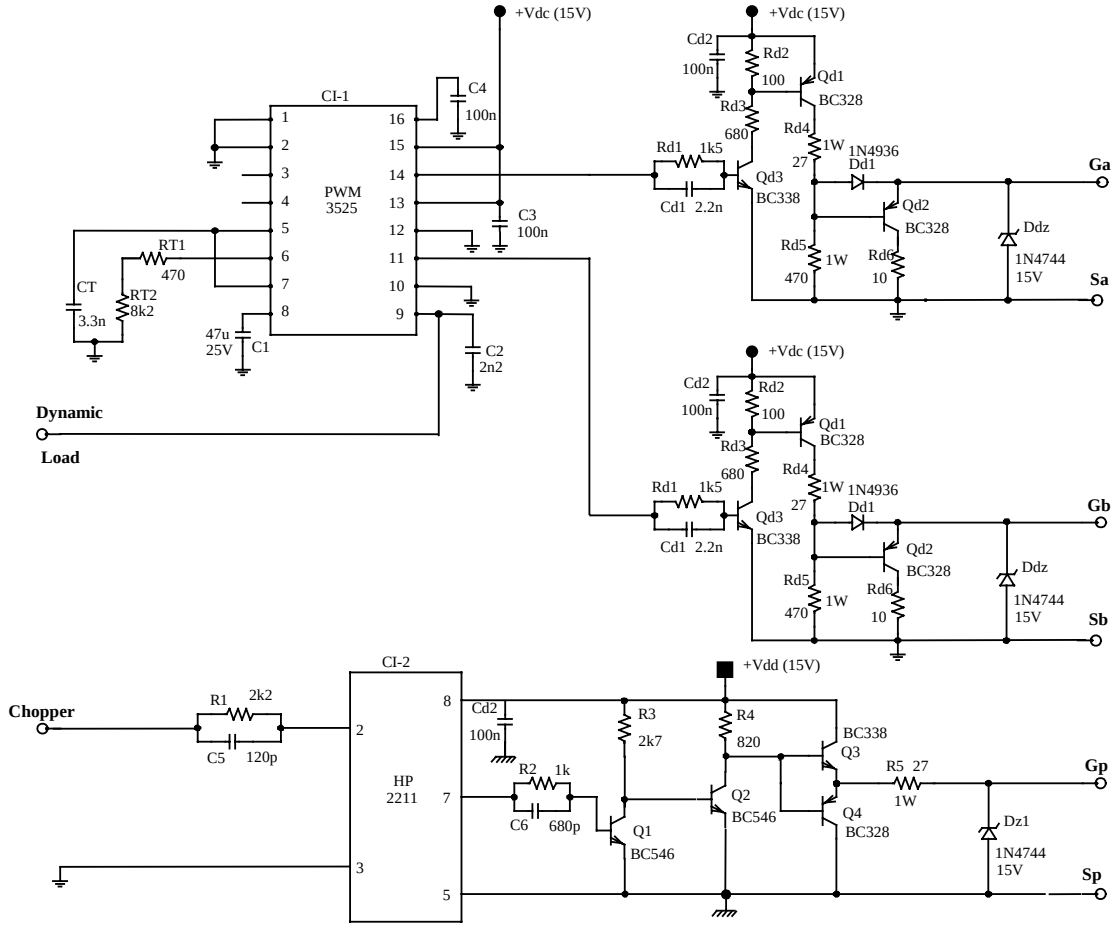


Fig. 6. The implemented control circuitry.

Figure 6 shows the main implemented control circuitry for the proposed electronic load, performing the specified features for dynamic tests of dc converters, and dc switching-mode power supplies.

Figures 7 and 8 show details of the implemented prototype. In addition, it should be noticed that the electronic load allows an external programmable pulse-width and adjustable period through an optic coupler.

The main experimental results, obtained from the prototype, are presented in the figures 9 until 14.

Figure 9 shows details of the current through the inductors La and Lb, and figure 10 shows the pulsed-current through one of the inductors (La) of the dynamic load. It is observed that, due to the phase-shift of the inductor currents, the input current ripple results smaller than the individual inductor current ripple, and the input current ripple presents a frequency twice the individual frequencies of the currents through La and Lb, due to the used interleaved technique. It should be informed that the switching frequency of the dynamic load is 25kHz.

Figure 11 shows the detail of the rise time of the input current, for equivalent duty cycle (D) at 0.45.

Figure 12 shows the input pulsed-current, considering a pulse-width of approximately 4ms. The pulse-width control of the static load is defined by an external auxiliary signal (for the purpose of these experimental tests, an external board, based on the mono-stable oscillator circuit UC4528, was implemented in order to perform the variation of the pulse-width control up to 6ms).

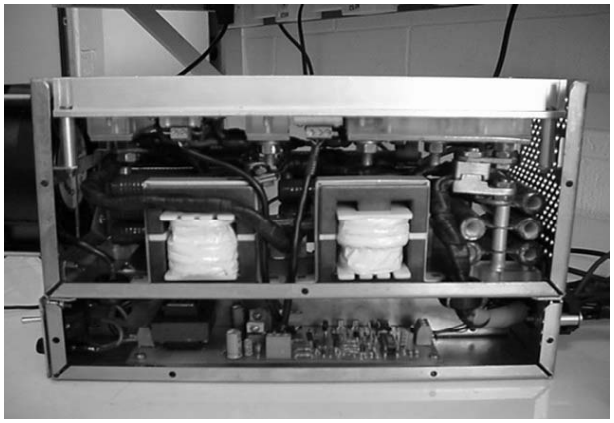


Fig. 7. Details of the Interleaved Inductors.

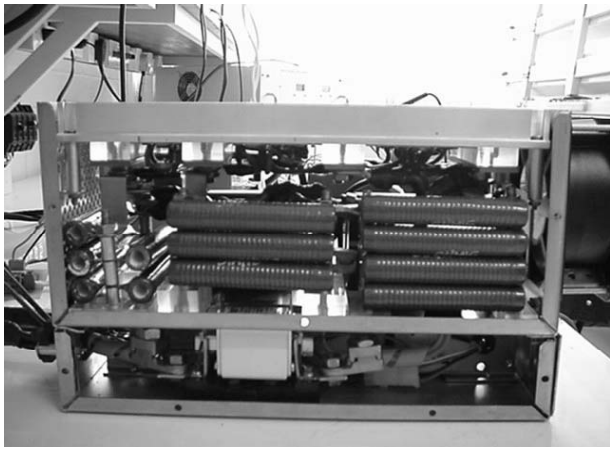


Fig. 8. Details of the Load Resistors.

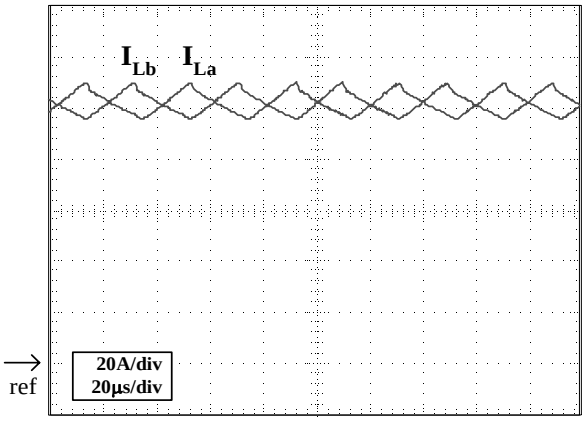


Fig. 9. Details of the currents through the inductors La and Lb (D=0.45).

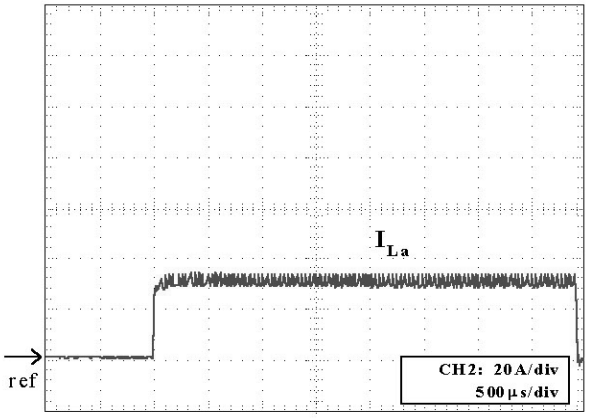


Fig. 10. Pulsed-current through La (D=0.45).

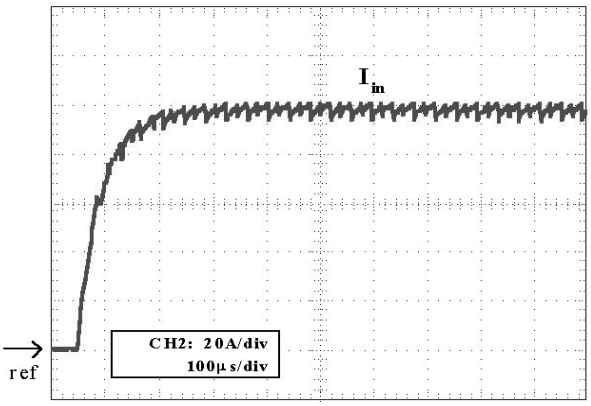


Fig. 11. Detail of the rise time of the input current (D=0.45).

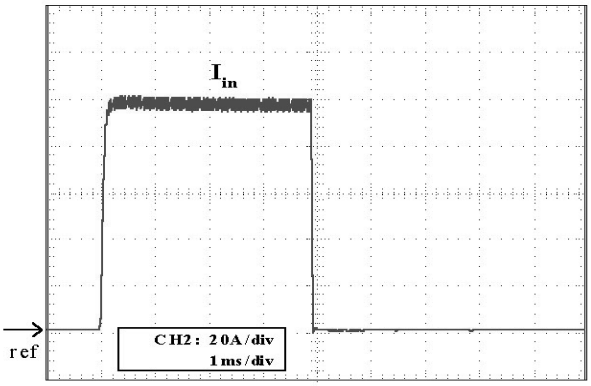


Fig. 12. Input pulsed-current (D=0.45).

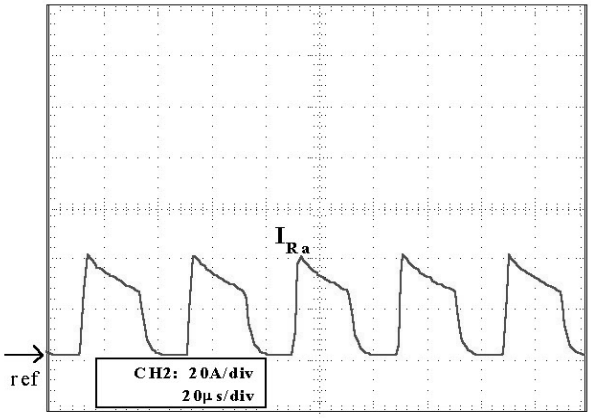


Fig. 13. Pulsed-current through Ra (D=0.45).

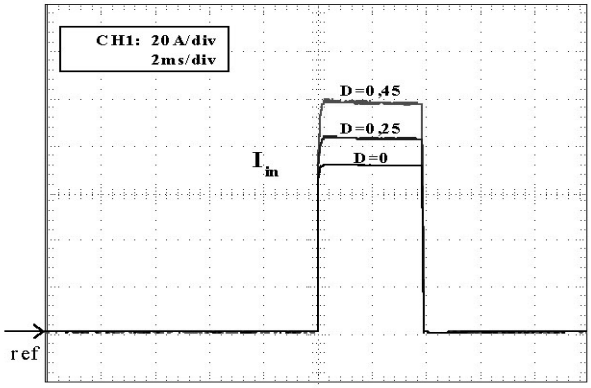
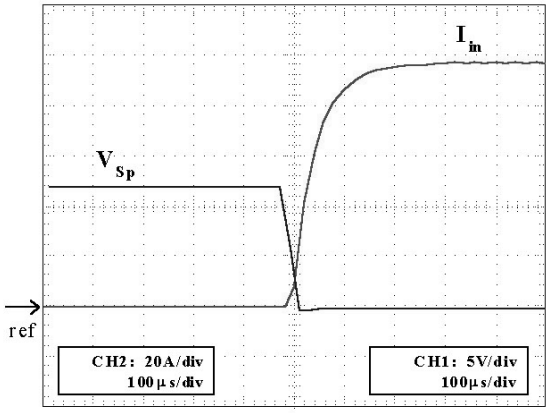
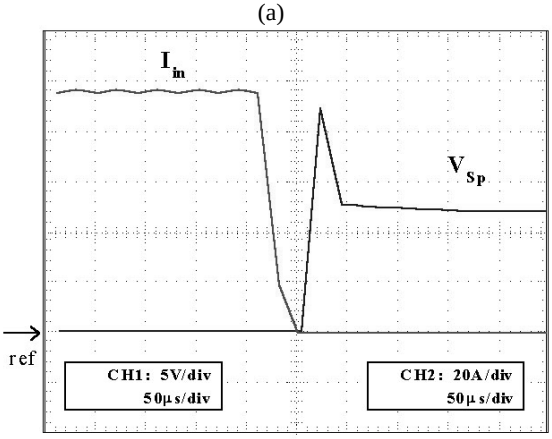


Fig. 14. Dynamic variation of the input pulsed-current (D=0 to 0.45).



(a)



(b)

Fig. 15. Commutation details for Sp, during its: (a)Turn-on, and (b)Turn-off; considering D=0.45.

Figure 13 shows the pulsed-current through one of the dynamic loads (Ra).

Finally, in figure 14, one can observe the dynamic variations of the input pulsed-current, driven by the command circuit strategy of the proposed dynamic electronic load. The designed dynamic electronic load operates at 10V until 20V of DC input voltage range, with 190A until 290A of amplitude range for the input pulsed-current, considering its nominal value equal to 240A (range: 240A±20%), and performing an adjustable pulse-width between 4ms (adjustable time-period of 200ms) until 6ms (adjustable time-period of 350ms).

Finally, it should be noticed that the switching losses are negligible, and the conduction losses were reduced through the use of Mosfets with reduced R_{DSon} , and Schottky Diode. Figures 15(a), and 15(b) show the commutation details for the switch Sp, considering D=0.45.

IV. CONCLUSIONS

A novel modified Buck+Boost interleaved converter, with the main purpose to obtain a dynamic electronic load with high level of pulsed current, was proposed in this paper. The proposed topology uses one static load and one dynamic load, without the use of boost diodes and the output filtering capacitor, performing an input pulsed-current range of 190A until 290A. The pulse-width, the magnitude and the period time of the input pulsed-current are controlled by a simple circuit strategy, and the converter provides an optic coupler for an external programmable control signal.

The main experimental results were presented in order to validate the proposed dynamic electronic load, capable of performing tests of load regulation for switching-mode power supplies, according to the manufacturer specifications.

Therefore, the proposed dc dynamic electronic load circuitry is very simple, effective and capable of emulating high pulsed-current levels, featuring fast rise/fall times for transient testing on high speed dc to dc converters and dc switching-mode power supplies.

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BIOGRAPHIES

Falcondes José Mendes de Seixas, was born in Jales - SP, in 1965. He received the B.S. degree in electrical engineering from Engineering School of Lins, in 1988 and the M.S. and Dr. degrees in electrical engineering from Federal University of Santa Catarina, Florianópolis, in 1993 and 2001, respectively. Currently, he is an Assistant Professor at the Department of Electrical Engineering at São Paulo State University and Treasurer in charge of the Brazilian Power Electronics Society - SOBRAEP. His research interests include active power-factor correction, switching mode power supplies and multi-pulse transformer for AC-to-DC applications.

Claudiner Mendes de Seixas, was born in Jales - SP, in 1969. He received the B.S. degree in electrical engineering from Engineering School of Lins, in 1991, the M.S. degree in electrical engineering from Federal University of Santa Catarina, Florianópolis, and the Master Business Administration from State University of Maringá, in 1993 and 2000, respectively. Since 1994, he is with the INDEL – Electronic Industry Ltd as a Maintenance Manager. His areas of interests include maintenance of the infra-structure equipments for telecom and engineering management.

Carlos Alberto Canesin, received the B.S. degree from São Paulo State University, Ilha Solteira(SP)-Brazil in 1984 and the M.S. and Ph. D. degrees from the Federal University of Santa Catarina - Power Electronics Institute, Florianópolis (SC), Brazil, in 1990 and 1996, respectively, all in electrical engineering. He started the Power Electronics Laboratory - LEP at the São Paulo State University, UNESP-FEIS, Ilha Solteira(SP), where he is currently an Associate Professor. He was Editor-in-Chief of the Brazilian Journal of Power Electronics, and Vice-president of the Brazilian Power Electronics Society-SOBRAEP. Currently, he is an Associate Editor for the IEEE Transactions on Power Electronics, Member of the Editorial Council of the Brazilian Journal of Power Electronics, Permanent member of the Deliberative Council of SOBRAEP, and President in charge of the Brazilian Power Electronics Society-SOBRAEP. His interests include soft-switching techniques, dc to dc converters, switching-mode power supplies, solar/photovoltaic energy applications, electronic fluorescent ballasts and active power-factor correction techniques.