

# ASSOCIATION OF AN INTERLEAVED BOOST-FLYBACK CONVERTER AND A FULL BRIDGE CONVERTER IN A SOFT-SWITCHING HIGH POWER FACTOR POWER SUPPLY

Carlos A. Gallo, Fernando L. Tofoli, João A. Corrêa Pinto\*, Ernane A. A. Coelho,  
Luiz C. Freitas, Valdeir J. Farias, João Batista Vieira Jr.

Universidade Federal de Uberlândia  
Faculdade de Engenharia Elétrica  
Núcleo de Eletrônica de Potência  
Campus Santa Mônica - Bloco "3N"  
Fone/Fax: 55 34 3239-4166  
CEP 38.400-902 – Uberlândia-MG – Brasil  
Email: [batista@ufu.br](mailto:batista@ufu.br)

(\*) Centro Federal de Educação Tecnológica do Pará  
(CEFET-PA)  
Coordenação de Eletrônica  
Av. Almirante Barroso, 1155 – Bairro Marco  
CEP 66.240-260 – Belém-PA – Brasil  
Fone: 55 91 226-0122 – Fax: 55 91 226-9710  
Email: [joao.pinto@cefetpa.br](mailto:joao.pinto@cefetpa.br)

**Abstract** — This work presents the analysis of a high power factor power supply operating at high switching frequency. An almost unity input power factor is obtained when an interleaved Boost-Flyback converter associated with a nondissipative snubber is used as a preregulator stage. A Full-Bridge converter is used as DC-DC stage, as the combination of both topologies results in the proposed SMPS. Theoretical background on each one of the converters is presented, and analytical results on the proposal are discussed in order to validate the proposal.

**Keywords** — SMPS, soft switching, high power factor.

## I. INTRODUCTION

Power supplies are very important units for electronic devices, because they provide the necessary voltages for the accurate operation of equipments. The evolution of such equipments has demanded the reduction of the size, weight and volume of power supplies. Generally, they employ AC voltages as primary power source, which must be converted to DC voltages [1].

Linear power supplies are adequate for low power applications, but are uneconomical and inefficient when more power is required. The alternative lies in the use of switched-mode power supplies (SMPS), which present multiple output DC voltages, constant switching frequency and reduced size and weight when compared with linear units [2].

However, the input stages of switched-mode power supplies are well known to be harmonic sources. Recently, there has been great interest about the reduction of the input current harmonic content and also power factor correction (PFC) [3]. Moreover, in many single-phase applications, the power levels can reach several kilowatts and, in some cases, the input voltage can be quite high as well. For such types of application, conventional Boost PFC converters have been intensively used as preregulator stages due to the characteristics of DC-voltage gain, lower inductor volume

and weight, and reduced losses on the power devices, which will affect converter cost, efficiency, and power density [3]-[5]. Conventional resonant and quasi-resonant converters [6]-[9] provide Zero-Current Switching (ZCS) and/or Zero-Voltage Switching (ZVS) [10]-[11], as they can operate at high frequency. However, such techniques have load limitation, because there are current and/or voltage stresses over the switches, and the control frequency range is restricted, complicating the design of the filter components. Interleaving techniques consist in the interconnection of multiple switching cells for which the operating frequency is the same, but the internal switching instants are sequentially phased over fractions of the switching period. The converter described in [12] employs this strategy with power factor correction IC UC3854, although the switching frequency is 100kHz. Within this context, this paper employs an interleaved Boost-Flyback converter to be used as a preregulator stage. Two switching cells operate at 100kHz each, as the design of the filter inductors and filter capacitors is performed with a switching frequency equal to 200kHz. It means that the sizes of the filter elements are substantially reduced if compared with the case studied in [13]. Further information about this converter can be found in [14].

Switched-mode power supplies are employed in DC voltage step-up or step-down. In this paper, a DC-DC converter is used in the process. There are several DC-DC converters that can be used in this case, but they are supposed to present multiple regulated output voltages, reduced switching losses and isolation, operating at high frequency. A DC-DC Full-Bridge converter [15] using a nondissipative snubber [16] that can reach high frequencies and high power levels is used in the proposed SMPS. This topology also presents some prominent advantages, as follows:

- Soft switching for a wide load range;
- Conduction losses are almost the same as those observed in the hard-switched converter.

## II. THE PROPOSED SMPS

As mentioned above, PFC is a desirable feature in power supplies, and a preregulator stage is necessary. Therefore an AC-DC stage is supposed to be associated with a DC-DC converter. The AC-DC and DC-DC converters are shown in Fig. 1 and Fig. 2, respectively, and Fig. 3 depicts the

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proposed SMPS. Switches  $S_1$ - $S_2$  and  $M_1$ - $M_3$  are turned on in ZCS mode, switches  $S_1$ - $S_2$  and  $M_2$ - $M_4$  are turned off in ZVS mode, due to the resonant cell, composed of three resonant

inductors ( $L_r$ ,  $L_{r1}$  and  $L_{r2}$ ), and four resonant capacitors ( $C_{r1}$ ,  $C_{r2}$ ,  $C_{r3}$  and  $C_{r4}$ ).

To simplify the analysis, the converters will be presented separately.

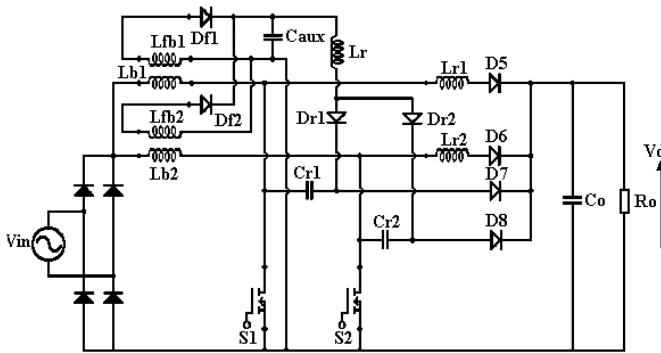


Fig. 1. AC-DC Interleaved Boost-Flyback Converter associated with a nondissipative snubber.

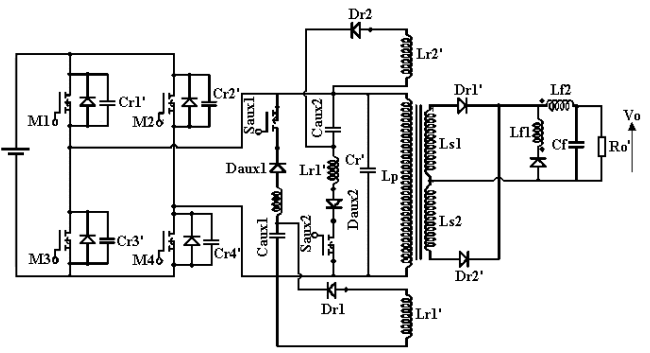


Fig. 2. DC-DC Full Bridge converter using a soft-switching cell.

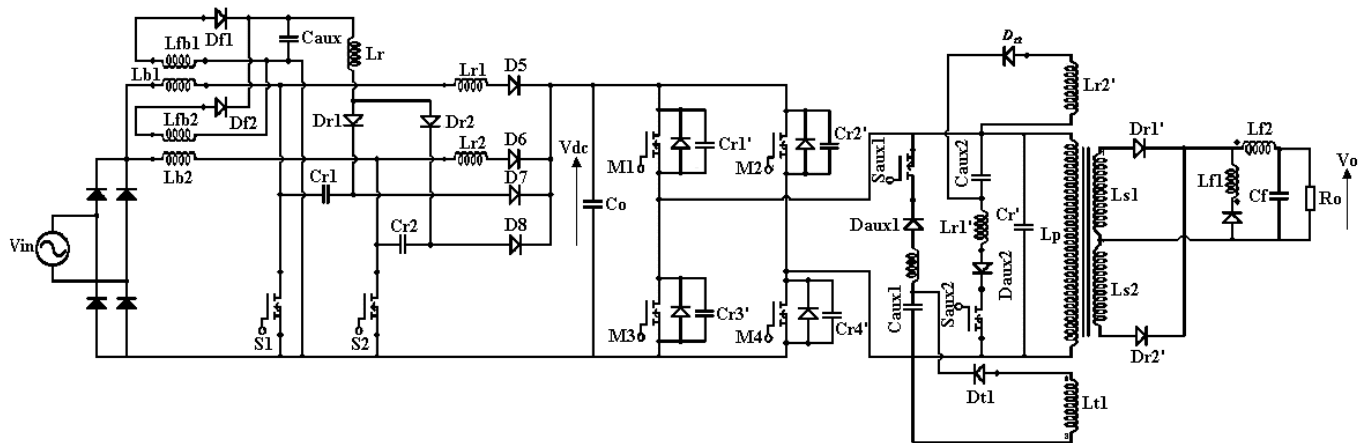


Fig. 3. Proposed high power factor switched-mode power supply.

### III. AC-DC INTERLEAVED BOOST-FLYBACK CONVERTER

Fig. 1 shows the interleaved converter associated with a nondissipative snubber to be used as a preregulator stage. The study of the converter is available in [14], and design guidelines on the circuit parameters are given in [18].

This stage operates with constant switching frequency and high power factor, using the average current mode control [19]-[20], illustrated in Fig. 4, which eliminates many serious problems, such as poor noise immunity, a need for slope compensation, and peak-to-average current errors which the inherently low current loop gain can not correct. However, the strategy demands current sensors and multipliers, increasing control complexity. In Fig. 4,  $T_{on}$  is the on-time of the switch driven by UC3854 and  $T_s$  is the switching period.

The control strategy represented in Fig. 5 monitors the input current, which is supposed to follow a reference signal. It is created when the rectified line voltage (A and C) is

multiplied by the output voltage (B). Hence the input voltage waveform is supposed to be nearly sinusoidal, which implies nearly unity displacement power factor and reduced harmonic distortion. In this case, this process is implemented by UC3854 [19].

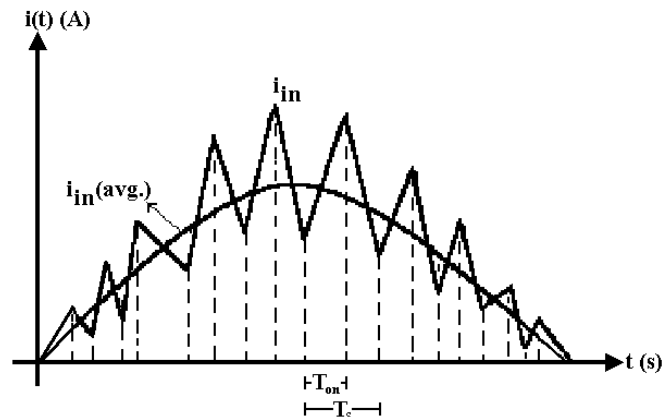


Fig. 4. Principle of the average current mode control.

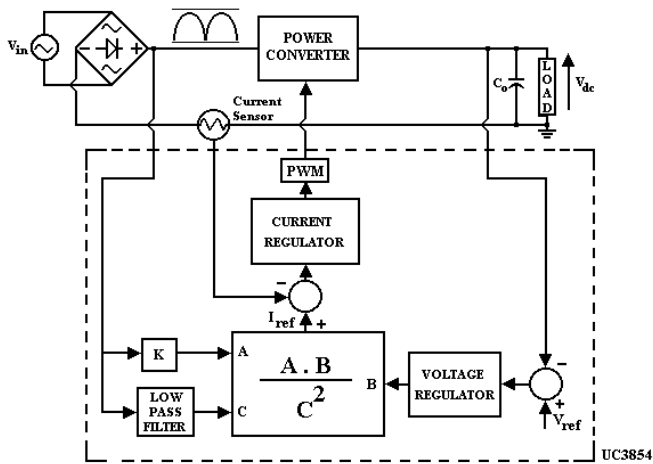


Fig. 5. Control strategy employed by the preregulator stage.

#### IV. DC-DC FULL-BRIDGE CONVERTER

Fig. 2 shows the Full-Bridge converter associated with a nondissipative snubber, representing the DC-DC stage of the SMPS.

This topology employs a coupled output inductor to minimize the currents through the primary winding and the main switches, resulting in reduced conduction losses and high switching frequency [22]. The snubber cell introduced here is an adaptation of the structure presented in [23]. Additional information on this approach can be found in [21].

The converter operates using phase shift control. Gating signals are generated by using IC UC3525A, according to the block diagram shown in Fig. 6.

The transfer function between output voltage  $V_o$  and DC voltage  $V_{dc}$  is given by (1) [21].

$$G = \frac{\frac{1}{\pi} \left[ K \cos(K_5) - K \sqrt{1 - K_5} + \frac{1}{2\alpha_1} \right] K_{f01} + 2 \frac{D_1}{n}}{\frac{1}{\pi} \left[ \cos(K_6) - \frac{\sqrt{1 - K_5}}{K_{Lf} - 1} + \frac{1}{n\alpha_1} \right] K_{f01} + \frac{K_{Lf} - 2D_1}{K_{Lf} - 1}} \quad (1)$$

where:

$1/n$  – turns ratio.

From [21], one can obtain the waveforms shown in Fig. 7.

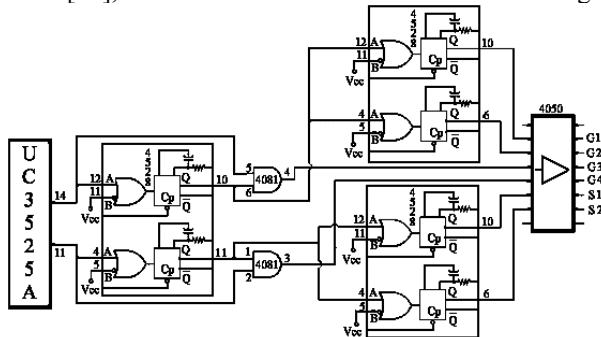


Fig. 6. Control circuit employed in the DC-DC Full Bridge converter.

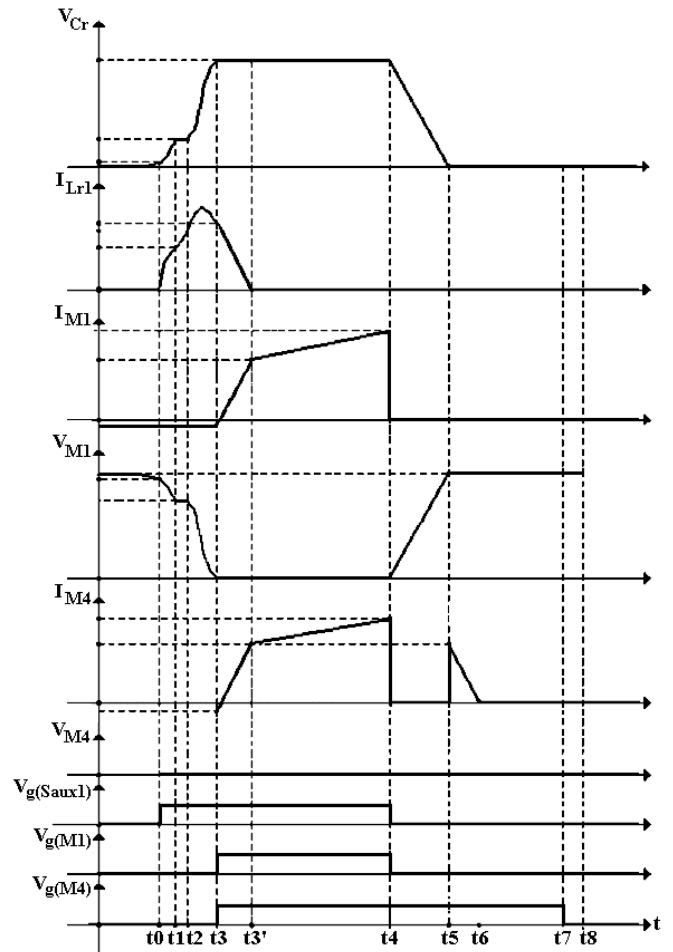


Fig. 7. Theoretical waveforms of the Full-Bridge converter.

The remaining parameters in (1) are given by definition as follows, according to [21].

$$K_{Lf} = \frac{L_{f1}}{L_{f2}} \quad (2)$$

$$K_{f01} = \frac{f}{f_{01}} \quad (3)$$

$$\alpha_1 = \frac{I_0}{V_{dc}} \sqrt{\frac{L_{r1}}{C_r}} \quad (4)$$

$$n_1 = n_2 = n \quad (5)$$

$$K_5 = \frac{V_{dc} - V_{aux1}}{V'_{Lf2} - V_{aux1}} \quad (6)$$

$$V'_{Lf2} = \frac{nV_0}{K_{Lf} - 1} \quad (7)$$

$$f_0 = \frac{\omega_0}{2\pi} \quad (8)$$

$$D = \frac{\Delta T}{T_s} \quad (9)$$

## V. SIMULATION AND EXPERIMENTAL RESULTS

The switched-mode power supply was analyzed via simulation tests using the parameters shown in Table I. A prototype of the proposed switched-mode power supply was also implemented using the parameters set shown in Table II.

In Fig. 8 (a) and (b), power factor correction at nominal load is evidenced, where the displacement power factor is above 0.99.

Fig. 9 demonstrates that the use of the average current mode control is efficient causing the reduction of the input current harmonic content. It must be mentioned that the input voltage is pure sinus in simulation tests.

Fig. 10 shows soft commutation in switch  $S_1$ , which is turned on and off under ZCS and ZVS conditions, respectively.

Fig. 11 and Fig. 12 present simulation and experimental results regarding switches  $M_1$  and  $M_2$ , respectively.

Fig. 13 shows the main waveforms of the resonant elements, and Fig. 14 corresponds to switch  $S_{aux1}$  voltage and current waveforms, which is turned on in ZCS mode.

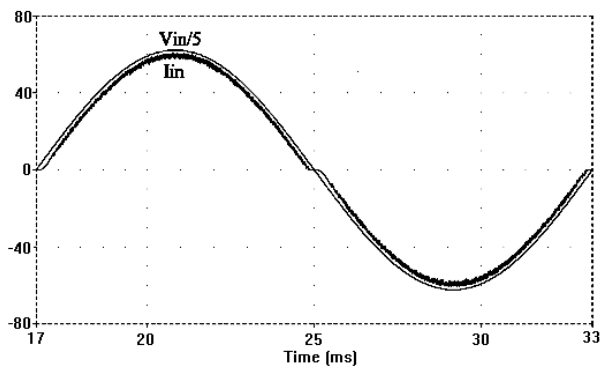
Fig. 15 shows the efficiency curve of the switched-mode power supply. It can be seen that the efficiency at nominal load is quite high i.e. above 90%.

**Table I**  
Parameters set used in the simulation tests

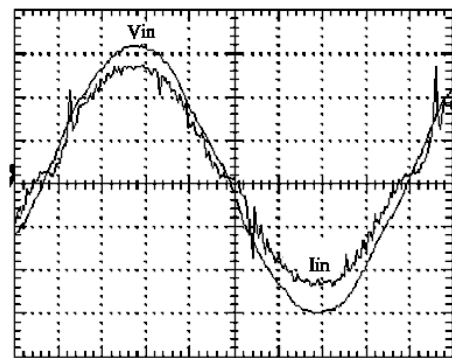
Parameter	Value
All switches	Ideal
All diodes	Ideal
Output voltage	$V_o=60V$
Output power	$P_o=2000W$
Output current	$I_o=33.3A$ ;
Resonant capacitors	$C_r=4.2nF$ $C_{r1}=15.6nF$ $C_{r2}=7.8nF$
Resonant inductors	$L_r=L_{r1}=L_{r2}=2.5\mu H$
AC input voltage	$V_{in}=127/220V$
Primary inductance	$L_p=1.2mH$
Secondary inductance	$L_s=550\mu H$
Tertiary inductance	$L_t=600\mu H$
Switching frequency	$F_s=100kHz$
Filter capacitor used in the DC-DC stage	$C_f=1mF$
Filter capacitor used in the AC-DC stage	$C_o=680\mu F$

**Table II**  
Parameters set used in the experimental tests

Parameter	Value
All switches	IrfP460
All diodes	MUR1560
Output voltage	$V_o=60V$
Output power	$P_o=2000W$
Output current	$I_o=33.3A$ ;
Resonant capacitors	$C_r=4.2nF$ $C_{r1}=15.6nF$ $C_{r2}=7.8nF$
Resonant inductors	$L_r=L_{r1}=L_{r2}=2.5\mu H$
AC input voltage	$V_{in}=127/220V$
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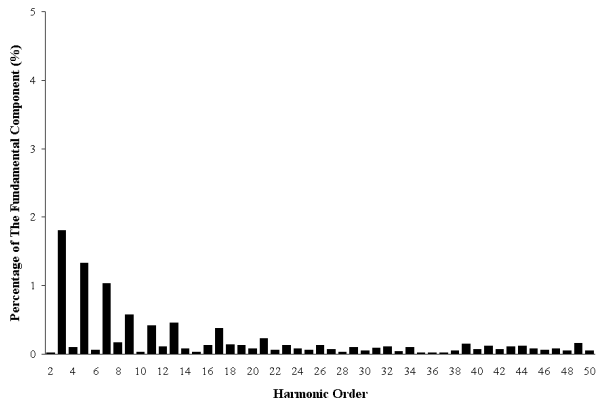
(a) Simulation results



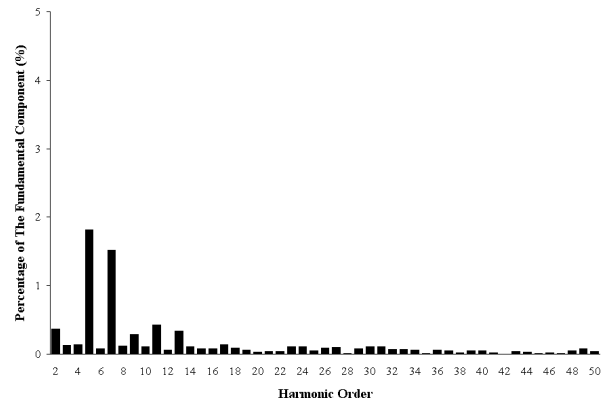
(b) Experimental results

Scales:  $I_{in} - 100V/div.$ ;  $V_{in} - 20A/div.$ ; time - 2ms/div.

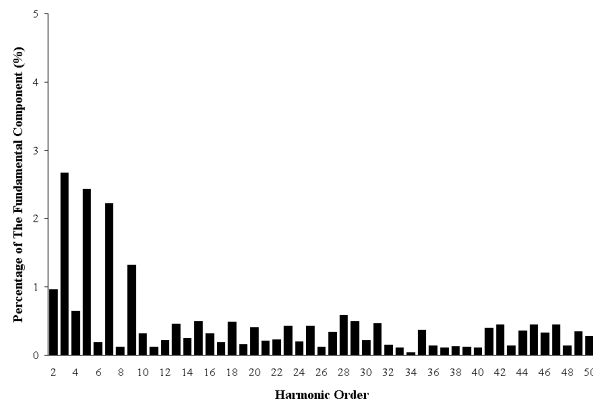
Fig. 8. Input voltage and input current at nominal load.



(a) Input current – simulation results ( $THD_I=2.84\%$ )

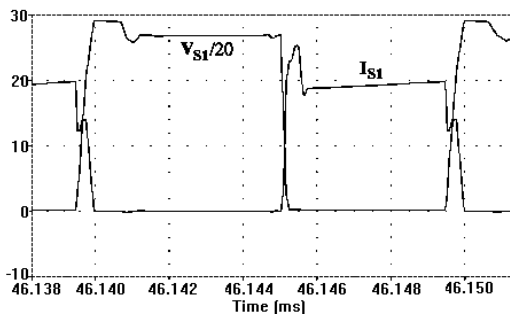


(b) Input voltage – experimental results ( $THD_V=2.83\%$ )

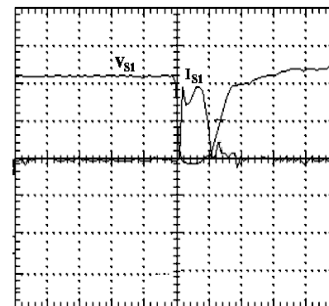


(c) Input current – experimental results ( $THD_I=4.85\%$ )

Fig. 9. Harmonic spectrum.



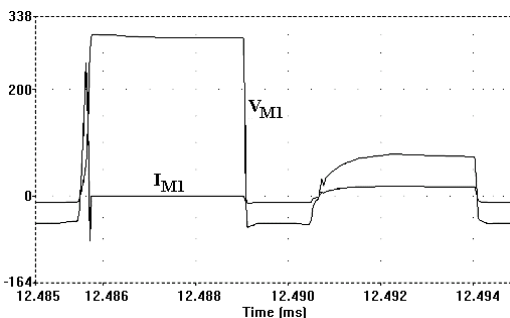
(a) Simulation results



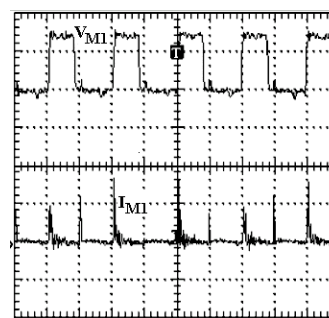
(b) Experimental results

Scales:  $V_{S1} - 200V/div.$ ;  $I_{S1} - 10A/div.$ ; time –  $2\mu s/div.$

Fig. 10. Drain-to-source voltage and current waveforms of switch  $S_1$ .



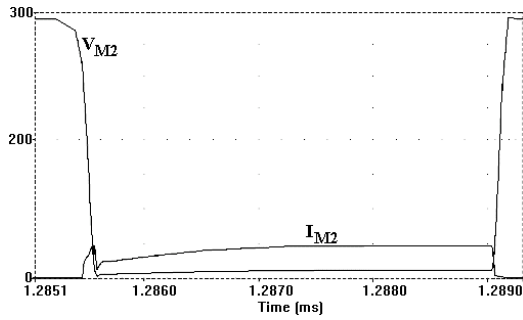
(a) Simulation results



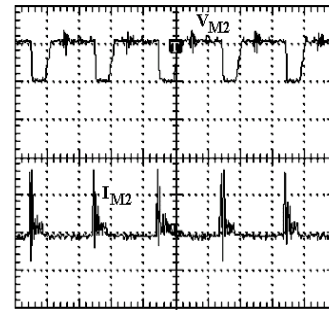
(b) Experimental results

Scales:  $V_{M1} - 200V/div.$ ;  $I_{M1} - 10A/div.$ ; time –  $5\mu s/div.$

Fig. 11. Drain-to-source voltage and drain current waveforms of switch  $M_1$ .



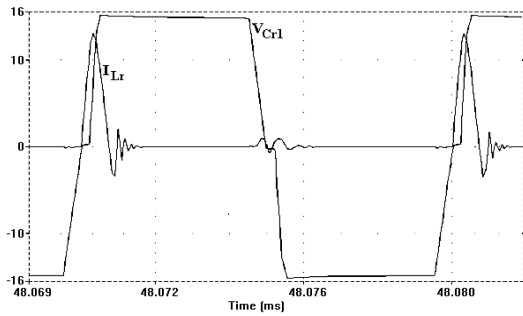
(a) Simulation results



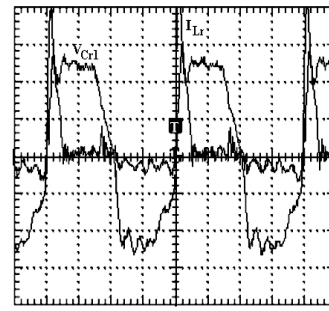
(b) Experimental results

Scales:  $V_{M2} - 300\text{V/div.}$ ;  $I_{M2} - 10\text{A/div.}$ ; time  $- 5\mu\text{s/div.}$

Fig. 12. Drain-to-source voltage and drain current waveforms of switch  $M_2$ .



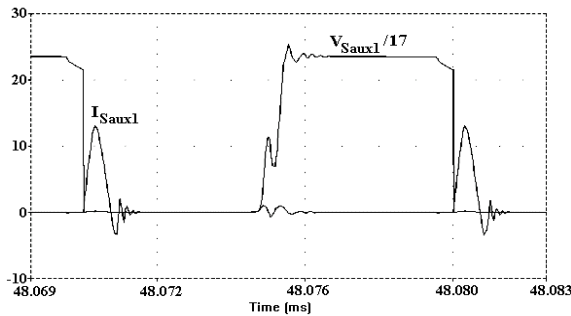
(a) Simulation results



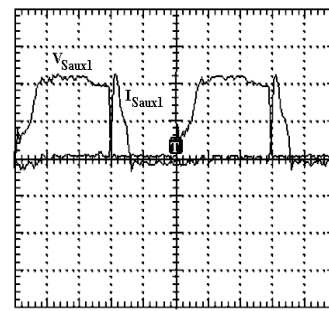
(b) Experimental results

Scales:  $V_{Cr1} - 50\text{V/div.}$ ;  $I_{Lr} - 4\text{A/div.}$ ; time  $- 5\mu\text{s/div.}$

Fig. 13. Resonant tank waveforms.



(a) Simulation results



(b) Experimental results

Scales:  $V_{Saux1} - 100\text{V/div.}$ ;  $I_{Saux1} - 4\text{A/div.}$ ; time  $- 2\mu\text{s/div.}$

Fig. 14. Drain-to-source voltage and drain current waveforms of auxiliary switch  $S_{aux1}$ .

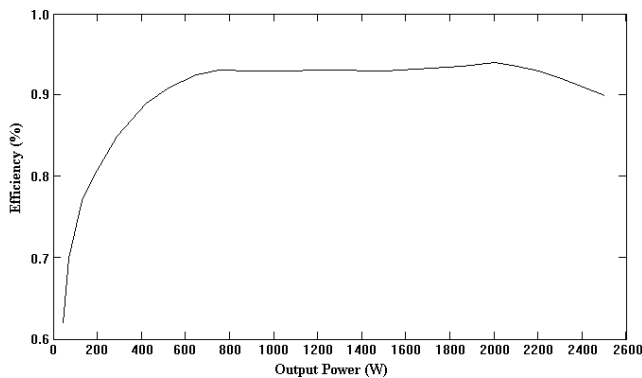


Fig. 15. Efficiency versus output power.

## VI. CONCLUSION

This paper has reported the analytical, simulation and experimental developments of a SMPS composed of two stages. The first stage is a soft-switched Boost-Flyback converter, and the second one is a Full-Bridge converter. The use of the average current control technique implies highly efficient power factor correction without commutation losses. The proposed approach also provides an optimum performance at high switching frequencies.

The objective initially proposed was achieved as a switched-mode power supply with unity input factor, high efficiency, low harmonic distortion rates and also regulated output voltage was analyzed theoretically, designed, evaluated and implemented successfully.

## VII. ACKNOWLEDGMENT

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## BIOGRAPHIES

**Carlos Alberto Gallo** was born in São José do Rio Preto, São Paulo, Brazil, on June 18<sup>th</sup>, 1974. He received the BSc and MSc degrees in Electrical Engineering from the Federal University of Uberlândia, Brazil, in 2000 and 2002, respectively. He is now PhD student at the same university. His research interest include high-frequency power conversion, microprocessor-based control of power converters, power factor correction topologies and UPS systems.

**Fernando Lessa Tofoli** was born on March 11<sup>th</sup>, 1976, in São Paulo, São Paulo, Brazil. He received the BSc and MSc degrees in Electrical Engineering from the Federal University of Uberlândia, Brazil, in 1999 and 2002, respectively. Nowadays he is PhD student at the Power Electronics Research Group of the same university. His research interests include power quality related issues, high

power factor rectifiers and soft switching techniques applied to static power converters.

**João Antonio Corrêa Pinto** was born in Belém, Pará, Brazil, on July 29<sup>th</sup>, 1955. He received both BSc degrees in Physics and Electrical Engineering from Federal University of Pará, Brazil, in 1982 and 1992, respectively. He also received the MSc and PhD degrees in Electrical Engineering from the Federal University of Uberlândia, Brazil, in 1997 and 2002, respectively. He is currently professor at Federal Center of Technological Education of Pará, Brazil. His research interests include high-frequency power conversion, modeling and control of converters, power factor correction circuits, UPS systems and new converters topologies.

**Ernane Antônio Alves Coelho** was born in Teófilo Otoni, Minas Gerais, Brazil, on April 1<sup>st</sup>, 1962. He received the BSc degree in Electrical Engineering from the Federal University of Minas Gerais, Brazil, in 1987 and the MSc and PhD degrees in Electrical Engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1989, and from the Federal University of Minas Gerais, in 2000, respectively. Presently he is titular professor of the Department of Electrical Engineering of the Federal University of Uberlândia, Brazil. His research interests are PWM inverters, power factor correction circuits and new topologies using digital control.

**Luiz Carlos de Freitas** was born in Prata, Minas Gerais, Brazil, on April 1<sup>st</sup>, 1952. He received the BSc degree in Electrical Engineering from the Federal University of Uberlândia, Brazil, in 1975, and the MSc and PhD degrees from the Federal University of Santa Catarina, Brazil, in

1985 and 1992, respectively. Nowadays he is with Department of Electrical Engineering of the Federal University of Uberlândia, Brazil. His research interests include high-frequency power conversion, modeling and control of converters, power factor correction circuits and novel converters topologies.

**Valdeir José Farias** was born in Araguari, Minas Gerais, Brazil, on November 18<sup>th</sup>, 1947. He received the BSc, MSc and PhD degrees in Electrical Engineering from the Federal University of Uberlândia, Brazil, in 1975, Federal University of Minas Gerais, Brazil, in 1981, and State University of Campinas, Brazil, in 1989, respectively. Nowadays he is with the Department of Electrical Engineering of the Federal University of Uberlândia, Brazil. His research interests are soft-switching converters and active power filters.

**João Batista Vieira Jr.** was born in Panamá, Goiás, Brazil, on March 23<sup>rd</sup>, 1955. He received the BSc degree in Electrical Engineering from the Federal University of Uberlândia, Brazil, in 1980 and the MSc and PhD degrees from the Federal University of Santa Catarina, Brazil, in 1984 and 1991, respectively. He started working as instructor teacher at the Department of Electrical Engineering of the Federal University of Uberlândia in 1980 where he is currently titular professor. His research interests include high-frequency power conversion, modeling and control of converters, power factor correction circuits and new converters topologies. He is member of the Brazilian Society of Automation (SBA) and member of the Brazilian Society of Power Electronics (SOBRAEP).