MAGNETICALLY-COUPLED CURRENT SENSOR USING AN INTEGRATED COIL AND A CMOS SPLIT-DRAIN TRANSISTOR

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***Abstract* – An integrated current sensing circuit intended for Smart-Power and embedded applications featuring galvanic isolation is implemented. It is based on magnetic detection using the CMOS compatible Split-Drain transistor (MAGFET) that provides a very linear output current versus magnetic field. The current to be sensed flows through an integrated coil placed atop the split-drain transistor and produces a relatively strong magnetic coupling enough to cause a detectable transistor unbalance current. An integrated sensor built in 0.35μm CMOS technology presented an output conversion factor of 1500nA/A and a minimum detectable magnetic field around 1μT within 1Hz bandwidth in thermal range for 100μA transistor bias current.**

***Keywords* - Magfet, split-drain, noise, current measurement.**

I. INTRODUCTION

Current sensing is one of the most important functions to be implemented on a smart power chip, hybrid systems and power electronics applications [1]. In addition to providing current limitation, it is also required to detect failure situations such as short-circuit or open-load as well as to provide the feedback signal to control purposes. The classical method for current sensing is to insert a sensing resistor in the current path of power device to obtain a voltage signal that can be read by the analogue circuitry. Such a simple method has a disadvantage of introducing additional losses in the smart power circuit. Other techniques include the drain-source resistance voltage reading. The main drawback of this technique is the low accuracy due to the non-linearity of drain-source resistance. This method enjoys commercial use because of its efficiency (no additional resistor is used). Another technique was introduced in [2]. It uses the inductor voltage (in the case of a DC-DC PWM converter) to measure the inductor current. The approach is based on an integrator that converts voltage to current by integration over time. The main disadvantage is that the inductor value should be known exactly. Another very employed technique is based on the SENSEFET [3]. The idea is to build a parallel MOS transistor with the main one to share a proportional load current. Since the V_{GS} and V_{DS} are the same, the current sharing will follow the rationed transistors areas. Despite being a practical approach, additional circuitry is necessary to follow the V_{DS} voltage, bringing about extra complexity when the technique is applied to either high-side or low-side drivers. Moreover, the technique is reported to be both noisy and low-bandwidth [4]. And last but not least, the SENSEFET approach does not present a galvanic isolation between power circuit and control circuitry, what can result in inconveniences in some applications. As an alternative solution, an integrated circuit application based on magnetic coupling using a split-drain transistor and an integrated coil placed on top of it and over the field silicon dioxide layer it is presented in this paper. This approach assures a real galvanic isolation because there is no electric connection between the split-drain transistor and the coil, whereof the current associated with the power or high-voltage circuit flows through. In an integrated circuit, the field silicon dioxide layer can bear about 1MV/mm allowing galvanic isolation-featured applications such as in the automotive industry, telecommunications, switched converters, household appliances and so on. As the current image instead of the actual one is needed for measuring and controlling purposes, the integrated coil can sense a scaled current by using a shunt element, external to the circuit and sized according the required application. Despite this approach be a current-sense one, voltage can be measured as well. It is enough to place a resistor and the coil in series to limit the current. Being the integrated coil self-inductance very low, the applied voltage will control the current and therefore the magnetic flux, allowing such voltage measurements, even at fairly high frequencies. This paper is organized as follows: In section II some basic aspects of the split-drain sensor is revised. In Section III, the 0,35μm CMOS integrated circuit is presented. Section IV addresses the thermal noise issues and associated resolution above the 1/f region. Section V shows some experimental results followed by the conclusions.

II. SPLIT-DRAIN-BASED MAGNETIC SENSOR: BASICS

The envisaged current sensor is based on the well-known magnetic sensor CMOS-compatible Split-Drain transistor (MAGFET) [5], [6]. This sensor produces a current imbalance dictated by Lorentz force and can detect perpendicular magnetic field upon it, according (1).

$$\Delta I = S.I_B.B \tag{1}$$

In (1), ΔI stand for the total current imbalance between the drain terminals of the transistor given in [Ampere], S the

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device sensitivity [1/T], I_B the split-drain bias current [Ampere] and B the magnetic field [T] applied perpendicularly to the device. The sensitivity depends on the device geometry (length and width) and Hall carrier mobility (μ_H) and is related to (2).

$$S = \mu_H . G . \frac{L}{W} \tag{2}$$

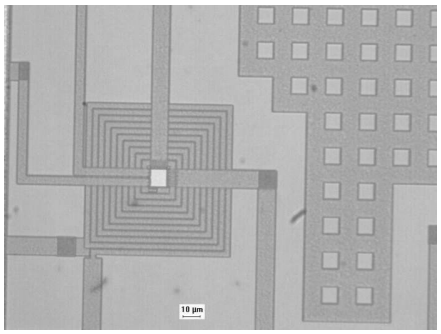
For rectangular shapes in the range $0.85 < W/L < \infty$, the geometrical correction factor (G) is given in (3) [6]. For square geometries, G=0.676.

$$G = 1 - \frac{16}{\pi^2} . e^{\frac{-\pi}{2} . \frac{W}{L}} . \left(1 - \frac{8}{9} . e^{-\pi . \frac{W}{L}} \right) \tag{3}$$

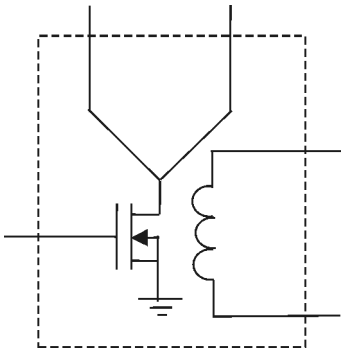
The Hall mobility (μ_H) is given by the product of the effective carrier mobility μ (process-based) and the Hall Factor r_H. According [7], the Hall factor for NMOS transistors is r_H=1.05 within the temperature range $-20^o < T < 120^o$ degrees Celsius. This value is considered to be appropriate for most practical applications. The carrier mobility parameter in the used 0,35µm CMOS process is μ=0,037m^2/V.S for NMOS transistors. The above expressions will be used in next session.

III. IMPLEMENTED CURRENT SENSOR

A double metal-layer (available in the 0,35µm CMOS technology) integrated coil and the split-drain transistor whose dimensions are W=10µm and L=10µm make up the sensor circuit as indicated in Figure 1.



(a)



(b)

Fig. 1. (a) Photomicrograph of the integrated coil and MAGFET transistor. (b) Equivalent electric circuit.

The coil is placed atop the transistor to concentrate the magnetic flux lines. As the involved distances are of the micrometer order, the magnetic field intensity is enough to be detected by the split-drain transistor. Figure 2 illustrates schematically the positioning of the coil and the split-drain transistor, whose distances are obtained from the employed technology.

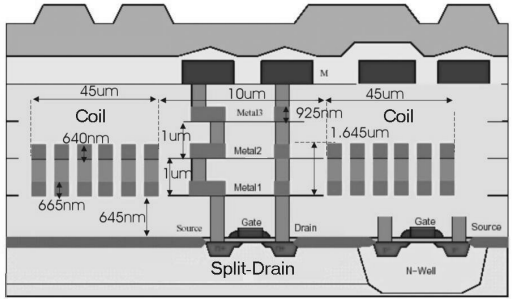
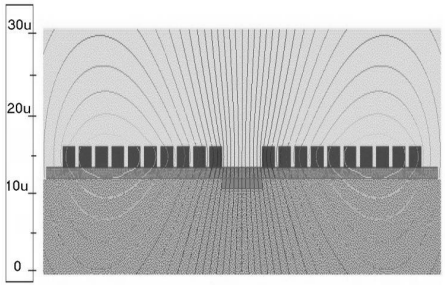
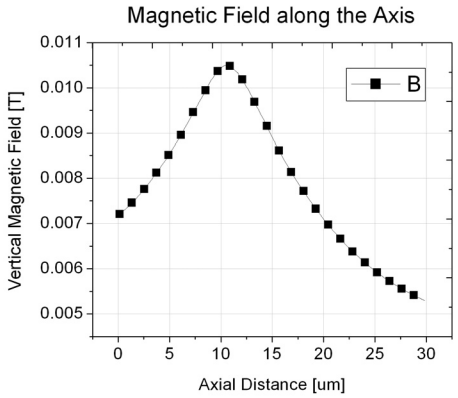


Fig. 2. Schematic view of the implemented sensor in 0,35µm technology and associated dimensions.

Electromagnetic simulations allow evaluating the magnetic field generated by the carrying-current coil. The MAXWELL 2-D electromagnetic software simulator can be used for determining the coil-generated magnetic field to the coil-current ratio (F_C). Thus, the obtained value from electromagnetic simulations was F_C=590mT/A for the coil-transistor placement indicated in Figure 2. This value will be used in conjunction with (1) to determine the split-drain output current. The generated-coil magnetic flux line plot is illustrated in Figure 3(a), whereas Figure 3(b) shows the vertical magnetic field for a 20mA coil current along its axial distance starting at approximately 10µm below the split-drain transistor. The F_C factor can be obtained from this graph. As indicated, the maximum vertical magnetic field perpendicular to the MAGFET plane is obtained at the center of the coil. Electromagnetic simulations can also evaluate the self-inductance taking into account the coil geometric parameters, viz., total length and track width. The computed value was 390nH.



(a)



(b)

Fig. 3. (a) Magnetic flux lines generated by the coil. (b) Vertical Magnetic Field computed along the coil axis for I_{COIL}=20mA.

The NMOS split-drain transistor aspect ratio was chosen unity (L=W=10μ) so the sensitivity obtained is very close to the ideal ratio [6], [8]. By using (2) and technology parameters the calculated sensitivity is S=0,026/T. According (1) the split-drain output current depends on the bias current. Typical bias current for the split-drain can be I_B=100μA, a reasonable compromise between sensitivity and power consumption, but other values can be chosen. Therefore, for this bias current and taking into account the F_C=590mT/A magnetic-field-to-coil-current ratio calculated by MAXWELL, the differential output current for the split-drain transistor magnetic sensor is approximately 1.5μA per 1A of coil current, or 1500nA/A. Obviously the coil can only carry a few milliamps of current, according the track width and process parameters. Excessive currents can speed up the electro migration effect.

IV. NOISE ANALYSIS

In order to evaluate the minimum coil-current sensed by the CMOS split-drain, the transistor noise should be investigated. It has been observed that the noise current spectral density measured differentially can be larger than the predicted one for the equivalent standard MOS transistor, i.e. same area and bias condition. This suggests that an excess-noise current generation is taking place thus affecting severely the sensor resolution. Moreover, split-drain noise measurements have shown that there is a negative correlation between drain noise currents. This observation was already mentioned in the literature [9], which includes thermal and 1/f noises. A new noise model was therefore developed aimed to explain this excess-noise current in thermal region [10]. The proposed noise model for the split-drain transistor is represented by noise current spectral densities equivalent sources, as indicated in Figure 4. Two of them model the longitudinal noise current (i_L) as in an ordinary transistor, each of them carrying half the total noise current, associated with the respective drain terminal. The third source models the transversal noise current (i_T) that flows between drains, bringing about the observed negative noise correlation. Being all noise sources thermal generated, they are assumed to be all uncorrelated.

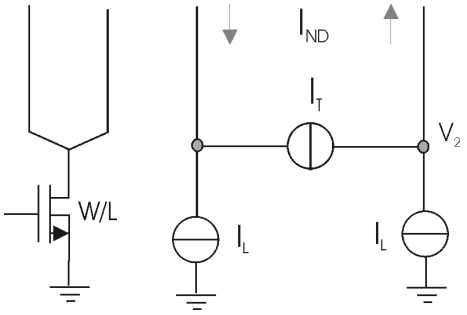


Fig. 4. Split-Drain Transistor Noise Model

The longitudinal and transversal noise currents (per √Hz base) are given in (4), whose parameters are K=1.381x10^{-23} [J/K], the Boltzmann constant, T the absolute temperature [K], μ the effective mobility, L and W the length and width of the split-drain transistor. The Q_I is the total transistor channel charge, and can be calculated using (5) for the split-drain transistor when operating in saturation under strong inversion.

$$i_L = \sqrt{\frac{2.K.T.\mu.Q_I}{L^2}} \qquad i_T = \sqrt{\frac{4.K.T.\mu.Q_I}{W^2}} \tag{4}$$

$$Q_I = \frac{2}{3}.W.L.C'_{OX}.(V_{GS} - V_T) \tag{5}$$

In (5), the new process parameter is C'$_{OX}$, the oxide capacitance per unit area. For the 0,35μm chosen CMOS process, C'$_{OX}$=4,54×10^{-3} F/m^2. The threshold voltage for N-MOS transistor in same technology is V_T=0,46V. Once the longitudinal and transversal currents are known, the differential noise current (i_{ND}) produced by the split-drain transistor can be evaluated. It is worth noting that as the split-drain output signal is differential mode, so is the resulting noise. Starting from the noise model depicted in Figure 4, the differential current spectral density (within 1Hz bandwidth) can be obtained and is given in (6).

$$i_{ND} = \sqrt{2.\left(i_L^{\,2} + 2.i_T^{\,2}\right)} \tag{6}$$

Combining (1) and (6) the minimum detectable magnetic field within 1Hz bandwidth above the 1/f region can be evaluated. Employing the 0,35μm CMOS process parameters and the chosen split-drain transistor (L=W=10μm), it results the graphic depicted in Figure 5. Taking into account the F_C=590mT/A factor, the minimum coil current is easily determined.

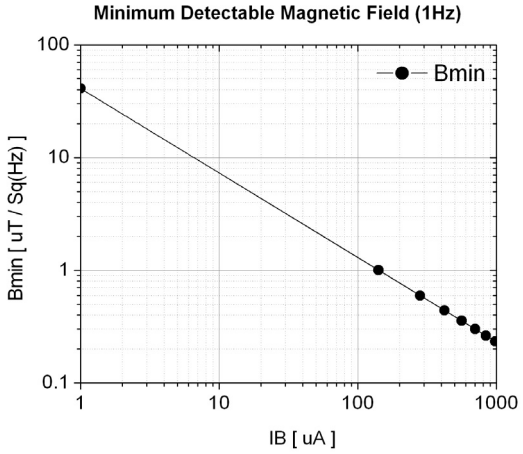


Fig. 5. Minimum detectable magnetic field for the 0,35μm CMOS L=W=10μm split-drain transistor as bias current function.

V. EXPERIMENTAL SETUP AND RESULTS

The implemented split-drain transistor was biased and the coil energized with a DC current in order to provide a magnetic field to be detected by the transistor. The semiconductor parameter analyzer HP4155 was used to test this basic configuration due to the equipment's sourcing features. In the test, the bias transistor was chosen I_B=115μA; and the coil current varied from 0 to 20mA, the coil current

conduction upper limit determined by its dimensions. According (1) and the coil factor (F_C=590mT/A), the output detected differential current for the maximum coil current is: $\Delta I=S\times I_B\times F_C\times I_{COIL}=0{,}026\times 115\mu\times 0{,}59\times 0{,}02=36\times 10^{-9}$A. This value is in good agreement with the experimental result obtained from HP4155 measurements as depicted in Figure 6. As observed, an approximately 2nA offset current is due to split-drain geometric mismatch and process variations. By using multiple devices in parallel this effect can be minimized. Taking this offset current into theoretical calculation, a better agreement to the measured data is achieved.

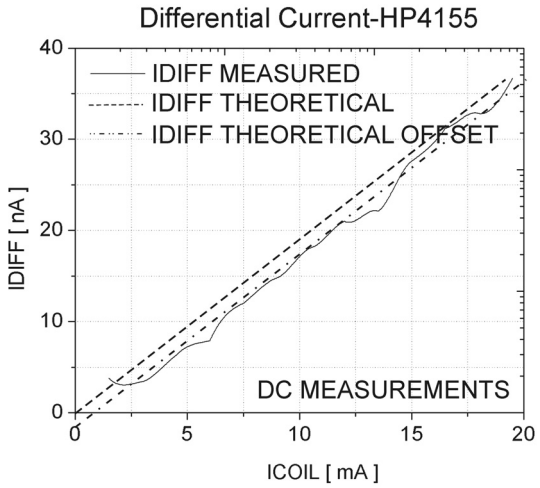


Fig. 6. Measured and theoretical Split-Drain output current as function of I_{COIL} for I_B=115μA.

Dynamic tests were also carried out. For this purpose, an additional instrumentation circuit was employed aiming a better visualization of the signals. In order to convert the differential output current into a differential voltage, a pair of matched low-noise resistors was used. Additionally, an instrumental amplifier was adjusted to provide a differential gain of G=50, as shown in Figure 7.

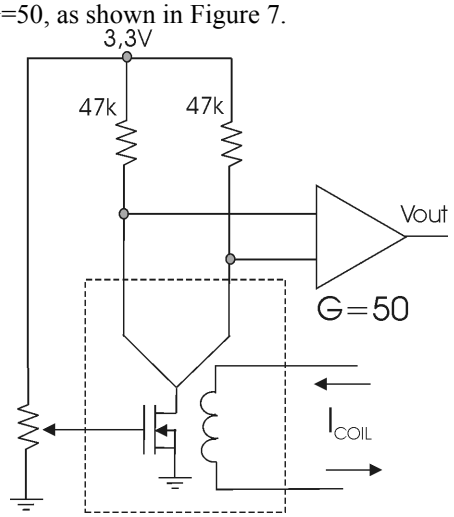


Fig. 7. Instrumental circuit associated to the basic configuration

As before, the split-drain transistor was I_B=115μA biased and 15mA current pulses were applied to the coil. In the amplifier output 62mV-pulses were obtained, according $V_{out}=R.\Delta I.G=47\times 10^3\times S\times I_B\times F_C\times I_{COIL}\times G=47\times 10^3\times 0{,}026\times 115\times 10^{-6}\times 0{,}59\times 0{,}015\times 50=62$mV. This value can be verified in Figure 8. The split-drain offset along with the resistor and amplifier ones affect severely the output voltage. In this case, for practical purposes, an offset correction should be employed by using auxiliary circuits. These preliminary experimental results have confirmed the predictions obtained from the calculated sensitivity analysis and from electromagnetic simulations as well.

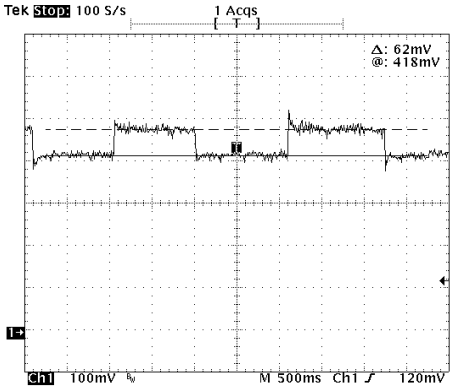


Fig. 8. Amplifier output for 15mA I_{COIL} pulses.

An AC test was performed to verify the steady-state functioning regime. A 3Hz-current coil I_{COIL}=2,5mA$_{RMS}$ was tested for same transistor bias conditions. Taking into account the current-to-voltage conversion gain, the output voltage will be $V_{out}=R.\Delta I.G=47\times 10^3\times S\times I_B\times F_C\times I_{COIL}\times G=47\times 10^3\times 0{,}026\times 115\times 10^{-6}\times 0{,}59\times 2{,}5\times 10^{-3}\times 50$ which gives V_{out} =10,3mV$_{RMS}$ or –39.6 dBV for the already mentioned parameters. Results are shown in Figure 9: Bottom trace: Applied current coil; Middle: FFT of the detected output voltage; Top: Time domain output voltage.

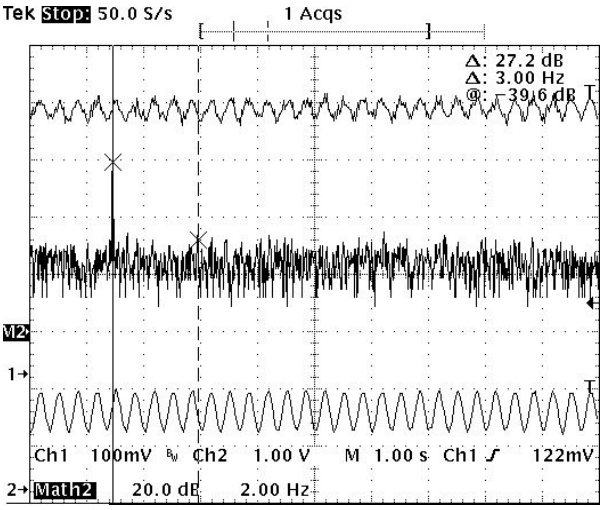


Fig. 9. 3Hz-2,5 mA$_{RMS}$ coil-current detection

Next, the split-drain transistor noise current is checked. To do so, a setup using two instrumental amplifiers whose gain is adjusted to 1900 (65,6dB) each one is used in conjunction with a two-channel signal analyzer HP3562A featuring cross-correlation algorithm, as shown in Figure 10(a). The cross-correlation technique eliminates the instrumental amplifier noise [10], [11] and gives the differential noise

voltage spectral density (√VPSD) whose value can be converted to current taking into account the 47kΩ I-V converter resistors. This procedure allows evaluating the measured differential noise current. The post-processed data can be checked out against the theoretical values predicted in (6). Thus, for the technology parameters and transistor bias current, the thermal noise spectral density along with the measured values within 1Hz bandwidth are given in Figure 10(b).

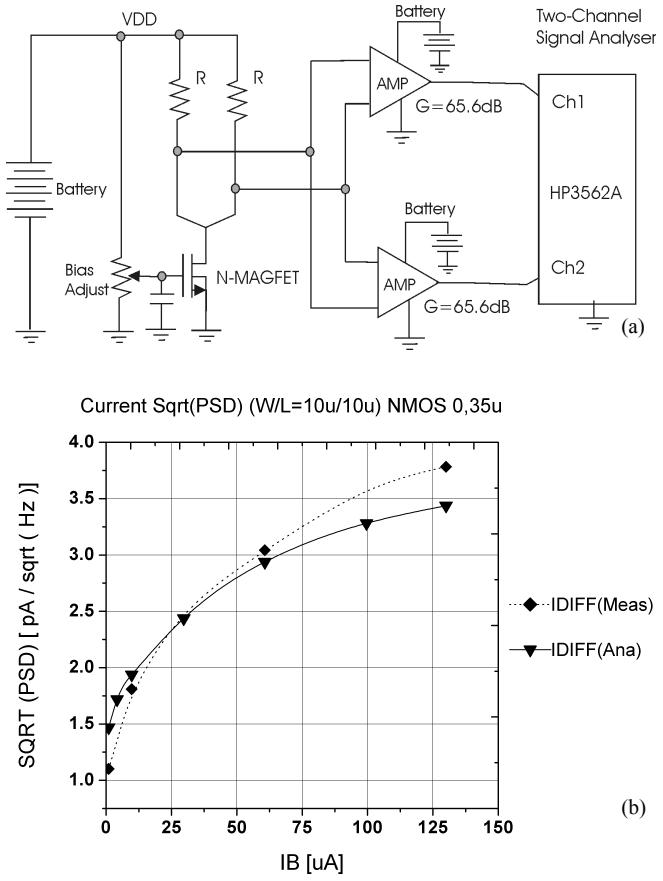


Fig. 10. (a) Setup for Noise Measurements. (b) Measured and theoretical differential noise current spectral density.

Figure 11 shows a typical HP3562A signal analyzer noise measurement within the 25kHz-75kHz range. Top trace shows the differential voltage PSD taken between drains using the 47kΩ I-V converter resistors. This value can be converted into the split-drain differential noise current as commented before; taking into account the amplifier gain and the resistors values. Bottom trace shows the measured correlation between drain noise voltages. The amplifier roll-off is responsible for the negative slope of the voltage PSD within the chosen range. However, knowing exactly the amplifier gain at the frequency test, this effect can be compensated and the noise calculations performed correctly. The low frequency noise range (1/f) was not tested because up to the best of authors' knowledge there is no available model to verify the split-drain differential 1/f noise level. Further studies aiming this topic are under development.

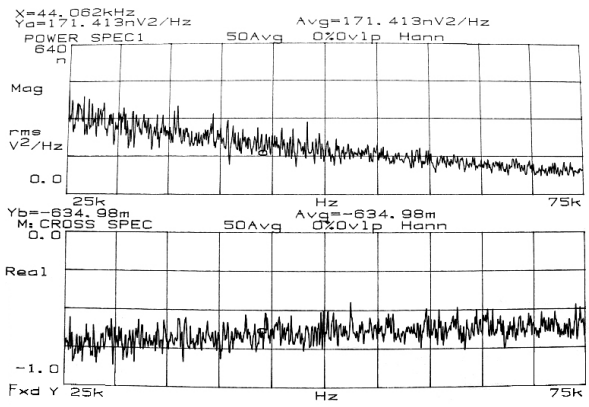


Fig. 11. HP3562 Noise Measurements

A frequency response was performed aiming to verify the sensor usefulness at frequencies other than the lower range (DC to Hz). The HP3577 network analyzer and a simple mirror employed to convert differential output current into voltage were used to perform such a task, as illustrated in Figure 12(a). An additional 47kΩ resistor produces the output voltage to be read by the network analyzer whereas a variable DC voltage adjusts the output voltage offset. The HP3577 sourcing features allows a variable-frequency current to be applied to the coil. As can be observed in Figure 12(b), due to coupling effects, the output voltage increases with the frequency. This effect limits the sensor operation at frequencies lower than 200Hz.

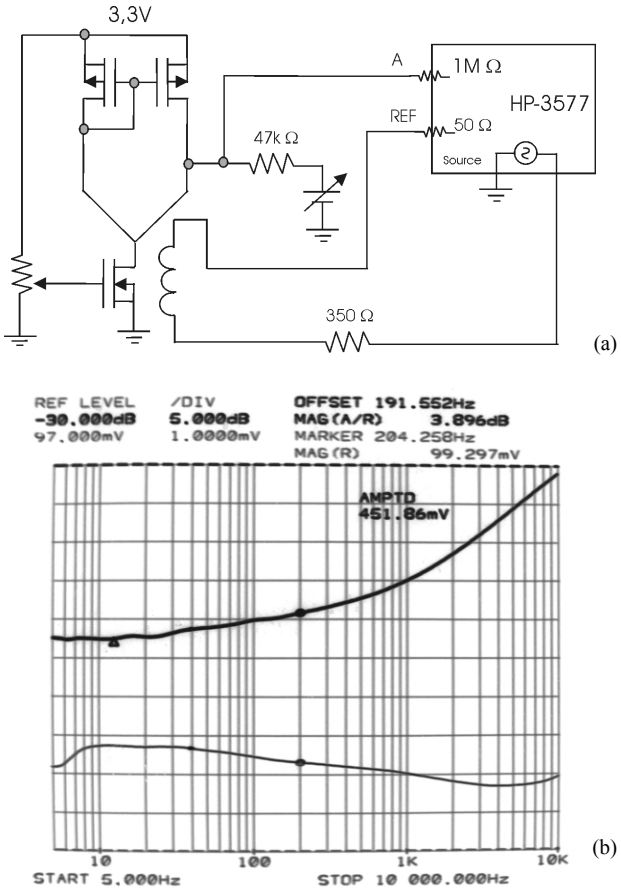


Fig. 12. (a) Setup for Frequency Measurements. (b) Measured frequency response.

VI. CONCLUSIONS

A current sensing technique showing galvanic isolation to be implemented within integrated circuits is devised. The sensor is based on the MOS Split-Drain transistor that can detect magnetic fields and show very linear response to the applied field. A current that is carried through an integrated metal coil generates the magnetic field. This coil is placed atop the split-drain transistor allowing a detection ratio of 1500nA/A differential output current per sensed current. The process-based silicon dioxide layer that isolates the coil can bear several hundred volts so high voltage and current can be measured off-chip. For higher current levels, a shunt resistor can be used in order to alleviate the electro migration effect. The noise analysis, based on a new noise model for the split-drain transistor, was necessary to evaluate the minimum detectable coil current. This work has shown that this approach can be conveniently used in several integrated current sensing applications as the ones applied in industry, research and development areas.

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