A HIGH FREQUENCY TRANSFORMER ISOLATION UPS SYSTEM WITH 110V/220V INPUT VOLTAGE

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***Abstract* – This work proposes an isolated double conversion UPS with power factor correction using a high frequency transformer, and input voltages equal to 110V/220V. The arrangement is suitable to rack structures because it has small size and reduced weight. For both input voltages, the proposed converter has almost the same efficiency processing the same output power. Other relevant features are soft commutation of the controlled switches in the chopper and the boost stage, simple control strategy that can be implemented with well-known integrated circuits, and the use of few batteries in series due to the step-up stage. Qualitative analysis and experimental results obtained from 2kVA laboratory prototype are presented.**

***Keywords* – high frequency transformer, double conversion UPS system, power factor correction, soft commutation.**

I. INTRODUCTION

Nowadays uninterruptible power systems (UPS) are used to protect sensitive loads against a wide variety of utility voltage disturbances and power outages. Most of such systems consist in the double conversion UPS configuration that operates normally with a low frequency transformer using a silicon-steel core. Such transformer is placed at the input or output depending on the topology arrangement. The addition of such magnetic component increases both weight and volume, and also adds cost and difficulties in the transportation to the installation site.

During the 1990's, the evolution of semiconductors (i.e. diodes and transistors) and other components have allowed the development of devices with nearly-ideal characteristics, making research on UPS systems with high frequency transformers possible [1]-[6].

Several UPS topologies have been proposed in the literature so far, and some of them are discussed briefly as follows.

The UPS scheme shown in figure 1 was studied in [1] [2]. It consists of a power factor correction (PFC) current-fed full-bridge converter and a voltage source full-bridge inverter. In this circuit, hard commutation of the controlled switches compromises efficiency and several batteries placed in series are necessary to achieve high DC-link voltage. Additionally, the current drawn by the battery bank is pulsed affecting the reliability of the battery bank.

The UPS shown in figure 2 was studied in [3]. The circuit is composed by a modified PFC current-fed full-bridge structure and a voltage source full-bridge inverter, similar to the previous one. This topology has the advantages of reduced amount of semiconductors in series during power transfer, implying the reduction of conduction losses and improving efficiency. The disadvantages are hard commutation of the controlled switches, and many batteries in series are necessary to achieve high DC-link voltage in order to supply the voltage source inverter.

Figure 3 shows the series-parallel resonant system proposed in [4], with galvanic isolation between the input side, the output side, and the battery. This system has the advantages of power factor correction, single preregulator stage, soft commutation of the controlled switches, and few batteries in series. On the other hand, the disadvantages are the complex control strategy and the adjustment of resonant parameters.

The two-stage UPS studied in [5] is shown in figure 4. The first stage consists of a PFC-DCM flyback converter with integrated battery charger, and the second stage is a boost inverter. Due to the operation of the flyback converter in discontinuous conduction mode, the system is only suitable for low power applications i.e. below 500W.

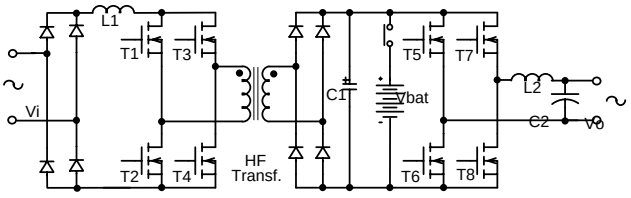

Fig. 1. Single-phase UPS proposed in [1] [2].

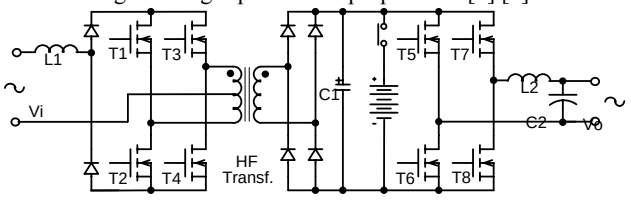

Fig. 2. Single-phase UPS proposed in [3].

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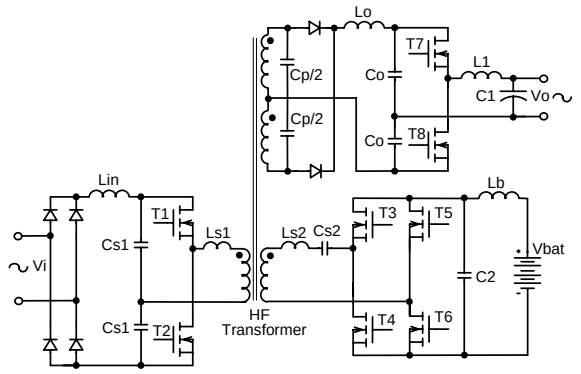


Fig. 3. Single-phase UPS proposed in [4].

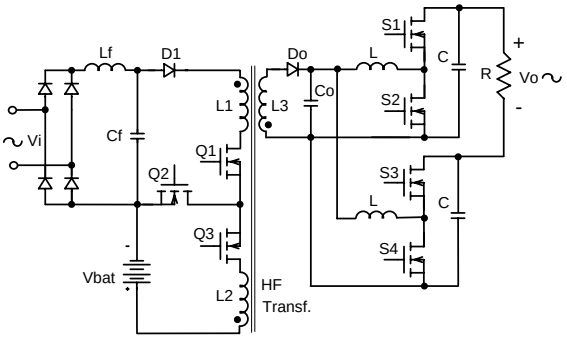


Fig. 4. Single-phase UPS proposed in [5].

Figure 5 shows the detailed diagram of the UPS reported in [6]. The circuit consists basically of a ZCS-PSRC (Zero Current Switching – Partial Series Resonant Converter) DC-DC converter, a dynamic power compensator given by a bi-directional converter, and a voltage source full-bridge inverter. Advantages of the circuit are power factor correction, soft commutation of the switches in the input stage, and the inverter switches operating at 50Hz. The main disadvantage lies in the need of several batteries in series to achieve the adequate DC link voltage when the battery bank supplies the load, since the bidirectional converter operation is analogous to a buck topology.

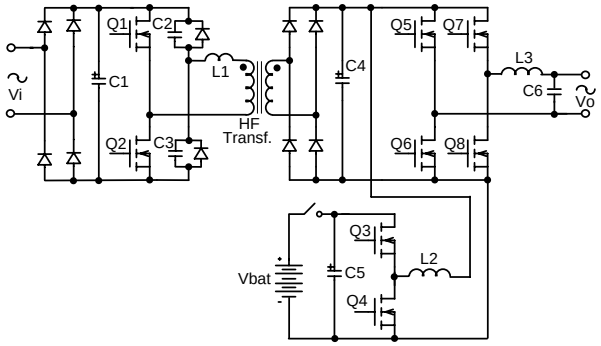


Fig. 5. Single-phase UPS proposed in [6].

Some other works involving isolated preregulators were presented in national conferences [7] [8], and can be used as the input stage of UPS's.

However, the aforementioned UPS topologies have some disadvantages that were discussed. Therefore such topologies can not be employed in the development of a high power UPS i.e. where the output power is greater than 1000W. To satisfy the requirements of single-phase voltages equal to 110V/220V found in Brazil, a flexible UPS system shown in figure 6 is proposed. It operates with two input voltage levels without compromising the global efficiency. The stages are controlled using well-known conventional PWM control techniques, allowing the use of low cost commercial integrated circuits. The preregulator topology, composed by chopper and boost stages, presents soft commutation of the switches, and few batteries in series are needed due to eventual voltage unbalance across them when several units are connected in series. Other features such as isolation and power factor correction are the former advantages of the aforementioned systems.

The operation with two input voltage levels, the cascaded operation of the chopper and the boost stage, and the possibility of achieving soft commutation of the chopper switches using coupled inductors were achieved in [3] [10] [11] [12] [13].

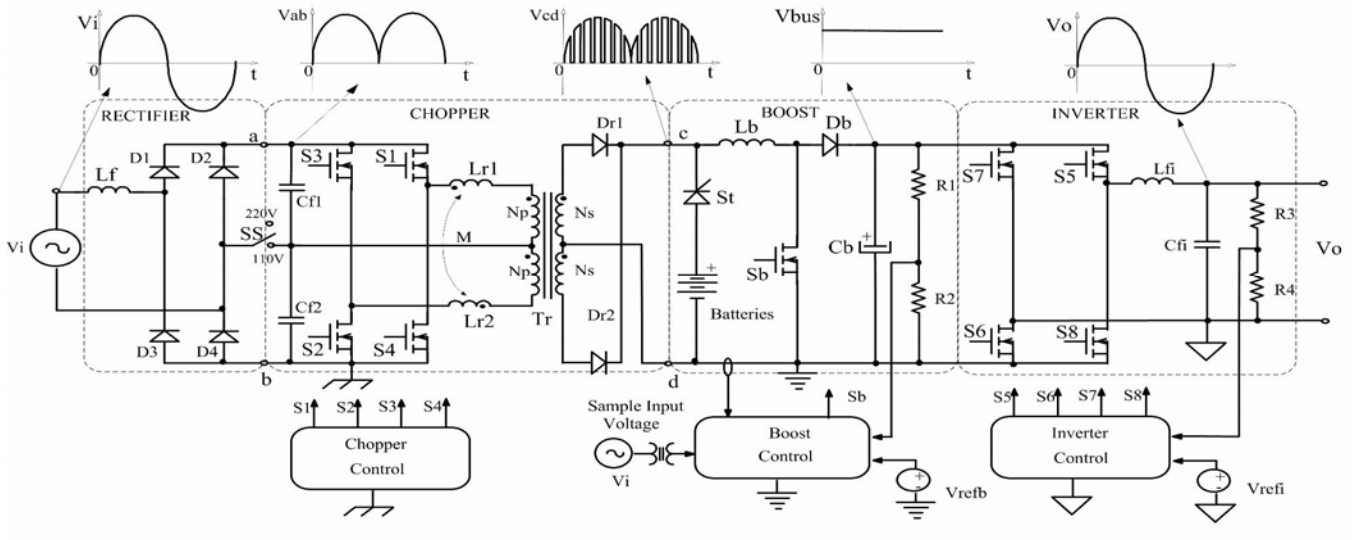


Fig. 6. Proposed single-phase isolated UPS with high frequency transformer.

II. DESCRIPTION OF THE PROPOSED UPS CIRCUIT

The proposed UPS is shown in figure 6. It is composed by the following parts: a full-bridge rectifier formed by diodes D_1-D_4; a full-bridge chopper formed by controlled switches S_1-S_4, high frequency transformer T_r, coupled inductors L_{r1}-L_{r2}, and rectifier diodes D_{r1}-$D_{r2;}$ a traditional boost converter formed by inductor L_b, switch S_b, diode D_b, and capacitor C_b; a full-bridge inverter formed by controlled switches S_5-S_8, inductor L_{fi}, and capacitor C_{fi}; and a high frequency input filter formed by inductor L_f and capacitors C_{f1} and C_{f2}.

III. ANALYSIS OF THE CHOPPER OPERATION WITH INPUT VOLTAGE EQUAL TO 110V

A. Principle of Operation

The chopper operates with fixed duty cycle ($D \cong 0.5$) using IC UC3525A. The control strategy allows the application of high frequency voltage pulses to the primary windings of transformer T_r, enabling the use of a high frequency transformer.

When the input voltage is 110V, the selector switch *SS* (manual or automatic) must be turned on and adjusted to the 110V position point. Under this condition, diodes D_2 and D_4 are always reverse biased.

Considering the positive semicycle of the input voltage, during half of the switching period, the converter operation can be resumed to four stages, as shown in figure 7, as the relevant waveforms are depicted in figure 8. The operation of the topology in the negative semicycle is analogous.

Interval (t_0-t_1): At $t=t_0$, switches S_1 and S_2 are turned on. The input voltage charges inductor L_{r1}, and the current increases linearly from zero to nI_{Lb}. The output current I_{Lb} is freewheeling.

Interval (t_1-t_2): During this interval, energy is transferred from the input source V_i to the load, represented by current source I_{Lb}.

Interval (t_2-t_3): At $t=t_2$, switches S_1 and S_2 are turned off under zero voltage condition due to the intrinsic capacitances. Half of the energy stored in inductor L_{r1} is transferred to inductor L_{r2}. The intrinsic capacitances are then charged and discharged.

Interval (t_3-t_4): When the voltages across switches S_1 and S_2 is equal V_i, the antiparallel diodes of switches S_3 and S_4 are directly biased. During this interval, switches S_3 and S_4 must be turned on.

When the input voltage is 110V, the input current is twice that in 220V, so that the same output power is maintained. As one can see in figure 7, only one controlled switch of the chopper is involved during the energy transfer, and consequently conduction losses are reduced.

In the chopper stage, duty cycle reduction ΔD occurs due to the input voltage across commutation inductors L_{r1} and L_{r2}, and also to the transformer leakage inductances, which cause the linear variation of the current through them. During this interval, output current I_{Lb} is freewheeling through rectifier diodes D_{r1} and D_{r2}. Therefore, there is no power transfer from the input to the load. The duty cycle reduction can be obtained from the inductor voltage given by (1).

$$v_L = L\frac{\Delta i_L}{\Delta t}, \tag{1}$$

as the involved parameters are:

$$v_L = \left|V_{i(pk)_{110V}} \sin(\theta)\right|, \tag{2}$$

$$\Delta i_L = \left|2nIL_{b(pk)} \sin(\theta)\right|, \tag{3}$$

$$\Delta t = \Delta D T_s, \tag{4}$$

$$L = L_{r1} = L_{r2}. \tag{5}$$

where n is the transformer turns ratio, $IL_{b(pk)}$ is the peak current through the boost inductor, $V_{i(pk)}$ is the peak input voltage, $\theta=\omega t$ is the phase angle of the input voltage, and T_s is the switching period.

Substituting (2), (3), (4), and (5) in (1), expression (6) results.

$$\Delta D = \frac{2L_{r1} f_s n IL_{b(pk)} \sin(\theta)}{V_{i(pk)_{110V}} \sin(\theta)}, \tag{6}$$

where f_s is the switching frequency.

The rms output voltage of the chopper, which supplies the boost converter, is given by:

$$V_{cd(rms)} = \sqrt{\frac{1}{\pi}\int_0^{\pi} 2\left(D-\Delta D\right)\left(nV_{i(pk)_{110V}} \sin(\theta)\right)^2 d\theta}. \tag{7}$$

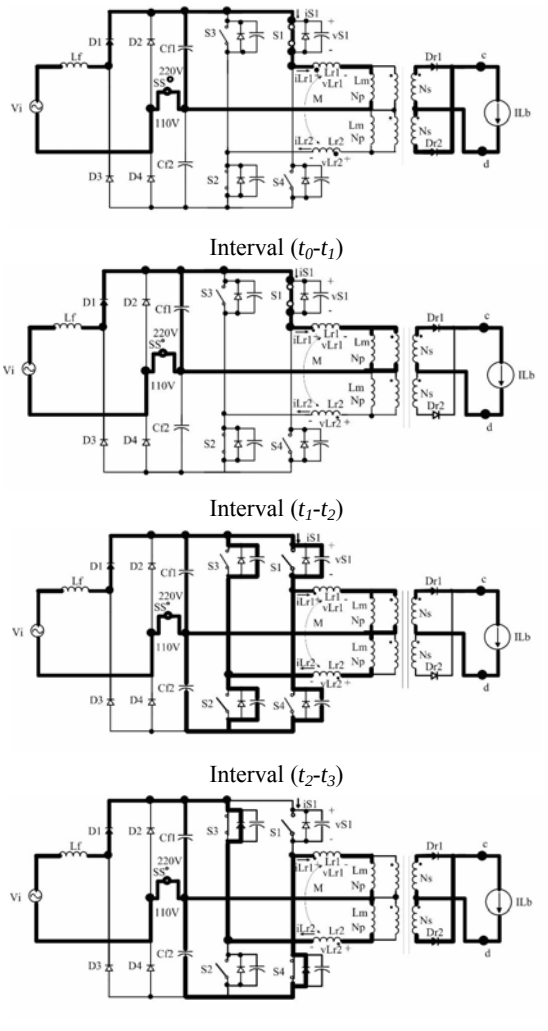


Fig. 7. Operating stages of the chopper circuit when the input voltage is 110V.

Simplifying (7) yields:

$$V_{cd(rms)} = nV_{i(pk)_{110V}}\sqrt{(D-\Delta D)}\,, \tag{8}$$

where $V_{cd(rms)}$ is the chopper rms output voltage, and D is the duty cycle. The inductor peak current is calculated with:

$$I_{Lb(pk)} \cong \frac{\sqrt{2}P_o}{V_{cd(rms)}}\,, \tag{9}$$

where P_o is the UPS active output power.

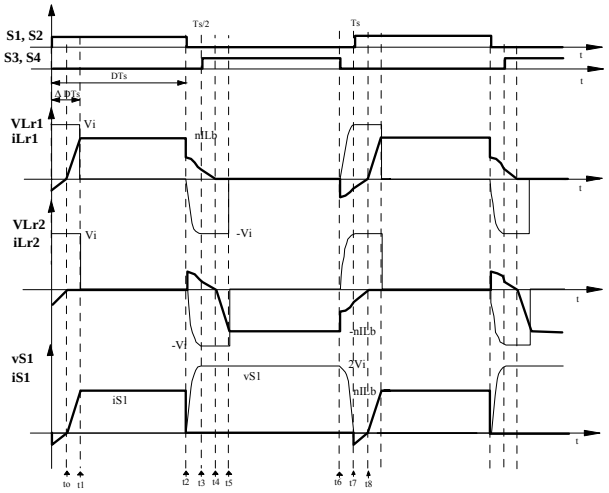


Fig. 8. Main theoretical waveforms when the input voltage is 110V.

IV. ANALYSIS OF THE CHOPPER OPERATION WITH INPUT VOLTAGE EQUAL TO 220V

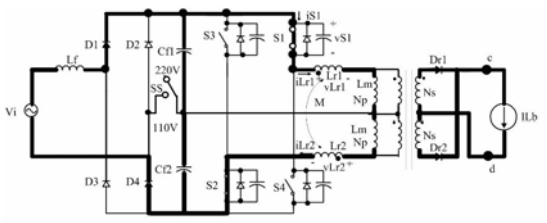
A. Principle of Operation

In this mode, the selector switch *SS* must be set to the 220V position. The control strategy is the same one used when the input voltage is 110V.

Considering the positive semicycle of the input voltage, during half of the switching period, the converter operation can be represented by four stages, as shown in figure 9, where the theoretical waveforms are presented in figure 10. The description of the operation is similar to the case where the input voltage is 110V.

Although the current flows simultaneously through both inductors when the chopper operates with 220V, the equivalent inductance, considering the mutual inductance and coupling coefficient nearly unity, is equal to four times L_{r1} or L_{r2} i.e. $L_{req} = 4L_{r1} = 4L_{r2}$.

According to figure 9, there are always two controlled semiconductors involved in the power transfer. Even though the input voltage is twice 110V, the current through the semiconductors is reduced to a half. Therefore, losses are approximately equal when the converter operates with 110V.



Interval (t_0-t_1)

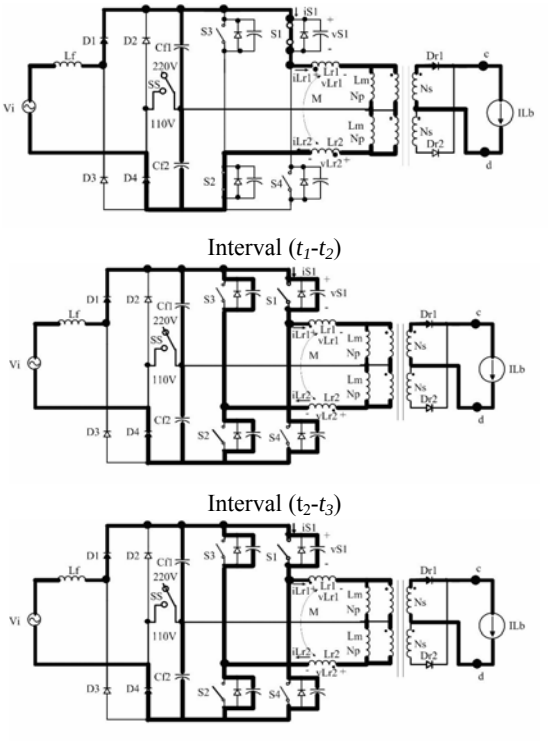


Fig. 9. Operating stages of the chopper circuit when the input voltage is 220V.

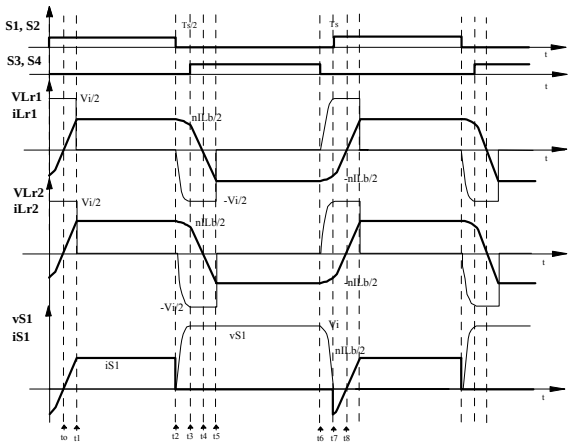


Fig. 10. Main theoretical waveforms when the input voltage is 220V.

V. BOOST CONVERTER

A classical boost converter shown in figure 11 is connected to the chopper. It is responsible for the output voltage regulation, power factor correction, and stepping the battery voltage up to the output voltage V_{bus}. Additionally, this stage provides an active filtering to block the pulsating current of the nonlinear load (i.e. the inverter stage) from the battery bank. Switch S_b operates with zero voltage switching in a wide range of output power using a passive nondissipative snubber circuit [12].

The boost converter is controlled using conventional average current mode control implemented with the well-known PWM IC UC3854 [9].

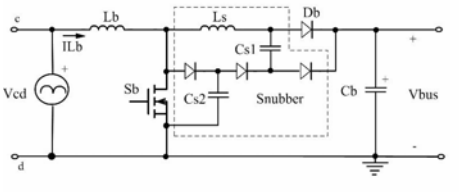


Fig. 11. Boost stage.

VI. BATTERY CHARGER

The battery charger is based on a small nonisolated buck converter, as shown in figure 12. The converter operates in continuous conduction mode (CCM) of the current through the filter inductor, and is supplied by the boost converter.

As the voltage across terminals *c* and *d* is chopped at 50kHz and the ripple frequency is 120Hz, as shown in figure 6, a controlled switch S_t is necessary. For this application, a thyristor associated with a passive snubber was used. Switch S_t is turned on when the AC mains voltage is null or out of the input voltage range, and it is turned off when AC mains voltage is within the desired limits. The gating signal is turned off during normal operation, it is reverse biased naturally when V_{cd} voltage is higher than battery bank voltage.

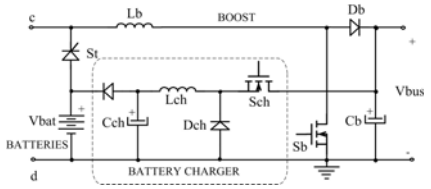


Fig. 12. Battery charger schematic.

VII. INVERTER STAGE

A classical voltage source full-bridge inverter is connected to the output of the boost stage, so that the DC bus voltage in AC output voltage can supply the load. In order to control the output voltage, sinusoidal PWM technique with unipolar voltage switching was applied. The inverter switches present hard commutation. To protect the switches against overvoltage, a RCD clamping snubber circuit was placed in each inverter leg.

VIII. SIMPLIFIED DESIGN EXAMPLE

A. Preliminary Specifications

The design specifications of the proposed UPS system are shown in Table I. The switching frequency for the all stages is assumed f_s=50kHz.

TABLE I
UPS specifications

Mains input voltage	V_i = 110Vac / 220Vac
AC mains frequency	f_r = 60Hz
Output voltage	V_o = 110Vac
Maximum active output power	P_o = 1400W
Maximum apparent output power	S_o = 2kVA
Output frequency	f_o = 60Hz

The design parameters of the UPS stages are listed in Table II.

TABLE II
Design parameters of the UPS stages

• Chopper Circuit	
Transformer turns ratio	$n = N_p/N_s = 1$
Maximum duty cycle	$D_{\max} = 0.48$
Maximum duty cycle reduction	$\Delta D_{\max} = 0.048$
• Boost Circuit	
Boost inductor current ripple	$\Delta IL_{b\max} = 0.15 IL_{b(pk)}$
DC-link output voltage	$V_{bus} = 220\text{V}$
Hold-up time	$\Delta t = 8.333 \cdot 10^{-3}\text{s}$
Minimum DC link output voltage	$V_1 = 190\text{V}$
• Battery Charger Circuit	
Maximum battery voltage	$V_{bat} = 108\text{V}$
Maximum battery charge current	$I_{ch} = 1\text{A}$
Current ripple through the filter inductor	$\Delta I_{ch} = 0.1\text{A}$
Duty cycle of the buck converter	$D_{ch} = 0.49$
Voltage ripple across battery bus	$\Delta V_{bat} = 0.2\text{V}$
• Inverter Circuit	
Modulation index	$ma = 0.71$
Filter inductor ripple current	$\Delta IL_{fi} = 2.7\text{A}$

B. Design Procedure of the Chopper Circuit

The rms output voltage of the chopper is calculated using (8).

$$V_{cd(rms)} = 1 \cdot \sqrt{2} \cdot 110 \cdot \sqrt{(0.48 - 0.048)} = 102.25\text{V}$$

The peak output current of the chopper is determined using (9).

$$IL_{b(pk)} \cong \frac{\sqrt{2} \cdot 1600}{102.25} \cong 19.36\text{A}$$

The maximum duty cycle reduction occurs when the voltage angle is $\theta = \pi/2$. Therefore, the inductance is obtained from (6) as:

$$L_{r1} = L_{r2} = \frac{V_{i(pk)_{110V}} \Delta D_{\max}}{2 f_s n IL_{b(pk)}}. \qquad (10)$$

Substituting the relevant parameters in (10), the inductances are given by:

$$L_{r1} = L_{r2} = \frac{\sqrt{2} \cdot 110 \cdot 0.048}{2 \cdot 50000 \cdot 1 \cdot 19.36} = 3.85\mu\text{H}.$$

The input filter capacitances must be small, and arbitrarily chosen as $C_{f1} = C_{f2} = 6.6\mu\text{F}$, given for the connection of three paralleled polyester capacitors . The frequency of the chopper input current is twice the switching frequency. Thus, using LC filter criterion given in [14] i.e. $f_f \le 2 f_s/10$, the filter inductance is:

$$L_f = \frac{1}{C_{f(eq)} \left(0.94 f_s\right)^2} \cong 137.18\mu\text{H}. \qquad (11)$$

C. Design Procedure of the Boost Converter

The boost inductance and filter capacitance are obtained according to [9].

$$L_b = \frac{\sqrt{2}V_{cd(rms)}D_{boost}}{f_s \Delta IL_{b\max}} = 338.60\mu\text{H}\,, \tag{12}$$

$$C_b = \frac{2P_o\Delta t}{V_{bus}{}^2 - V_1^2} = 2167.9\mu\text{F}\,, \tag{13}$$

where:

$$D_{boost} = 1 - \frac{\sqrt{2}V_{cd(rms)}}{V_{bus}} = 0.34\,. \tag{14}$$

D. Design Procedure of the Battery Charger

The filter inductance is obtained substituting the design parameters in (15),

$$L_{ch} = \frac{V_{bat}(1-D_{ch})}{f_s \Delta I_{ch}} = 11.01\text{mH}\cdot \tag{15}$$

The filter capacitance and equivalent series resistance are calculated as follows:

$$C_{ch} = \frac{\Delta I_{ch}}{8 f_s \Delta V_{bat}} = 1.25\mu\text{F}\,, \tag{16}$$

$$R_{se} \le \frac{\Delta V_{bat}}{\Delta I_{ch}} \le 2\Omega\cdot \tag{17}$$

The prototype was implemented using an electrolytic capacitor rated at 100μF/250V.

E. Design Procedure of the Voltage Source Inverter

The filter inductance is obtained from the inductor voltage equation, which is similar to (1). The design considers purely resistive load, and the angle of the fundamental input voltage across the LC filter is θ=ωt=π/2. Substituting the design parameters in (18) gives:

$$L_{fi} \cong \frac{\left(V_{bus} - \sqrt{2}V_o\right)ma}{2 f_s \Delta IL_{fi}} = 170\mu\text{H}\,. \tag{18}$$

The resonance frequency of the output LC filter applying unipolar voltage switching technique is given by expression (19) [14],

$$f_{fi} \le \frac{2f_s}{10} = \frac{1}{2\pi\sqrt{L_{fi}C_{fi}}}\,. \tag{19}$$

The inverter output filter capacitance must be greater than C_{fi}≥1.49μF. The prototype was implemented with a metalized polypropylene capacitor rated at 30μF/250V.

IX. EXPERIMENTAL RESULTS

In order to verify the feasibility and performance of the proposed UPS system, assembled with the parameters obtained in the section XIII (shown in Tables III, IV and V), a laboratory prototype was implemented and evaluated.

TABLE III
Parameters of the Chopper Stage

Rectifier Diodes	GBPC3508A
Input Filter Inductor	L_f = 137.18μH
Input Filter Pilyester Capacitors	$C_{f1} = C_{f2}$ = 3×2.2μF/400Vdc
Switches S_1–S_4	IXFX44N60
Coupled Inductors	$L_{r1} = L_{r2}$ = 3.9μH
High Frequency Transformer	NEE-65/39 (Thornton Ipec) *Np*=12 turns; *Ns*=12turns
Diodes D_{r1} and D_{r2}	HFA30PA60C

TABLE IV
Parameters of the Boost Stage

Boost Inductor	L_b = 338.60μH
Output Electrolytic Capacitors	C_o = 3×680μF/450V
Diode D_b	HFA25PB60
Switch S_b	IXFX44N60
Resonant Inductors	L_S = 0.9μH
Polypropylene Film Capacitors	C_{S1} = 120nF C_{S2} = 6.8nF
Diodes D_{a1}, D_{a2} and D_{a3}	MUR460

TABLE V
Parameters of the Inverter Stage

Output Filter Inductor	L_{fi} = 170μH
Output Filter Polyprop. Capacitor	C_{fi} = 30μF
Switches S_5 - S_8	IXFX44N60

The experimental results consist of relevant voltage and current waveforms, and also efficiency and power factor curves.

A. Input Voltage Equal to 110V

Figure 13 shows the input voltage and input current waveforms, as high power factor is observed. Figure 14 shows the voltage and the current waveforms regarding switch S_1, where soft commutation details can be seen. The output voltages and currents of the inverter are shown in figures 15 and 16, where a high quality sinusoidal voltage waveform results, independently of the load characteristic. Figure 17 represents the efficiency curve as a function of output power. Finally, figure 18 depicts the power factor behavior as a function of the output power.

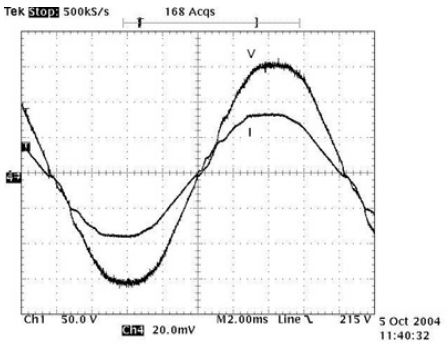


Fig. 13. Mains input voltage and current.
(50V/div.; 10 A/div.; 2ms/div.)

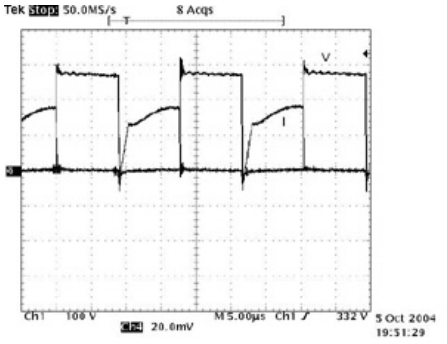


Fig. 14. Voltage and current of the chopper switch S_1.
(100V/div.; 10 A/div.; 5us/div.)

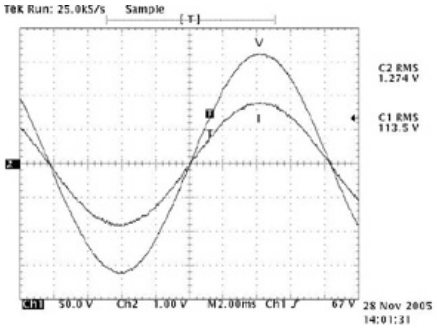


Fig. 15. Output voltage and current of the inverter for linear load.
(50V/div., 10A/div.; 2ms/div.)

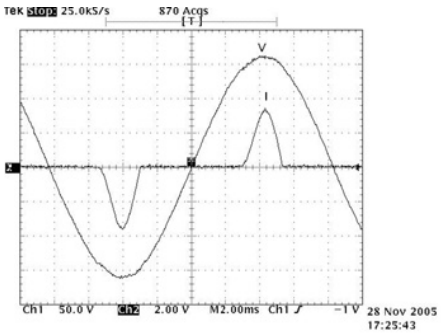


Fig. 16. Output voltage and current of the inverter for nonlinear load.
(50V/div., 20A/div.; 2ms/div.)

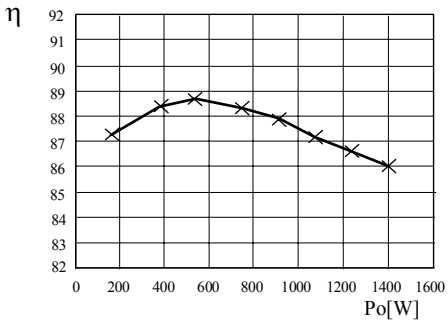


Fig. 17. Efficiency of the UPS system as a function of the output power.

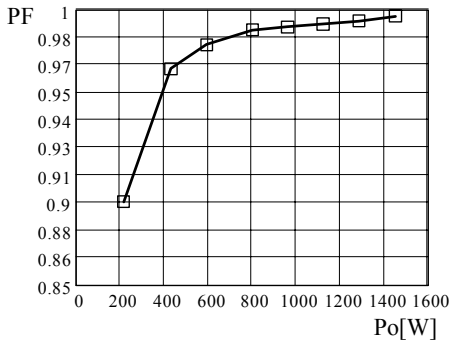


Fig. 18. Power factor as a function of the output power.

B. Input Voltage Equal to 220V

The corresponding waveforms for 220V input voltage are shown from figures 19 to 24. The analysis of the waveforms and curves is similar to the case when the input voltage is 110V.

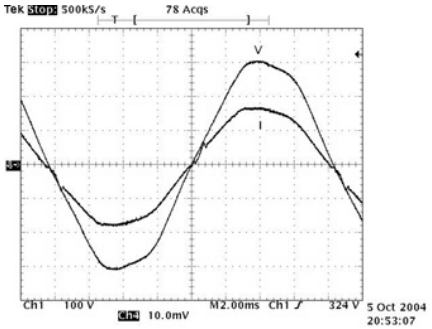


Fig. 19. Mains input voltage and current.
(100V/div.; 5 A/div.; 2ms/div.)

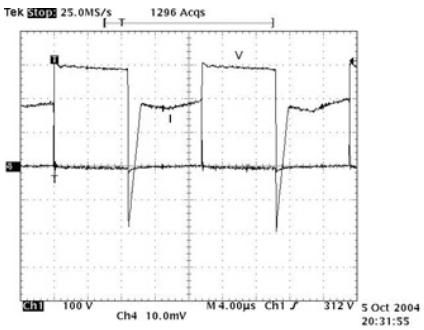


Fig. 20. Voltage and current of the chopper switch S_1.
(100V/div.; 5 A/div.; 4us/div.)

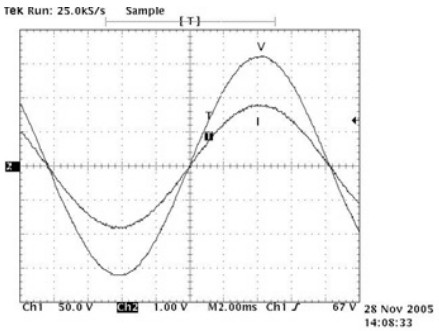


Fig. 21. Output voltage and current of the invert for linear load.
(50V/div.; 10 A/div.; 2ms/div.)

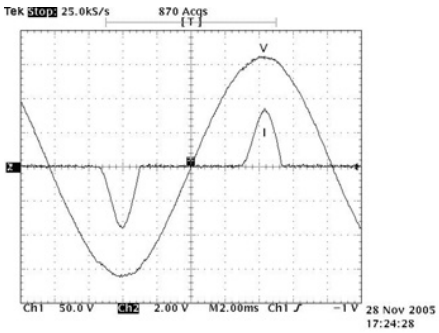


Fig. 22. Output voltage and current of the inverter for non-linear load.
(50V/div., 20A/div.; 2ms/div.)

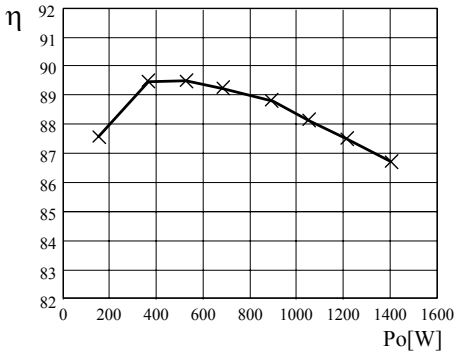


Fig. 23. Efficiency of the UPS system as a function of the output power.

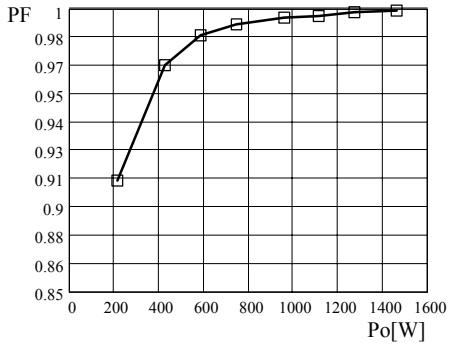


Fig. 24. Power factor as a function of the output power.

X. CONCLUSIONS

This paper has proposed a double conversion UPS, which is able to operate with rms input voltages equal to 110V-220V, 115V-230V, or 120V-240V. The qualitative analysis for the input voltage equal to 110V-220V, a simple design example, and experimental results obtained from 2kVA prototype have been presented.

As shown in figures 13 and 19, the system presents power factor correction. This characteristic is due to the boost stage, which is controlled using the well-known average current mode control. The maximum power factor obtained at full-load is shown in figures 18 and 24.

The chopper stage converts the continuous input voltage to high frequency AC voltage, so that the use of a high frequency transformer is possible. The chopper switches have soft commutation as shown in figures 14 and 20. Therefore commutation losses are reduced.

The inverter stage presents sinusoidal output voltage when supplying linear or nonlinear loads, according to figures 15, 16, 21 and 22. Hard commutation of the switches is verified. To limit the voltage overshoot across the switches, simple RCD snubbers were used. For this application, passive and active nondissipative snubbers are not adequate due to the complexity.

The global efficiency at full load is 86% for 110V, and 86.5% for 220V, as shown in figures 17 and 23.

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