AC-TO-AC CONVERTERS WITH HIGH INPUT POWER FACTOR AND VARIABLE OUTPUT FREQUENCY WITHOUT ANY FEEDBACK CONTROL

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***Abstract* – The main goal of this paper is to propose three single-phase AC-to-AC converters based on the AC-DC Nabae converter. The proposed topologies improve input power factor and input current waveform without any complicated switching modulation, such as pulse width modulation, or feedback control. These topologies can operate with either variable output frequency in applications such as AC drive systems or fixed output frequency such as UPS (Uninterrupted Power Supply). The main characteristics of the proposed configurations are also presented. Experimental results verify the theoretical studies.**

***Keywords* – Power factor control, AC-to-AC converter, Single-phase to single-phase converter.**

I. INTRODUCTION

In many applications a single-phase input voltage source type feeds a single-phase load. Single-phase AC-to-AC conversion usually employs full-bridge topologies, which implies in eight power switches. In general, the use of a large number of power switches increases the cost and reduces the reliability of the power conversion system. Thus, the study of topologies with a reduced number of power switches constitutes an important topic in power electronics [1], [2], [3], [4], [5], [6], [7], [8], [9], [10].

The usual alternative to reduce the number of power switches is the converter with four power switches and a capacitor DC-link midpoint connection [11]. However, it has half voltage capability in comparison with the full-bridge eight switch converter. Other possibility for reducing the number of power switches is obtained via configurations in which the input and output converters are connected by a shared-leg [12]. All these configurations utilize a complicated control strategy for obtaining a high power factor and need measuring of the voltage and current.

On the other hand, the power factor correction based on the boost converter is the most popular technique to achieve unity power factor [13], [14], [15]. Its operation in Discontinuous – Inductor – Current Mode (DCM) is popular at low to moderate power level. The input current of this converter automatically follows the sinusoidal line voltage so that, the current control loop can be removed, the whole

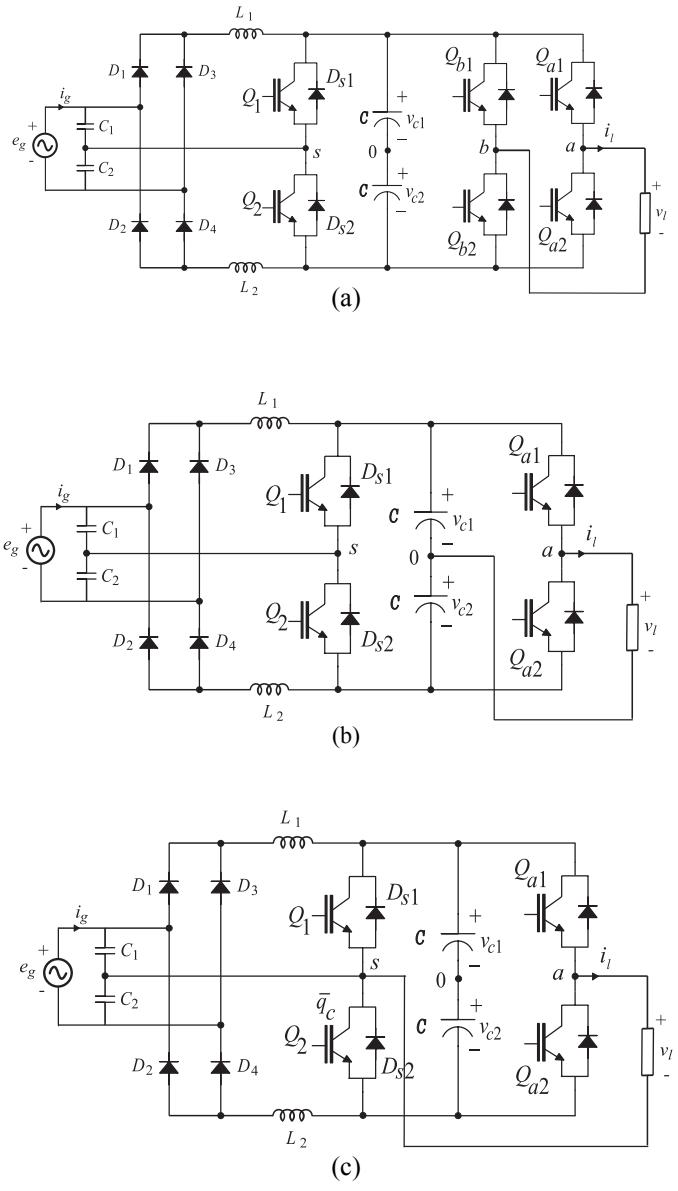

Fig. 1. AC-to-AC converters with independent output frequency and using Nabae's converter to provide power factor control: (a) Configuration 3*L*, (b) Configuration 2L_c and (c) Configuration 2L_s.

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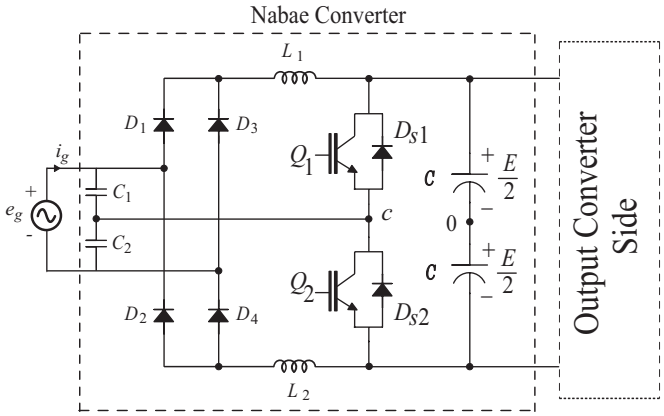


Fig. 2. Nabae Converter.

TABLE I
Comparison between Nabae and Full-Bridge Converter

	Nabae	Full-Bridge
Switches	2	4
Diodes	4	0
Inductors	2	1
Voltage Sensor	0	1
Current Sensor	0	1
Feedback Control	no	yes

control loop being simplified. However, DCM boost PFC is seldom adopted in the industry for high power application.

The main goal of this paper is to propose three single-phase AC-to-AC converters based on AC-DC Nabae converter which improve input power factor and input current waveform without any complicated switching modulation such as pulse width modulation or a complicated feedback control [16]. The proposed topologies can operate with either variable output frequency in applications such as AC drive systems, or with fixed output frequency such as UPS.

A direct comparison between the Nabae and the Full-Bridge standard configurations is shown in Table I, in this table the power switches are considered with anti-parallel diodes. The capacitors C_1 and C_2 were not included in the comparison shown in Table I because their sizes are negligible ($C_1 = C_2 = 1\mu F$) and in this way it is no important for final price of the configurations.

Figure 1 shows the proposed configurations. The input of all proposed converters is composed of a full-bridge diode, a pair of capacitors, a pair of inductors and a pair of switching devices, while the output converter is composed by a two-leg full-bridge converter (Configuration $3L$), as in Figure 1(a), or a one-leg half-bridge converter (Configuration $2L_c$), as in Figure 1(b), or a two-leg shared-leg converter (Configuration $2L_s$), as in Figure 1(c). It is worth to mention that the configuration shown in Figure 1(c) has already been studied in a previous work [17], but with the limitation of fixed output frequency.

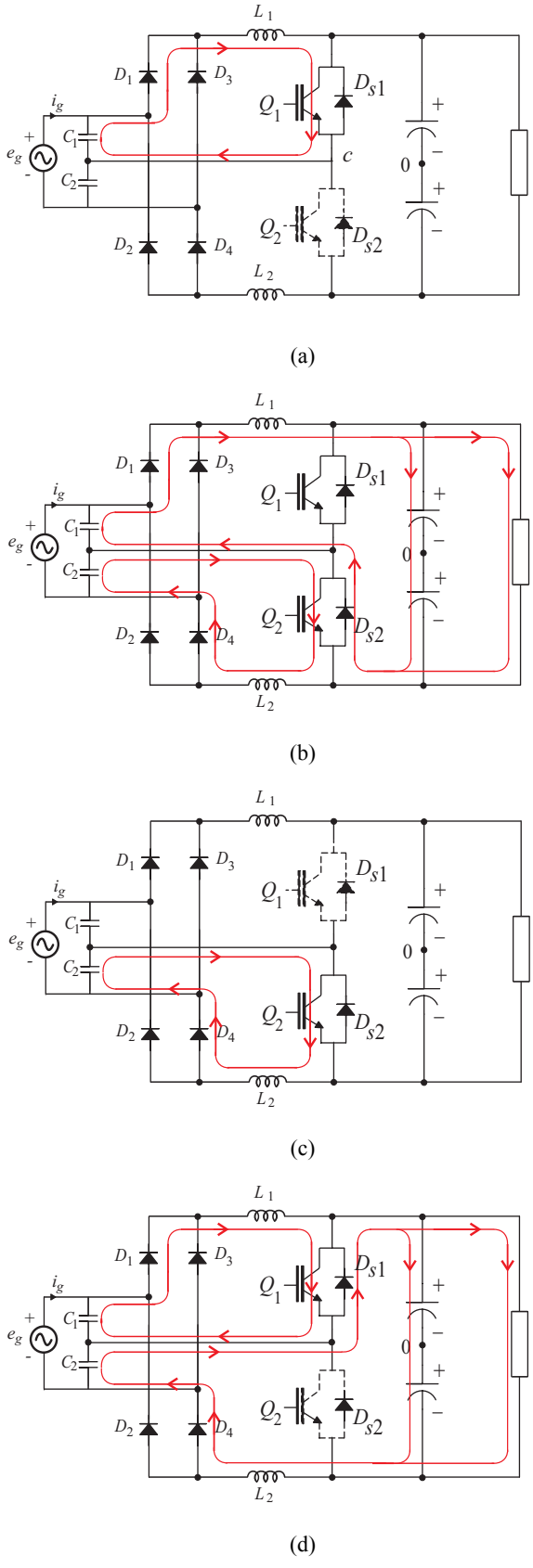


Fig. 3. Nabae converter modes of operation: (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4.

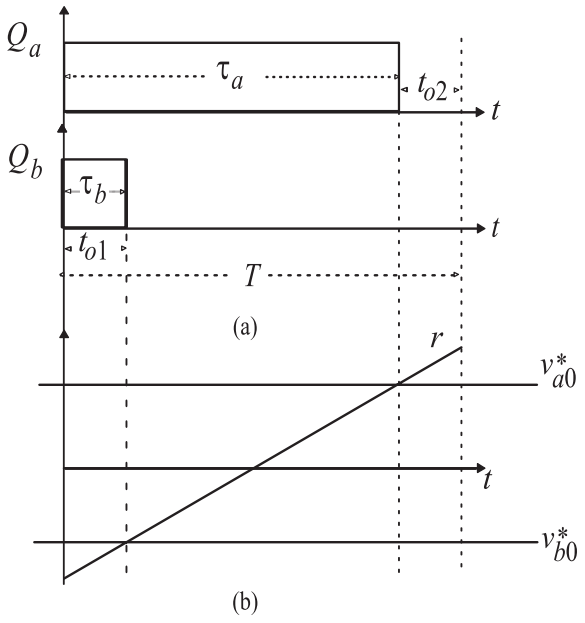


Fig. 4. (a) Pulse widths τ_a and τ_b. (b) Equivalence to the triangular carrier technique (hardware technique).

II. CHARACTERISTICS OF THE NABAE CONVERTER (INPUT CONVERTER SIDE)

A. Principle of operation

The input converter side (Nabae Converter) shows in Figure 2 consists of a diode bridge (D_1, D_2, D_3 and D_4), a pair of small capacitors (C_1, C_2), a pair of inductors (L_1, L_2) and a pair of IGBTs, each IGBT includes a flywheel diode. The two IGBTs are switched ON and switched OFF complementarily (duty cycle for each one is 50%, that is $D_1 = D_2 = 0.5$) at a constant frequency much higher than the source frequency. In the Nabae converter there are four modes of operation, as shown in the Figure 3.

In Mode 1 IGBT Q1 is switched ON and the current flows via C_1 - D_1 - L_1 - Q_1. Energy stores up in L_1, while a discharge current of output capacitor C flows through output converter side. In Mode 2, Q_1 is switched OFF and Q_2 is switched ON at the same time. Then, the stored energy of L_1 is released to the output converter side and C via D_{S2} - C_1 - D_1, while L_2 stores energy by a current though C_2 - Q_2 - $D2$. After all energy in L_1 is released, Mode 3 starts, similarly to Mode 1, but with the parts related to the bottom side. So it is for Mode 4.

The input current is a continuous sinusoidal waveform, the ripple frequency is twice the switching frequency, and the amplitude of the ripple component is far decreased, compared to that of the discontinuous inductor current.

As shown in [16] the input average current is given by

$$i_g = \frac{e_g T_s}{16L}\frac{1}{\left(1 - e_g / 2E\right)} \tag{1}$$

where e_g is the input voltage, E is the DC-bus voltage, Ts is the switching frequency, and L is the boost inductance ($L=L_1=L_2$). Considering $M=E/V_g$ as the amplitude of the input voltage, it can be shown that the higher the value of M is the more harmonic content of i_g decreases and the distortion factor is improved.

III. PWM STRATEGY – CONFIGURATION 3*L* (OUTPUT CONVERTER SIDE)

The output converter of Configuration 3*L* [see Figure 1(a)] comprises four switches (Q_{a1}, Q_{a2}, Q_{b1} and Q_{b2}) and a capacitor bank at the DC-link. Switch-pairs $Q_{a1} - Q_{a2}$ and $Q_{b1} - Q_{b2}$ are complementary. The conduction state of all switches can be represented by a homonymous binary variable Q_{a1} and Q_{b1}, where $Q = 1$ indicates a close switch while $Q = 0$ indicates an open one.

If the desired load voltage is given by v_l^*, then the reference mid-point voltage may be expressed as

$$v_{a0}^* = v_l^* + v_\mu^* \tag{2}$$

$$v_{b0}^* = v_\mu^* \tag{3}$$

Equations (2) and (3) can not be solved unless v_μ^* is obtained. The voltage v_μ^* can be calculated taking into account the apportioning factor μ that is

$$v_\mu^* = E\left(\mu - \frac{1}{2}\right) - \mu v_{\max}^* + \left(\mu - 1\right)v_{\min}^* \tag{4}$$

where $v_{\max}^* = \max V$ and $v_{\min}^* = \min V$ where $V = \left\{v_l^*, 0\right\}$.

This expression was derived by using the same approach used to obtain the equivalent one for the three-phase PWM modulator [18], [19].

The apportioning factor μ ($0 \le \mu \le 1$) is given by

$$\mu = t_{o1} / t_o \tag{5}$$

and indicates the distribution of the free-wheeling period t_o (period in which voltages v_{a0} and v_{b0} are equal) at the beginning ($t_{o1} = \mu t_o$) and at the end ($t_{o2} = (1 - \mu)t_o$) of the switching period T (see Figure 4) [18], [19].

In this case, the proposed algorithm is:

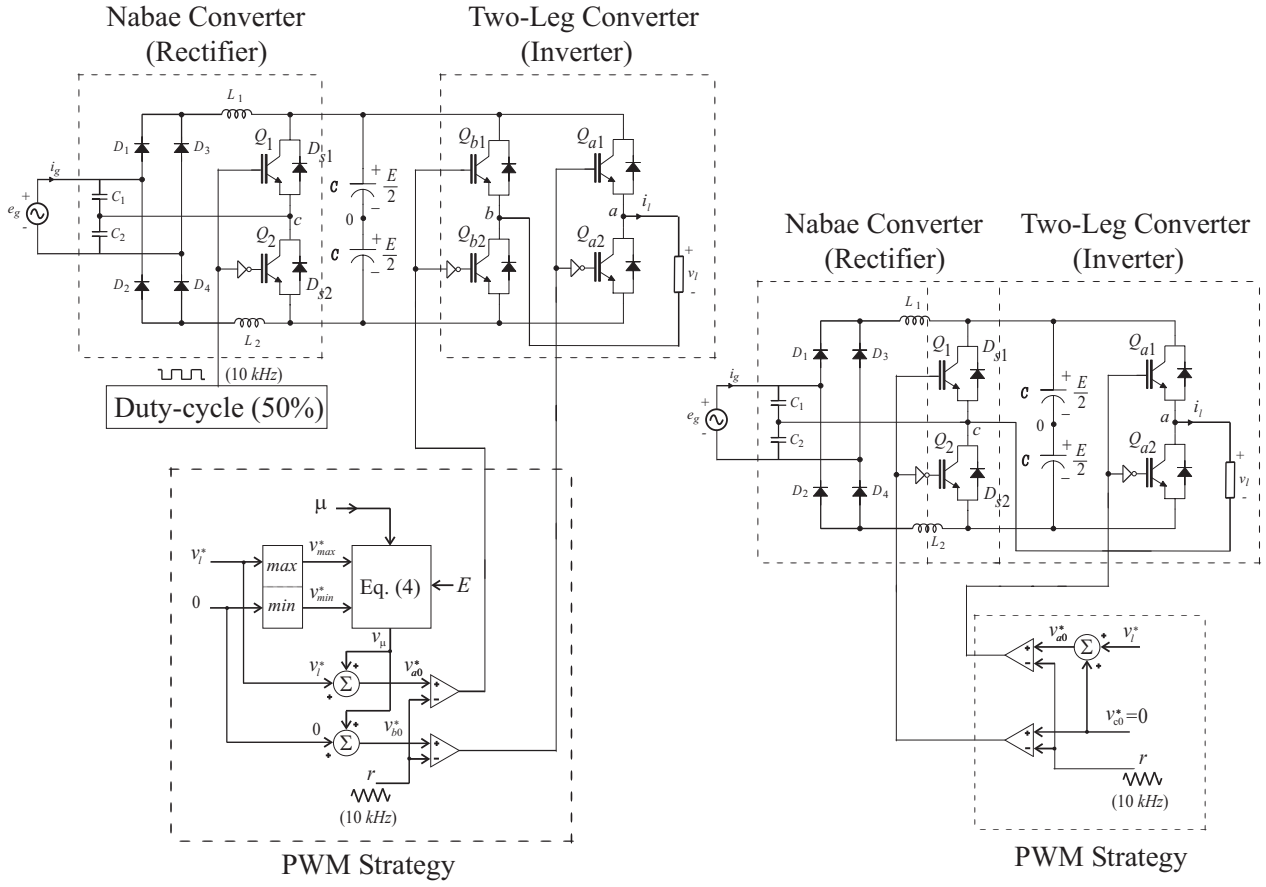
Step 1. Choose the apportioning factor μ and calculate v_μ^* from (4).

Step 2. Determine v_{a0}^* and v_{b0}^* from (2)-(3).

Step 3. Once the mid-point voltage have been determined, pulse-widths τ_a and τ_b are calculated by using

$$\tau_j = \frac{T}{2} + \frac{T}{E}v_{j0}^* \quad \text{for} \quad j=a \text{ or } b \tag{6}$$

where $E = v_{c1} + v_{c2}$ and gating signals (τ_a and τ_b) are generated with programmable timers. Alternatively, gating signals can be generated comparing modulating reference signals v_{a0}^* and v_{b0}^* with a high frequency triangular carrier signal. The PWM strategy described above is shown in Figure 5(a), together with the complete control for Configuration 3L.



(a) (b)

Fig. 5. Implementation scheme for the proposed AC-to-AC converters: (a) Configuration 3*L* and (b) Configuration 2L_c (with the switch *k* connected to point 0) or Configuration 2L_s (with the switch *k* connected to point *s*).

IV. PWM STRATEGY – CONFIGURATION 2L_C (OUTPUT CONVERTER SIDE)

The output converter of Configuration 2L_c [see Figure 1 (b)] comprises two switches (Q_{a1} and Q_{a2}) and a capacitor bank at the DC-link with midpoint connection. As in Configuration 3*L* the switch-pairs Q_{a1} - Q_{a2} are complementary.

If the desired load voltage is given by v_l^* then the reference mid-point voltage may be expressed as

$$v_{a0}^* = v_l^* \tag{7}$$

Once the mid-point voltage has been determined, pulse-width τ_a is calculated by using (6), the gating signal being generated with programmable timers. Alternatively, the gating signal can be generated by comparing the modulating reference signal v_{a0}^* with a high frequency triangular carrier signal. The PWM strategy presented for Configuration 2L_c is shown in Figure 5(b) with the switch *k* connected to point 0, the complete control for Configuration 2L_c is also presented in Figure 5(b).

On the other hand, to eliminate the error due to the capacitor unbalance resultant from the capacitor midpoint connection, the expression (6) is no longer valid. To compensate the capacitor unbalance pulse-widths must be computed by using (8). The new expression for τ_a is given by

$$\tau_a = \left(v_{a0}^* + v_{c2}\right)\frac{T}{v_{c1} + v_{c2}}. \tag{8}$$

Note that it is necessary to measure v_{c1} and v_{c2}. This expression was obtained in [20].

V. PWM STRATEGY – CONFIGURATION 2L_S (OUTPUT CONVERTER SIDE)

The output converter of Configuration 2L_s [see Figure 1(c)] comprises four switches (Q_{a1}, Q_{a2}, Q_1 and Q_2) and a capacitor bank at the DC-link. Switch-pairs Q_{a1} - Q_{a2} and Q_1 - Q_2 are complementary. In this configuration the leg (Q_1 - Q_2) is shared between the input and output converter side.

If the desired load voltage is given by v_l^* then the reference mid-point voltage may be expressed as

$$v_{s0}^* = 0 \tag{9}$$

$$v_{a0}^* = v_l^* + v_{c0}^*. \tag{10}$$

The Configurations 3*L* and 2L_c pulse-widths τ_s and τ_a are calculated by using (6), and gating signals are generated with programmable timers. Alternatively, gating signals can be generated comparing modulating reference signals v_{s0}^* and v_{a0}^* with a high frequency triangular carrier signal.

TABLE II
Comparison among the configurations

	Configuration 3*L*	**Configuration 2L_c**	**Configuration 2L_s**
Number of power switches	6	4	4
Output voltage capability	*E*	*E*/2	*E*/2
Capacitor mid-point connection	*no*	*yes*	*no*

The PWM strategy presented for the Configuration 2L_s is shown in Figure 5(b), with the switch *k* connected to point *s*, as well as the complete control for Configuration 2L_s is shown in Figure 5(b).

VI. COMPARISON AMONG THE CONFIGURATIONS

The direct comparison among the proposed configurations are summarized and shown in Table II.

VII. SIMULATION RESULTS

Some simulation results of the proposed configurations are shown in Figure 6. Figures 6(a), 6(b) and 6(c) shows the power factor control (input current and input voltage) and load current (operating at 20*Hz*) for the Configurations 3*L*, 2L_c and 2L_s, respectively.

Note that for Configuration 3*L* the amplitude of the load current is greater than Configuration 2L_c or 2L_s, due to the maximum dc-bus voltage utilization ($V_l = E$). The amplitude of the load current of the Configurations 2L_c and 2L_s are equal.

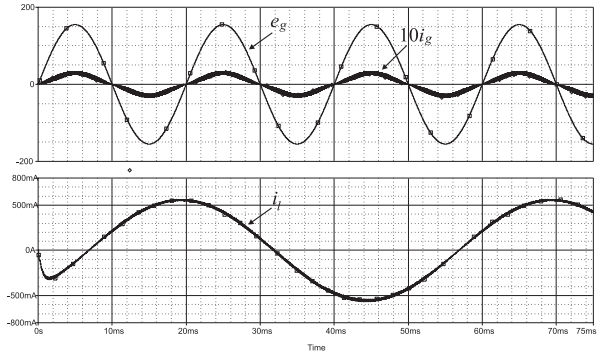
VIII. EXPERIMENTAL RESULTS

Topologies presented in Figure 1 have been experimentally implemented. In the tests the switching frequency was 10*kHz*, the capacitance of the DC-bus capacitor bank was 2200μF, the input capacitances (C_1 and C_2) were 3.3μF, and the inductances (L_1 and L_2) were 2*mH* each one. The set-up used in the experimental tests is based on a microcomputer (PC-Pentium) equipped with appropriate plug in boards and sensors. Switches (Q_{a1} - Q_{a2}, Q_{b1} − Q_{b2} and Q_1 - Q_2) are implemented by IGBTs. Four fast diodes (D_1, D_2, D_3 and D_4) are used in the diode bridge.

Figure 7 presents selected experimental results for Configuration 3*L* [see Figure 1(a)]. Figure 7(a) shows the input voltage source (e_g) and input current (i_g) with high power factor. As expected, the power factor control was obtained without any feedback control and without any current or voltage measurement. Figures 7(b) - 7(d) shows the converter output voltage (v_l) and input current (i_g); in these results the frequency of the output voltage has been, 20*Hz*, 60*Hz* and 80*Hz*, respectively.

Also, as expected, the proposed topologies can operate with independent output frequency. Figures 7(e) and 7(f) show the inductors currents (i_{L1} and i_{L2}) and the dc-link voltage (v_c), respectively.

Similar results were obtained for Configurations 2L_c and 2L_s, as shown in Figures 8 and 9.



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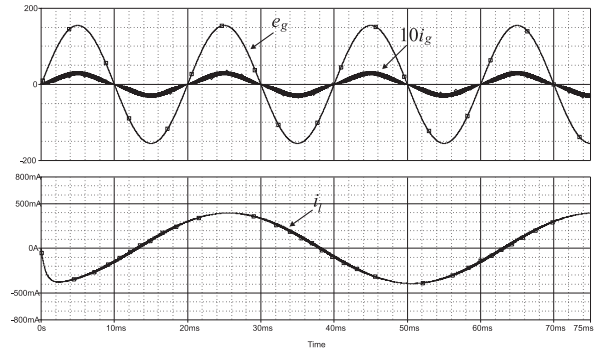

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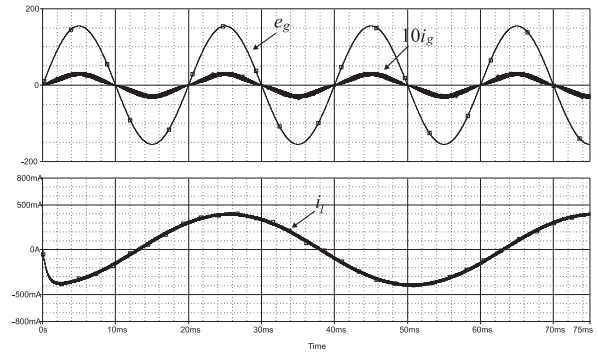

(c)

Fig. 6. Simulation results of the proposed configurations. (a) Configuration *3L*. (b) Configuration *2L*$_c$. (c) Configuration *2L*$_s$.

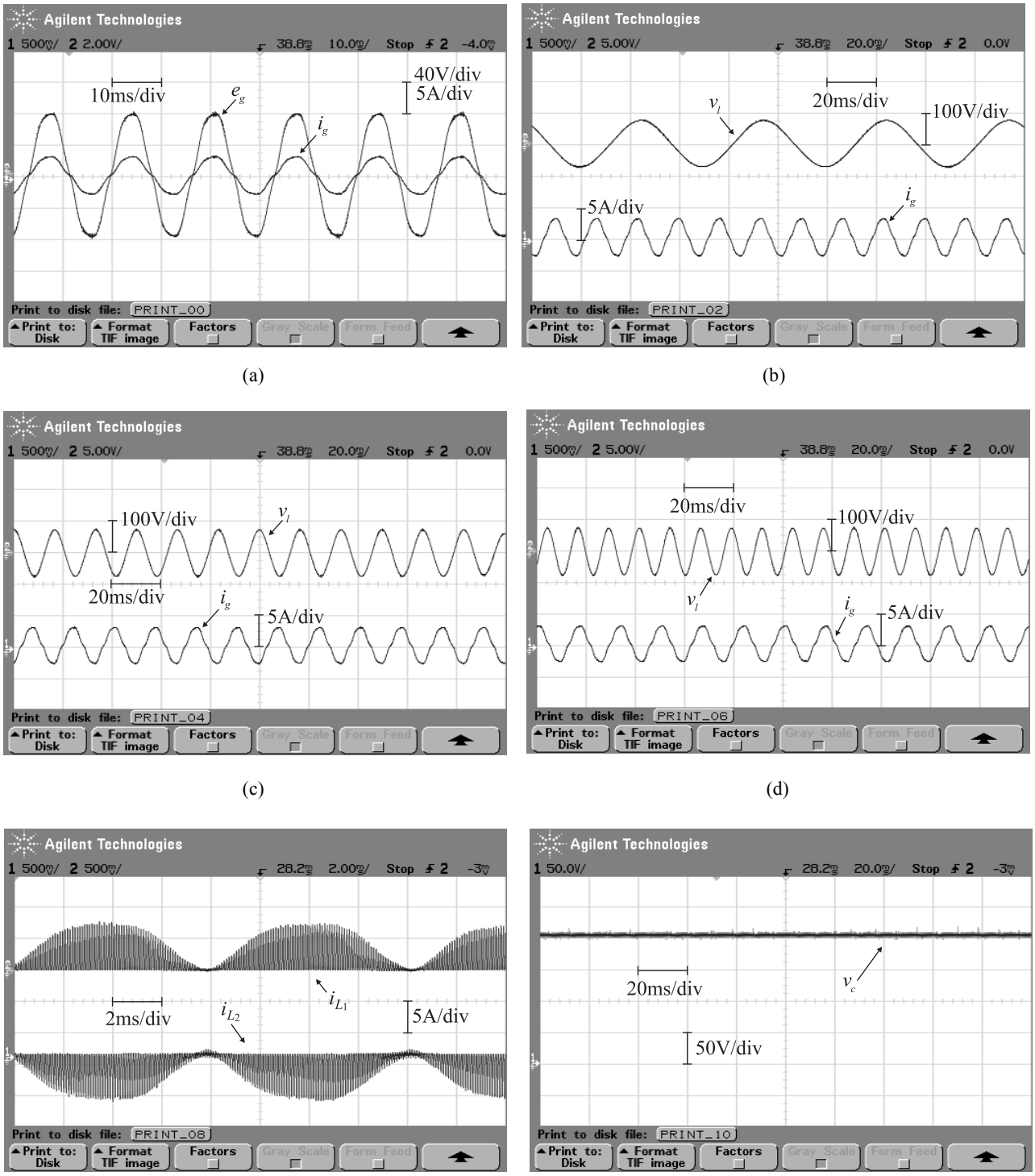

Fig. 7. Experimental results using the proposed integrated AC-to-AC converter (Configuration 3*L*): (a) input voltage source (e_g) and input current (i_g) with high power factor; (b) Converter output voltage (v_l) operating at 20*Hz*; (c) 60*Hz*; (d) 80*Hz*; (e) inductors currents (i_{L1} and i_{L2}); (f) dc-link voltage (v_c).

IX. CONCLUSIONS

This paper has presented three single-phase AC-to-AC converters. The main characteristics of the proposed configurations are:

- Improved input power factor;
- Input sinusoidal current waveform;
- Reduced number of power switches;
- No currents or voltage sensors;
- Independent output voltage.

These characteristics have been obtained without any voltage or current sensor and without any feedback control.

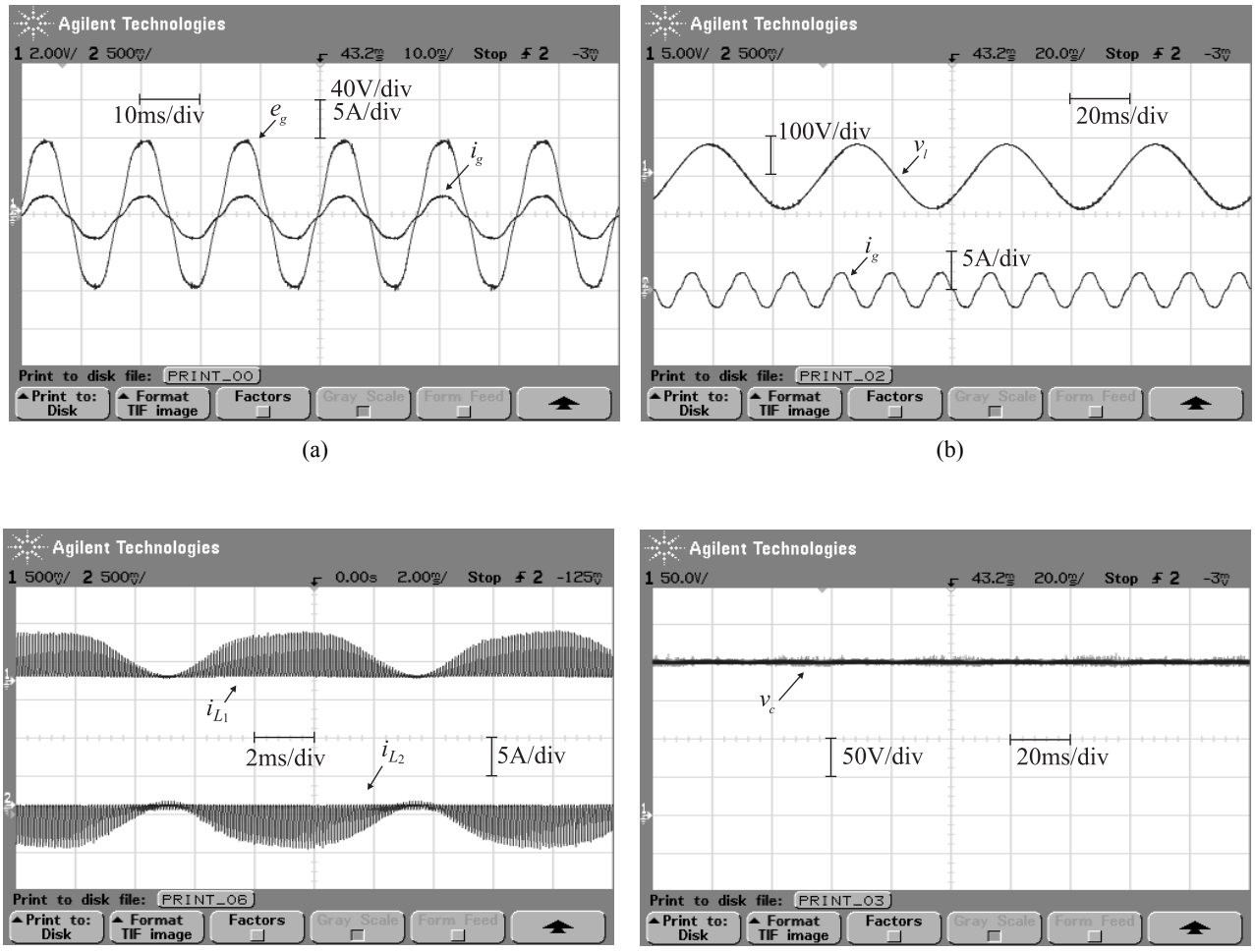

Fig. 8. Experimental results using the proposed integrated AC-to-AC converter (Configuration $2L_c$): (a) input voltage source (e_g) and input current (i_g) with high power factor; (b) Converter output voltage (v_l) operating at $20Hz$; (c) inductors currents (i_{L1} and i_{L2}); (d) dc-link voltage (v_c).

Furthermore, the proposed single-phase AC-to-AC converters represent a reduced switch count power conversion system, and these configurations can operate either with variable output frequency in applications such as AC drive systems, or with fixed output frequency such as UPS (Uninterrupted Power Supply).

This paper has proposed an overall control strategy for each configuration proposed, including an enhanced PWM technique. It has been shown that the overall performance of the system is adequate and the experimental results confirmed the theoretical prediction.

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BIOGRAPHIES

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