DIGITAL CONTROL OF A THREE-PHASE UPS

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Abstract— **This paper presents a design methodology for the digital controllers of a three-phase UPS (Uninterruptible Power Supply). Upon a state-feedback control topology, a systematic method for pole placement and determination of controller gains was developed. In order to attest the efficiency of the adopted control scheme, experimental tests were carried out on a 4kVA three-phase on-line UPS, resulting in unity power factor operation of the controlled rectifier and low harmonic distortion of inverter output voltage, even under heavy non-linear loads.**

Keywords - Digital control, State feedback, Uninterruptible power systems, Power quality.

I. INTRODUCTION

Following the increasing use of electronic equipment and its application in critical areas, a great development of uninterruptible power supplies has been noticed. During the last decades a general awareness of harmonic related power quality issues has also emerged, leading to the creation of a few regulatory standards like the IEC-555 and the IEEE-519 [1]. As an equipment directly related to ensuring power quality, modern UPS systems are generally required to output high quality sinusoidal voltage under various load conditions, while not polluting the AC mains with current harmonics.

Literature mentions many current control schemes that should allow unity power factor operation of a UPS rectifier. Histeresys comparator methods generally result in robust and simple implementations [1]–[3], but the variable switching frequency generates a broad range of harmonics and stresses semiconductors. Predictive controllers can also be used, although their response is somewhat sensitive to the target system model accuracy [2], [3]. Fuzzy-logic and neural network based controllers are ideal for systems where parameters are unknown, but usually require considerable processing power [2]. Linear PI controllers driving a sinusoidal PWM are also a commonly used approach either on stationary [2]–[4] or rotating frames [3], [4]. Although in the stationary frame there is a small phase and magnitude error for sinusoidal references, the analog or digital implementation is quite simple, whereas in the rotating frame the mentioned errors do not exist but the implementation is complex and digital-only.

There are also several methods to achieve a low THD in the inverter output voltage. Although most techniques nowadays are implemented digitally, there is an interesting analog implementation of an instantaneous output voltage control which establishes an analogy between the output LC filter control and a DC motor control [5]. A second approach takes the latter and turns its traditional outer voltage and inner current control loops into a parallel state feedback structure with feed-forward actions for all states [6]. Repetitive controllers represent a very effective approach to compensate for periodic disturbances in the output voltage, as those caused by typical non-linear loads [7], [8]. Nevertheless, they do not compensate for sudden or non-periodic disturbances such as linear load steps, being usually employed along with another controller to carry out this task [9]. Dead-beat controllers are also mentioned as being used to control current while an external voltage loop is driven by a fuzzy-logic controller [10], or as part of a hybrid controller that uses a dead-beat algorithm for non-linear loads and a traditional cascaded linear controller for linear loads [11]. This last method uses dead-beat observers to compensate for the calculation time lag, which affects controller stability in a critical manner. However, the resulting implementation is rather complex [12].

One of the main objectives of this work was to lay the foundation for creating a high-performance digital control software library that can be used to easily integrate UPS systems. Thus, the choice of a state feedback control structure was mainly based on the possibility of automatic calculation of the controllers gains [13]. Since the presented controller design method is general, it can be applied to all the UPS control subsystems, allowing for quick and uniform design. Additionally, the state feedback structure guarantees fast dynamic response of the systems at a reduced computational cost, fulfilling commercial UPS requirements, where digital processors usually take on many sencondary tasks beyond the power converters control.

II. BASIC CONTROL STRUCTURE AND DESIGN METHOD

In this work, the basic state feedback control structure includes two additional feed-forward terms, one for the reference and another for the disturbance [14]. These terms are responsible for reducing the controller action by compensating for steady state conditions, effectively leaving to the controller the task of compensating the transitory load behavior and the steady state errors caused by errors in the system model.

The block diagram of this structure is shown in Figure 1. The reference signal ($w[k]$) is supplied through k_w and the disturbance ($v[k]$) through k_v. The feedback gain vector ($\mathbf{k^T}$) is made up of two parts: one related to the system gains ($\mathbf{k}_s^\mathbf{T}$) and another relative to the state introduced by the output error integrator (k_R). Therefore, $u_c[k]$ represents the state feedback signal, $u_v[k]$ the disturbance feed-forward action and $u_w[k]$ the reference feed-forward signal.

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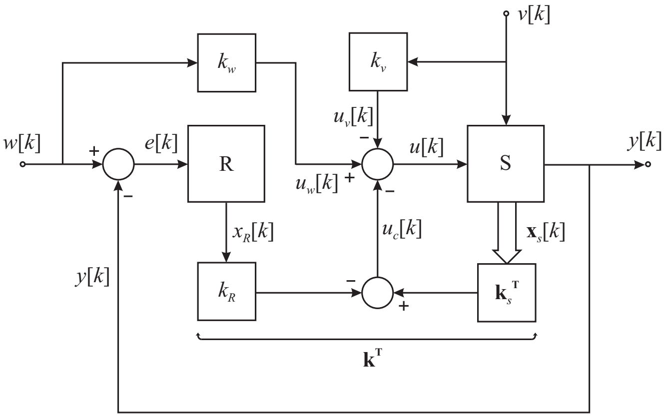

Fig. 1. Basic state feedback control structure.

Considering the system under control (S) as SISO, it is possible to represent it, in discrete form, by the following state equations [14]:

$$\mathbf{x}_s[k+1] = \mathbf{F}_s\,\mathbf{x}_s[k] + \mathbf{h}_s\,u[k] + \mathbf{h}_{sv}\,v[k] \tag{1}$$

$$y[k] = \mathbf{c}_s^{\mathbf{T}}\,\mathbf{x}_s[k] \tag{2}$$

In order to obtain the equations of the closed loop system, one needs the equations of the augmented system, which is the combination of the system to be controlled with the controller integral action and reference feed-forward and disturbance compensation terms. Thereby, its state vector is formed by the original system states plus the integrator related state:

$$\mathbf{x}[k] = \begin{bmatrix} \mathbf{x}_s[k] \\ x_R[k] \end{bmatrix} \tag{3}$$

Note that the augmented system will be of order $n = n_s + 1$ (where n_s is the order of the system to be controlled), and will have the following state equations:

$$\mathbf{x}[k+1] = \mathbf{F}\,\mathbf{x}[k] + \mathbf{h}\,u[k] + \mathbf{h}_w\,w[k] + \mathbf{h}_v\,v[k] \tag{4}$$

$$y[k] = \mathbf{c}^{\mathbf{T}}\,\mathbf{x}[k] \tag{5}$$

where:

$$\mathbf{F} = \begin{bmatrix} \mathbf{F}_s & \mathbf{0} \\ -\mathbf{c}_s^{\mathbf{T}} & 1 \end{bmatrix};\quad \mathbf{h} = \begin{bmatrix} \mathbf{h}_s \\ 0 \end{bmatrix};\quad \mathbf{h}_w = \begin{bmatrix} \mathbf{0} \\ 1 \end{bmatrix};\quad \mathbf{h}_v = \begin{bmatrix} \mathbf{h}_{sv} \\ 0 \end{bmatrix}$$

$$\mathbf{c}^{\mathbf{T}} = \begin{bmatrix} \mathbf{c}_s^{\mathbf{T}} & 0 \end{bmatrix} \tag{6}$$

Once the state vector of the augmented system (3) is defined, its state feedback gain vector is automatically established as:

$$\mathbf{k}^{\mathbf{T}} = \begin{bmatrix} \mathbf{k}_s^{\mathbf{T}} & -k_R \end{bmatrix} \tag{7}$$

Based on Figure 1, the controller output can be written as:

$$u[k] = -\mathbf{k}^{\mathbf{T}}\,\mathbf{x}[k] + k_w\,w[k] - k_v\,v[k] \tag{8}$$

By combining equation (8) with the state equation of the augmented system (4), the closed loop state equations are obtained, including the reference and disturbance feed-forward actions:

$$\mathbf{x}[k+1] = \mathbf{F}_G\,\mathbf{x}[k] + \mathbf{h}_{Gw}\,w[k] + \mathbf{h}_{Gv}\,v[k] \tag{9}$$

$$y[k] = \mathbf{c}^{\mathbf{T}}\,\mathbf{x}[k] \tag{10}$$

where:

$$\mathbf{F}_G = \mathbf{F} - \mathbf{h}\,\mathbf{k}^{\mathbf{T}} \tag{11}$$

$$\mathbf{h}_{Gw} = \mathbf{h}_w + \mathbf{h}\,k_w \tag{12}$$

$$\mathbf{h}_{Gv} = \mathbf{h}_v - \mathbf{h}\,k_v \tag{13}$$

As long as the system controllability is attested, the poles of the closed loop system can be placed in arbitrary positions by adequately adjusting the state feedback gains. Once the required system performance parameters are defined, it is possible to apply pole placement techniques to obtain the necessary state feedback gains.

Following that, the reference feed-forward and disturbance compensation gains (k_w and k_v) should be found. In this work, it was assumed the controller should only compensate for transients and errors in the system model. Thereby, k_w and k_v should be calculated as to guarantee null controller output ($u_c[k] = 0$) in steady state for a step input, leading to the following expressions [14]:

$$k_w = \frac{1}{\mathbf{c}_s^{\mathbf{T}}\,(\mathbf{1} - \mathbf{F}_s + \mathbf{h}_s\,\mathbf{k}_s^{\mathbf{T}})^{-1}\,\mathbf{h}_s} \tag{14}$$

$$k_v = \frac{\mathbf{c}_s^{\mathbf{T}}\,(\mathbf{1} - \mathbf{F}_s + \mathbf{h}_s\,\mathbf{k}_s^{\mathbf{T}})^{-1}\,\mathbf{h}_{sv}}{\mathbf{c}_s^{\mathbf{T}}\,(\mathbf{1} - \mathbf{F}_s + \mathbf{h}_s\,\mathbf{k}_s^{\mathbf{T}})^{-1}\,\mathbf{h}_s} \tag{15}$$

III. RECTIFIER MODEL AND CONTROLLER DESIGN

The input rectifier of the target UPS is a three-phase power converter switching at 15360Hz, as shown in Figure 2. Besides being capable of unity power factor operation, this structure allows for bi-directional power flow, providing fast response and a very good DC bus regulation [3].

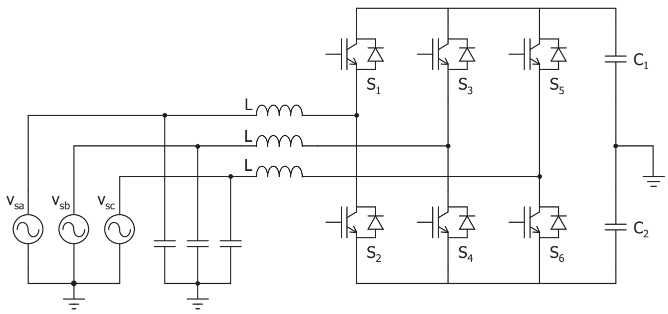

Fig. 2. Three-phase rectifier schematic diagram.

According to Figure 3, the DC bus voltage and capacitors voltage balance control systems form an outer and slower control loop, whose output is the reference to the faster, inner control loop of inductor current.

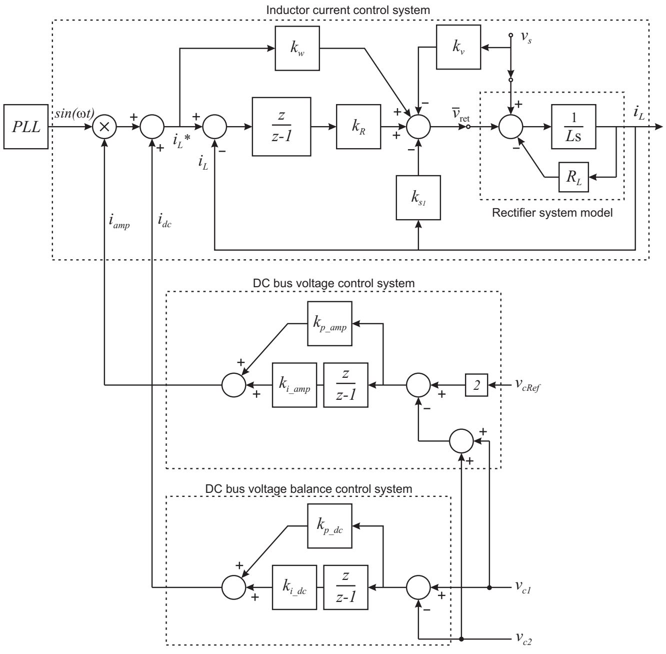

Fig. 3. Rectifier control system diagram.

A. Inductor current control system

Figure 4 presents the simplified diagram for the rectifier current control system. Each rectifier leg is represented by the voltage source $v_{ret}(t)$, which is the input variable in the current control system. The mains voltage, represented by $v_s(t)$, is considered a disturbance in the system model.

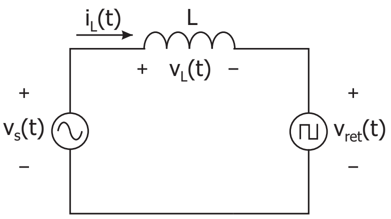

Fig. 4. Simplified rectifier model.

The difference equation shown in (16) can be derived directly from the presented model, as long as two approximations are taken into account: constant instantaneous mains voltage during the sampling period (T_s) and zero inductor resistance.

$$i_L[k+1] = i_L[k] + \frac{T_s}{L}\, v_s[k] - \frac{T_s}{L}\, \bar{v}_{ret}[k] \tag{16}$$

To achieve the goal of controlling the inductor current (i_L), one can actuate on the mean voltage applied by the rectifier during the sampling period ($\bar{v}_{ret}$), the mains voltage (v_s) being considered a disturbance. According to equations (1) and (2), that leads to:

$$\mathbf{F}_s = 1\ ;\quad \mathbf{h}_s = -\frac{T_s}{L}\ ;\quad \mathbf{h}_{sv} = \frac{T_s}{L}\ ;\quad \mathbf{c}_s^{\mathbf{T}} = 1 \tag{17}$$

The reference input of the current controller is a 60Hz sinusoidal signal. Thus, it is enough to define the closed loop poles at 600Hz. Considering an optimal damping response ($\xi = 0.707$), the following poles are obtained:

$$s_1, s_2 = -2665.3 \pm 2666.1j \,\mathrm{rad/s} \tag{18}$$

As the whole rectifier control system runs at a 15360Hz sampling frequency (f_s), these poles are mapped on the z plane as:

$$z_1, z_2 = 0.8281 \pm 0.1452j \tag{19}$$

By supplying the discrete system state matrices (17) – with $L = 4.14\mathrm{mH}$ – and the desired closed loop poles (19) to the controller design method presented herein, the controller gains are output as follows:

$$\begin{aligned} k_w &= -21.8869\ ; & k_{s1} &= -21.8669 \\ k_v &= -1\ ; & k_R &= -3.2204 \end{aligned} \tag{20}$$

B. DC bus voltage control system

The DC bus of the target UPS is composed by a capacitor voltage divider with a neutral connected center tap. The batteries connected in parallel to each capacitor bank are not considered in this model since the DC bus control system should work even with no batteries attached (worst case).

By analyzing the DC bus energy balance with a small signal model, the following state equations can be derived:

$$\begin{aligned} \Delta\dot{v}_{dc}(t) &= \left(\frac{3}{2}\,\frac{V_{\phi(peak)}}{V_{dc}}\,\frac{1}{C_{eq}}\right)\Delta i_L(t) \\ y(t) &= \Delta v_{dc}(t) \end{aligned} \tag{21}$$

where Δv_{dc} represents a small change in the DC bus voltage, Δi_{dc} a small change in the inductor current, $V_{\phi(peak)}$ the mains peak voltage, V_{dc} the DC bus nominal voltage and C_{eq} the equivalent series association of the capacitor banks which make up the voltage divider.

Considering $V_{\phi(peak)} = 180\mathrm{V}$, $V_{dc} = 456\mathrm{V}$, $C_{eq} = 1400\mu\mathrm{F}$ and discretizing the system for $f_s = 15360\mathrm{Hz}$, the following matrices are obtained:

$$\mathbf{F}_s = 1\ ;\quad \mathbf{h}_s = 0.0275\ ;\quad \mathbf{c}_s^{\mathbf{T}} = 1 \tag{22}$$

This controller has to be slow enough to avoid distorting the current controller output, but fast enough to keep up the nominal DC bus voltage irrespective of the loads connected to the inverter output. It is worth pointing out that three-phase non-linear loads on the UPS output cause a 360Hz ripple on the DC bus voltage, and single-phase non-linear loads are even worse, causing a 120Hz ripple on the DC bus.

Thus, the strategy was setting the closed loop poles to reject the 120Hz ripple by 20dB, resulting in a 8.5Hz pole frequency. Applying the optimum damping criteria ($\xi = 0.707$), the resulting poles were:

$$s_1, s_2 = -37.7588 \pm 37.7702j \,\mathrm{rad/s} \tag{23}$$

which map on the z plane as:

$$z_1, z_2 = 0.9975 \pm 0.0025j \tag{24}$$

Taking (22) and (24) through the proposed controller design method, the following gains are output:

$$k_w = 0.1786\ ;\quad k_{s1} = 0.1786\ ;\quad k_R = 4.3799\times10^{-4} \tag{25}$$

With $k_w = k_{s1}$ and $k_v = 0$ in the control diagram of Figure 1, the controller becomes a conventional PI controller, as shown in Figure 3.

C. DC bus capacitors voltage balance control system

Figure 5 shows the system schematic diagram, as well as the relevant signals for the DC bus capacitors voltage balance control.

According to the adopted conventions, if voltage $v_{C_1}(t)$ drops below $v_{C_2}(t)$, a rise in current $i_{C_1}(t)$ over current $i_{C_2}(t)$ is needed to re-establish the voltage balance, which leads to a positive $i_{dif}(t)$. On the other hand, if it is voltage $v_{C_2}(t)$ which drops below $v_{C_1}(t)$, it is necessary that current $i_{C_2}(t)$ rises over $i_{C_1}(t)$, which means a negative $i_{dif}(t)$ is needed to re-establish the voltage balance.

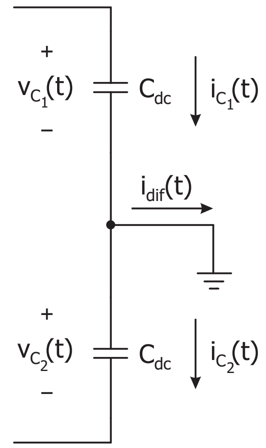

Fig. 5. DC bus capacitors voltage balance model.

Considering $i_{dif}(t) = i_{C_1}(t) - i_{C_2}(t)$ and $v_{dif}(t) = v_{C_1}(t) - v_{C_2}(t)$, it is possible to represent the system by the following state equations:

$$\begin{aligned} \dot{v}_{dif}(t) &= \left(\frac{1}{C_{dc}}\right) i_{dif}(t) \\ y(t) &= v_{dif}(t) \end{aligned} \tag{26}$$

By taking $C_{dc} = 2800\mu\text{F}$ and discretizing the system for $f_s = 15360\text{Hz}$, the following discrete matrices are obtained:

$$\mathbf{F}_s = 1 \; ; \quad \mathbf{h}_s = 0.0233 \; ; \quad \mathbf{c}_s^{\mathrm{T}} = 1 \tag{27}$$

Since this controller affects the current controller reference by injecting a DC level in its reference, it should do so in a very soft manner. For achieving that, a 2Hz frequency was chosen for the closed loop poles, with a damping factor of $\xi = 0.707$:

$$s_1, s_2 = -8.8844 \pm 8.8871j \,\text{rad/s} \tag{28}$$

which map on the z plane as:

$$z_1, z_2 = 0.9994 \pm 0.0006j \tag{29}$$

Applying the controller design method to (27) and (29), the following gains result:

$$k_w = 0.0498 \; ; \quad k_{s1} = 0.0498 \; ; \quad k_R = 2.8770 \times 10^{-5} \tag{30}$$

As in the DC bus voltage controller, this one can also be replaced by a PI controller with $k_p = k_w = k_{s1}$ and $k_i = k_R$, as shown in Figure 3.

IV. INVERTER MODEL AND CONTROLLER DESIGN

The UPS output inverter is a three-phase half-bridge with output LC filters, as shown in Figure 6.

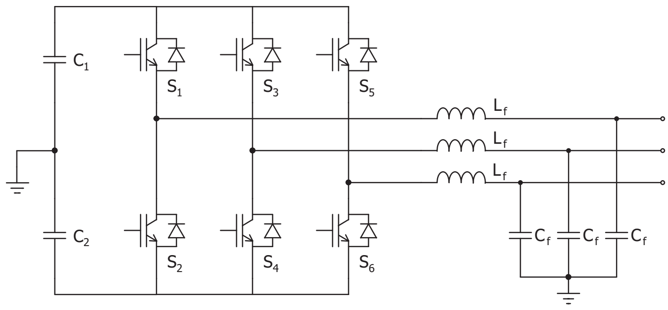

Fig. 6. Three-phase output inverter schematic diagram.

Figure 7 presents the schematic diagram of the per-phase output circuit, from which a simple dynamic model can be derived for the LC filter. By inspection, its continuous differential equations (31) and (32) can be written.

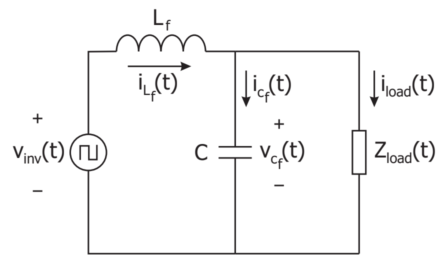

Fig. 7. Output inverter and LC filter schematic diagram.

$$\frac{\mathrm{d}}{\mathrm{d}t} v_{C_f}(t) = \frac{1}{C_f}\, i_{L_f}(t) - \frac{1}{C_f}\, i_{load}(t) \tag{31}$$

$$\frac{\mathrm{d}}{\mathrm{d}t} i_{L_f}(t) = \frac{1}{L_f}\, v_{inv}(t) - \frac{1}{L_f}\, v_{C_f}(t) \tag{32}$$

The system output was taken as the capacitor voltage (v_{C_f}), and the actuating signal is the voltage applied by the inverter (v_{inv}). The load current (i_{load}) is considered a disturbance.

For the controller to cope with the faster dynamic response requirements of the inverter under non-linear loads, an assymetric PWM technique was used. With this PWM method, the sampling frequency is the double of the IGBT switching frequency, which remains at 15360Hz. Thus, taking $C_f = 28\mu\text{F}$ and $L_f = 900\mu\text{H}$ and discretizing the system for $f_s = 32720\text{Hz}$, the following matrices are obtained:

$$\begin{aligned} \mathbf{F}_s &= \begin{bmatrix} 0.9790 & 1.1544 \\ -0.0359 & 0.9790 \end{bmatrix}; \quad & \mathbf{h}_s &= \begin{bmatrix} 0.0210 \\ 0.0359 \end{bmatrix} \\ \mathbf{c}_s^{\mathrm{T}} &= \begin{bmatrix} 1 & 0 \end{bmatrix}; & \mathbf{h}_{sv} &= \begin{bmatrix} -1.1544 \\ 0.0210 \end{bmatrix} \end{aligned} \tag{33}$$

In order to completely specify the closed loop behavior of the output voltage control system (Figure 8), three poles have to be placed (the LC filter itself is already a 2$^{\text{nd}}$ order system).

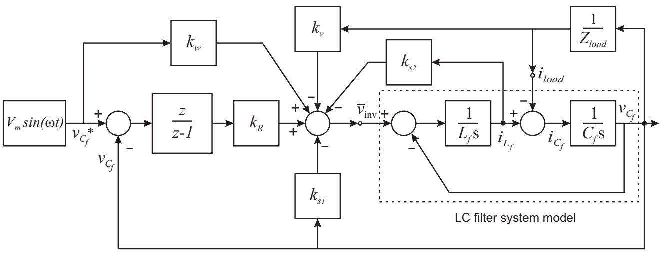

Fig. 8. Closed loop inverter output voltage control system.

Aiming to get a 60Hz sinusoidal reproduced by the inverter with negligible phase error, the smaller pole frequency was set at 800Hz (real pole). The remaining two poles were defined as complex conjugates, at a frequency of 2000Hz with a damping factor $\xi = 0.707$:

$$\begin{aligned} s_1, s_2 &= -8884.4 \pm 8887.1j \text{ rad/s} \\ s_3 &= -5026.5 \text{ rad/s} \end{aligned} \tag{34}$$

Mapping these on the z plane leads to:

$$\begin{aligned} z_1, z_2 &= 0.7177 \pm 0.2136j \\ z_3 &= 0.8491 \end{aligned} \tag{35}$$

Applying the controller design method to (33) and (35), the obtained controller gains are:

$$\begin{aligned} &k_w = 4.7984\ ; \qquad k_{s1} = 3.7984\ ; \qquad k_R = 0.4614 \\ &k_v = -16.5380\ ; \qquad k_{s2} = 16.5380 \end{aligned} \tag{36}$$

Extensive computer simulation showed this arrangement, in conjunction with a saturation in the controller integrator, proved adequate for providing low harmonic output voltage under heavy non-linear loads.

V. EXPERIMENTAL RESULTS

The target UPS is a commercial 4kVA on-line UPS equipped with two identical CPU boards based on a Texas Instruments TMS320LF2407A DSP. The first board is connected to the controlled rectifier and runs an A/D driver, a PLL, responsible for the sinusoidal references for the current controller, the 3-phase current controller, the DC bus voltage and balance controllers, a PWM generator and its driver. The second board is connected to the inverter and runs an A/D driver, a 3-phase sinusoidal reference generator, the 3-phase output voltage controller and a PWM generator and its driver.

The following sections present several experimental tests carried out to verify the effectiveness of the designed algorithms.

A. Controlled rectifier

1) Rectifier start-up: Figure 9 shows the UPS already connected to a tree-phase 220V system when the rectifier is started. Note the initial voltage on the capacitor bank C_1 is 180V, with the rectifier still inactive.

Once the rectifier is turned on, voltage on C_1 stabilizes at $230V$ in 96ms, showing a steady state error of 0.87% from its nominal value of 228V (the full DC bus nominal voltage is 456V). The small line current before and after the transient is caused by the input capacitor filters (Figure 2).

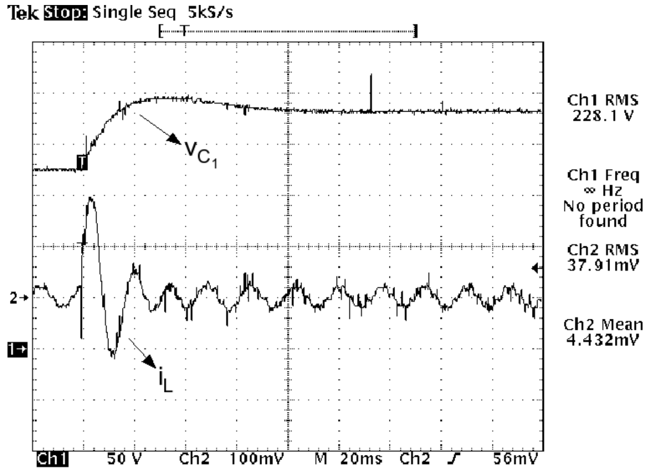

Fig. 9. Voltage on DC bus capacitor C_1 and line current (10mV/A).

2) DC bus full power step load: in order to evaluate the transient response of the DC bus voltage controller, a 4kW resistive load was connected across the whole DC bus. Figure 10 shows the voltage on capacitor bank C_1 suffers a 12% drop relative to its nominal value when the load is connected, recovering completely in 86ms. The line current on that condition is almost sinusoidal.

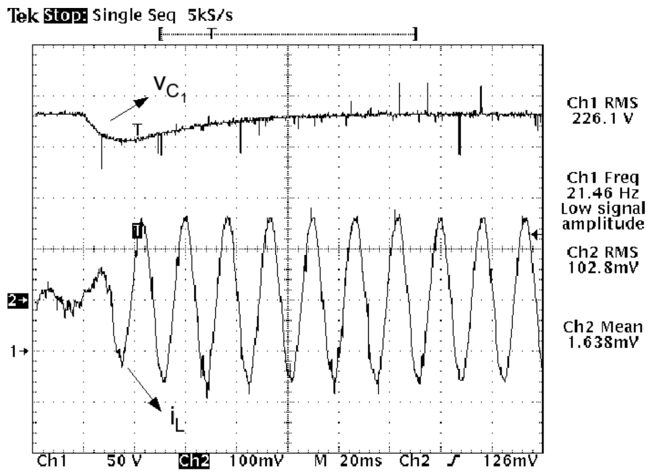

Fig. 10. Voltage on DC bus capacitor C_1 and line current (10mV/A).

3) Full load steady state: keeping the 4kW resistive load applied across the DC bus, Figure 11 shows the rectifier operating at unity power factor, with a $4.4°$ displacement angle.

4) DC bus unbalanced step load: in order to verify the DC bus capacitors voltage balance controller, a resistive load of 460W (approximately 10% of the UPS nominal load) was applied from the neutral connected center tap to the upper capacitor bank of the DC bus (C_1). It was verified the system injected a 700mA DC level in the line currents in order to compensate this disturbance, which is shown in Figure 12. According to it, the system recovered in 340ms with the load still applied.

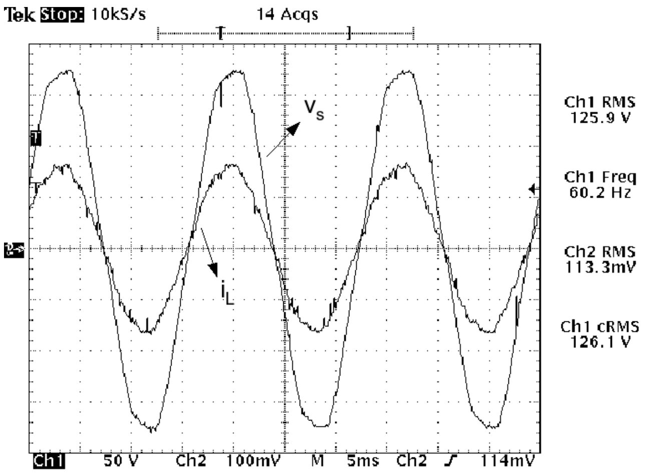

Fig. 11. Mains voltage (1:1 transformer) and line current (10mV/A).

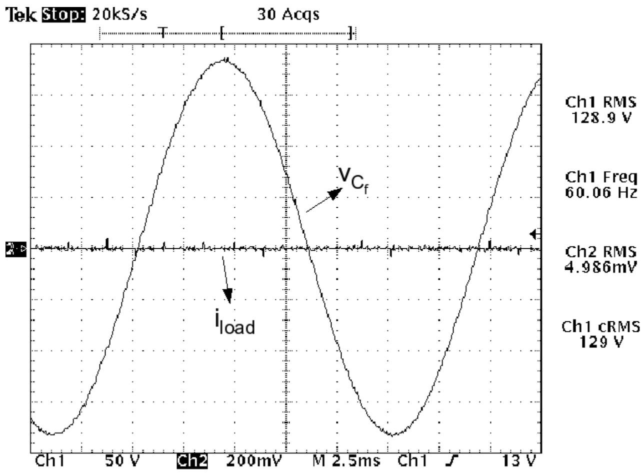

Fig. 13. No-load inverter output voltage.

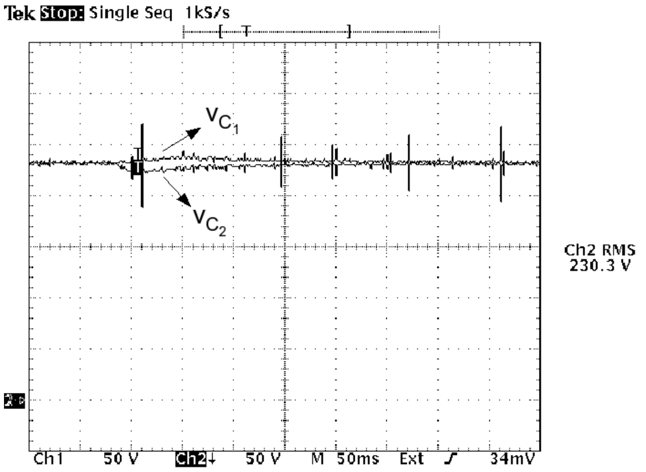

Fig. 12. Voltage on DC bus capacitor banks C_1 and C_2.

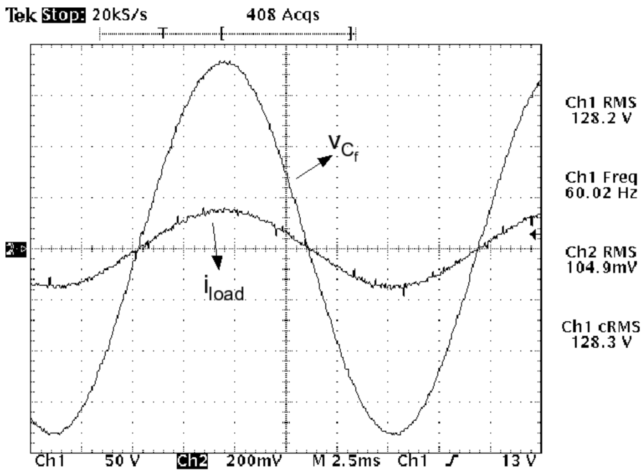

Fig. 14. Inverter output voltage and load current (10mV/A).

B. Output inverter

1) No-load operation: for the output inverter operating at a PWM frequency of 15360Hz and a sampling frequency of $f_s = 30720$Hz with no loads connected, it was obtained a sinusoidal output voltage of $128\mathrm{V_{RMS}}$ with THD=0.42%, as shown in Figure 13.

2) Nominal linear load steady-state operation: the full linear load was applied to the inverter output, drawing a current of $10.5\mathrm{A_{RMS}}$ from the UPS. Under this condition, Figure 14 shows a 0.78% THD output voltage and the load current.

3) Nominal linear load step transitory: while the 4kW linear load remains the same, it is now suddenly connected to the inverter output when the instantaneous output voltage reaches its maximum value. Figure 15 shows a voltage drop of 25%, followed by a 10.6% overshoot before returning to normal, all that under 0.85ms.

4) Nominal non-linear load steady-state operation: in this test an adjustable non-linear load was employed in order to draw the nominal RMS current of 10.5A from the inverter output. That resulted on a heavy non-linear behavior, with crest factor greater than 3. Nevertheless, the output voltage control system was able to attain a 2.83% THD under this load condition (see Figure 16) with no harmonic surpassing 3% of the fundamental amplitude, as it is shown in Figure 17.

VI. CONCLUSION

There were presented several control system models needed to implement a three-phase on-line UPS. It is shown that all the required control subsystems may be subjected to the same state feedback gain calculation method, including optional reference feed-forward and disturbance compensation actions. Implemented in software, the presented methodology allowed for the automatic tunning of all the UPS control loops.

Experimental testing on a 4kVA three-phase UPS demonstrated proper operation of all modeled control subsystems, leading to unity power factor operation of the controlled rectifier and a total harmonic distortion as low as 2.83% for the inverter output voltage, even under non-linear loads with crest factor greater than 3.

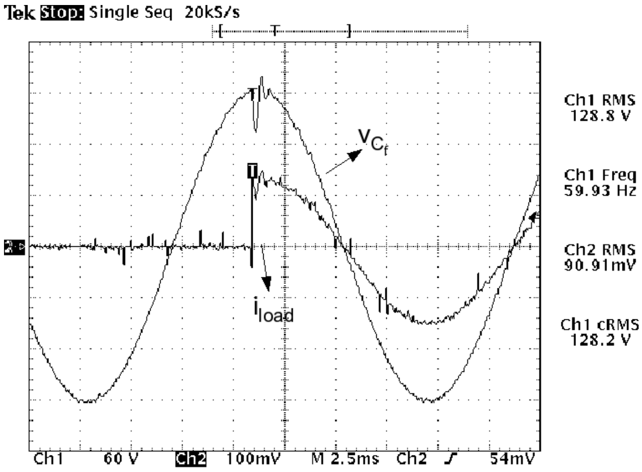

Fig. 15. Output voltage and load current (10mV/A).

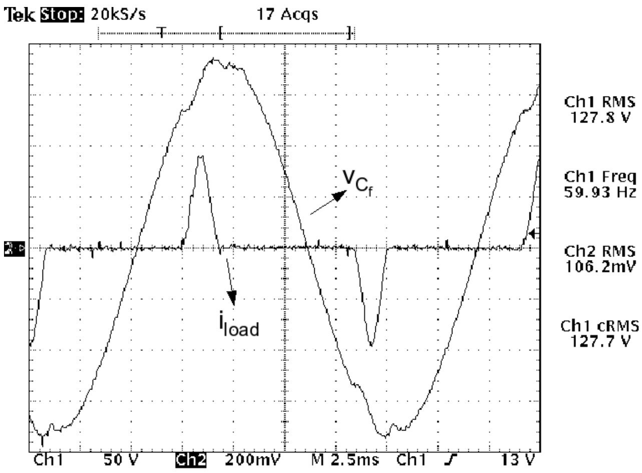

Fig. 16. Output voltage and load current (10mV/A).

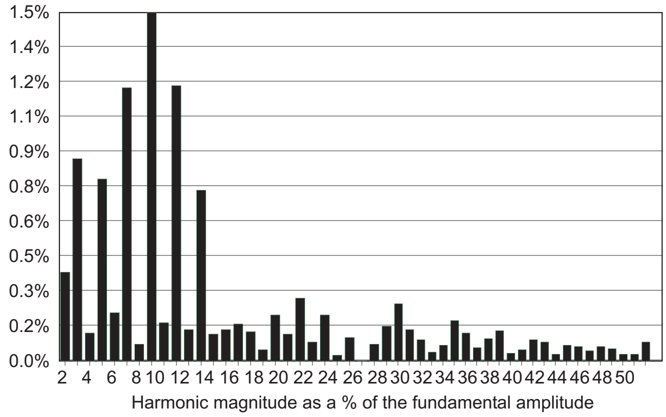

Fig. 17. Output voltage harmonic analysis.

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BIOGRAPHIES

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