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Modified SEPIC ZVRT Converter with Serial Magnetic Coupling and Voltage Multiplier Cell

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ABSTRACT This paper presents a high voltage gain dc-dc converter operating with soft switching, high switching frequency, and reduced voltage stress in all semiconductors, which is suitable for applications as renewable energy sources. The proposed topology uses the coupled inductor and voltage multiplier cell techniques to obtain high voltage gain. The switch turn-on and turn-off occur with zero voltage switching (ZVS). The soft-switching range is independent of the load and is maintained from nominal output power to light load operation with reduced conduction losses. The theoretical analysis and experimental results of a prototype with 94.55% efficiency at nominal output power (200 W) operating with voltage gain equal to 15 times are presented in this paper.

KEYWORDS dc-dc converters, soft-switching, renewable energy, high voltage gain.

I. INTRODUCTION

The development of non-isolated dc-dc converters with a high voltage gain is a focus of research due to the advancement of their applications on renewable energy sources, battery powered systems, and electric vehicle applications, among others. However, the classical step-up structures have limitations such as dissipative commutations, high voltage and current stress for the semiconductors, as well as operation with high duty-cycles, limiting the use of conventional non-isolated dc-dc converters in operations demanding high switching frequency and efficiency [1]. The operation of conventional non-isolated converters can be improved with techniques that increase the voltage gain without increasing the duty-cycle. These techniques can be particularly interesting in applications requiring very high voltage gains (Vo/Vi> 10). Several topologies have been proposed in the literature, including some techniques to increase the voltage gain of conventional boost converters and other non-isolated structures. An extensive analysis of these techniques and a comparison among high voltage gain dc-dc converters is presented in [1]. However, most structures present hard-switching, which limits the operation on high switching frequencies (f >100 kHz).

In this paper, the integration of a soft-switching technique to high-gain non-isolated dc-dc converters to improve the performance and operation on high switching frequency is proposed. Some converter structures and techniques that increase voltage gain are discussed to define the main hard-switching topologies considered, and soft-switching integration and operation are presented for one of these structures. However, the results and considerations described here can be extended to all converters derived from the same principle. The Modified SEPIC converter, presented in Figure 1.a, is a recently developed non-isolated structure capable of reaching a voltage gain close to twice that of the conventional boost converter, with voltage stress in all semiconductors lower than the output voltage [2]. This topology can present high performance in applications with a voltage gain lower than ten times [2]. Including high gain techniques may be necessary to lower the duty-cycle, in order to attain gains higher than ten times. Some examples including capacitors and diodes are the switched capacitor [3]-[4] and voltage multiplier cell [5] techniques, which increase the voltage gain and reduce the semiconductor's voltage stress. However, multiple stages may still be necessary for such high-gain applications, and the reverse recovery current of the diodes must be considered. The coupled inductor is a technique that includes a secondary winding to increase the voltage gain through the coupled inductor turn ratio. However, the energy of the leakage inductance of the coupled inductors must be considered to avoid overvoltage in some semiconductors. Another alternative is the association of two or more high-gain techniques. A configuration proposed in several works is the association of the coupled inductor with the switched capacitor technique, which allows for a very high voltage gain while reducing the drawbacks of each technique. The switched capacitor increases the converter voltage gain and avoids the semiconductor's overvoltage, operating with the energy of the leakage inductance from the coupled inductors as a non-dissipative clamping circuit. The leakage inductance of the coupled inductors limits the semiconductor's current variation (di/dt), reducing the reverse recovery current of the diodes and enabling zero current switching (ZCS). Some configurations of the Modified SEPIC converter using a voltage multiplier cell and coupled inductors, all of which present similar operating characteristics, are presented in Figure 1.b [2], Figure 1.c [7], Figure 1.d [8] and Figure 1.e [9]. The main distinction is how the coupled inductors and the voltage multiplier cell are integrated, which changes the voltage gain, as shown in Figure 1.f. Although these topologies present high performance in applications with very

high voltage gain, dissipative commutation limits the use in applications that demand high switching frequency, making the search for improved solutions an important research topic.

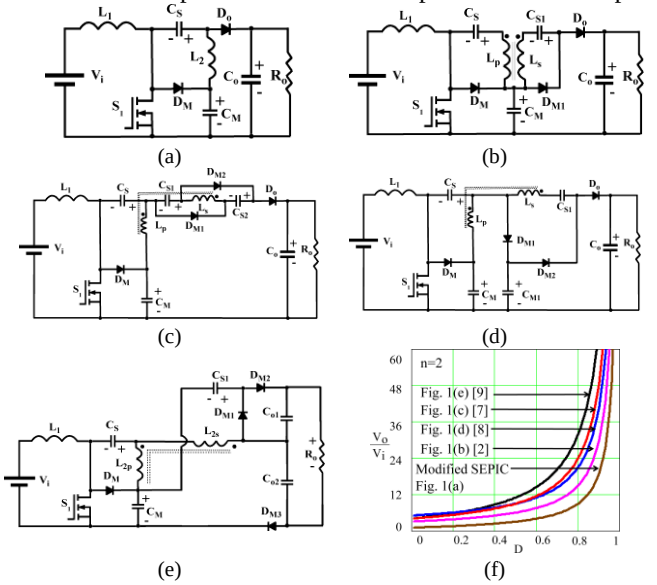

FIGURE 1. Original configuration and topological variations of the Modified SEPIC converter with the inclusion of coupled inductor and voltage multiplier cell techniques operating with dissipative commutation: (a) Original configuration [2]; (b) Variation proposed in [2]; (c) Variation proposed in [7]; (d) Variation proposed in [8]; (e) Variation proposed in [9]; (f) Converter´s voltage gain considering coupled inductor turn ratio n=2.

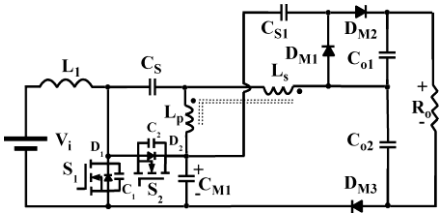

FIGURE 2. Modified SEPIC ZVRT converter with coupled inductor and voltage multiplier cells.

Several soft-switching techniques were developed for dc-dc converters with different costs, complexity, and performance, as presented in [10] and [11]. Active clamping is a widely used soft-switching technique, mainly applied in isolated and non-isolated dc-dc converters with coupled inductors [16]. A clamping capacitor and an active switch are necessary for the active clamping technique. The energy of the leakage inductance is used to charge and discharge the intrinsic capacitance of the switches, resulting in a zero voltage switching (ZVS) operation, as presented in [16]. However, the operation range with soft-switching is limited and not maintained with a light load, which makes it unsuitable for applications such as photovoltaic generation which usually operates in conditions below nominal output power. The weighted efficiency (such as the California Energy Commission - CEC or European efficiency - EU), must be considered for this type of application, because the efficiency presented with reduced load is a significant factor in determining the structure's performance.

Another simple soft-switching technique for non-isolated dc-dc converters is the Zero-Voltage Resonant-Transition (ZVRT) proposed in [12], also recently referred to as Zero-Voltage Switching Quasi-Square Wave (ZVS-QSW) in [13] or Triangular Current Mode (TCM) in [11] and [14]. The unique change for the soft-switching implementation is the replacement of the converter´s diode by an active switch with a complementary command to the main switch command. However, reducing the converter's inductance is necessary for soft-switching, thus increasing the inductor´s current ripple and the converter's conduction losses [10]. This technique maintains the ZVS operation in all load ranges. The ZVRT technique can be implemented for all converters presented in Figure 1, replacing the diode D_M with an auxiliary switch with a complementary command. The operation analysis of this soft-switching technique applied to the basic Modified SEPIC converter shown in Figure 1.a was reported in [15]. However, when this soft-switching technique is applied to the structures with coupled inductors presented in Figure 1, there are some changes in the operation characteristics due to non-idealities present in these structures, such as the coupling inductors' leakage inductance. Therefore, this paper develops the operation analysis of the ZVRT soft-switching technique applied to the Modified SEPIC converter with coupled inductors. The highest voltage gain structure, presented in Figure 1.e, was chosen for the soft-switching circuit operation analysis, but the results can be extended to the other converters with coupled inductors presented in Figure 1 due to the similarity among these structures. By including the soft-switching technique to the hard-switching converter shown in Figure 1.e, the proposed soft-switching converter presented in Figure 2 is obtained.

Recent developments using SEPIC-based high voltage gain dc-dc converters are discussed, highlighting which are the main advantages and contributions of each configuration. Some soft-switching high voltage gain topologies using the semi-resonant soft-switching technique are proposed in [17]-[20]. The original structure of the Modified SEPIC converter presented in Figure 1.a operating with ZVS commutation with a switching frequency equal to 1 MHz and without additional components is proposed in [17]. This is a high-power density configuration for low-power applications, considering the operation only in discontinuous conduction mode (DCM) for the ZVS operation. Some drawbacks of the soft-switching technique include variable switching frequency, operation exclusively in DCM, and some problems with light loads. The configuration of [17] operating with integrated inductors to increase the power density and improve the converter efficiency is proposed in [18]. The same semi-resonant soft-switching technique was applied in [19], with a configuration derived from the topology presented in Figure 1.b, including the switched inductor technique at the input inductor to increase the voltage gain. A high-power density converter is proposed operating at 500 kHz and voltage gain equal to 15 times. The converter presented in Figure 1.b was also proposed in [20], operating with soft-switching using a GaN (Gallium nitride) switch and planar-integrated magnetic components. However, the drawbacks of the converters proposed in [18]-[20] are the same as reported for [17], limiting the use of this soft-switching technique in applications with low output power (P_o<100 W). The voltage gain of the original configuration presented in Figure 1.a is increased in [21] by replacing the input inductor with the switched inductor technique, operating with hard switching. Another configuration of the modified SEPIC converter, using

coupled inductor and voltage multiplier cells similar to the structures presented in Figures 1.c and 1.d, and operated with hard-switching is proposed in [22]. A SEPIC-based converter using a three-winding built-in transformer is reported in [23], and an input current ripple-free configuration is proposed in [24] using a coupled inductor and voltage multipliers. The ripple-free technique allows the reduction of the input inductor as well as the conduction losses. These configurations, both with all dissipative commutation as [21] and with the turn-off dissipative commutation as configurations with coupled inductors [22]-[24], limits the switching frequency (f < 60 kHz) to maintain suitable efficiency. Therefore, the inclusion of a soft-switching technique with simple implementation and operating in continuous conduction mode (CCM) in all load range with low conduction losses is proposed for the Modified SEPIC converter with coupled inductor and voltage multiplier cells.

II. PROPOSED CONVERTER OPERATION

The proposed converter presented in Figure 2 was analyzed operating in continuous conduction mode (CCM), presenting nine operation stages shown in Figure 3. The capacitors are considered voltage sources except for the intrinsic switches' capacitances (C_1-C_2), the diodes are considered ideal, and the circuit is operating at a steady state for the theoretical analysis of the proposed converter. The intrinsic switches' capacitances C_1 and C_2 and the intrinsic switches' diodes D_1 and D_2 are considered in the converter operation. Moreover, non-idealities from the coupled inductor, such as the influence of leakage inductance (L_{dp}) in the topology's voltage gain and the soft-switching process, are considered.

A. *OPERATIONS STAGES*

First stage (t_o-t_1) – Figure 3.a: The input inductor L_1 is magnetizing, submitted to the input voltage V_i because switch S_1 is turned on and S_2 is turned off. The primary winding L_p is submitted to the voltage difference between the capacitors C_{M1} and C_S, and this value is approximately equal to the input voltage. The secondary winding L_S is submitted to a voltage equal to the input voltage multiplied by the coupled inductor turn ratio (n). The semiconductors S_1 and D_{M2} are conducting in this stage, charging the output capacitor C_{o1}. The capacitors C_{S1} and C_{M1} are discharging, whereas C_S is charged by the charge released by C_{M1}. Equation (1) defines the resonant current at the primary winding of the couple inductor L_P during the conduction of the switch S_1 ($i_{Lp\omega o}(t)$). The leakage inductance referent to the primary side (L_{dp}), and the equivalent capacitance C_{eq} calculated by (2) define the resonant frequency (ω_o) in (3). The S_2 switch voltage (V_{S2}) is clamped to the capacitor C_{M1} voltage, which is lower than the output voltage. This stage is finished when the diode D_{M2} is blocked at the end of half of the resonant period $T_o=1/\omega_o$.

Second stage (t_1-t_2) – Figure 3.b: In this stage, the switch S_1 remains in conduction, and S_2 is turned off. The diode D_{M2} is turned off at the end of half of the resonant period at t_2, and the capacitors C_{S1} and C_{o1} have been charged.

$$i_{Lp\omega o}(t) = \sqrt{\frac{C_{eq}}{L_{dp}}} \cdot V_i \cdot \sin(\omega_{o\cdot t}) \tag{1}$$

$$C_{eq} = \frac{1}{\frac{1}{C_S} + \frac{1}{C_{M1}} + \frac{n^2}{C_{S1}}} \tag{2}$$

$$\omega_o = \frac{1}{\sqrt{L_{dp} \cdot C_{eq}}} \tag{3}$$

$$V_{L1}(t) = V_{Lp}(t) = V_{CM1} - V_{CS} = V_i \tag{4}$$

$$V_{S1}(t) = V_{C1}(t) = 0 \tag{5}$$

$$V_{S2}(t) = V_{C2}(t) = V_{CM1} \tag{6}$$

$$V_{Co1} = V_{CS1} + (1+n) \cdot V_i \,. \tag{7}$$

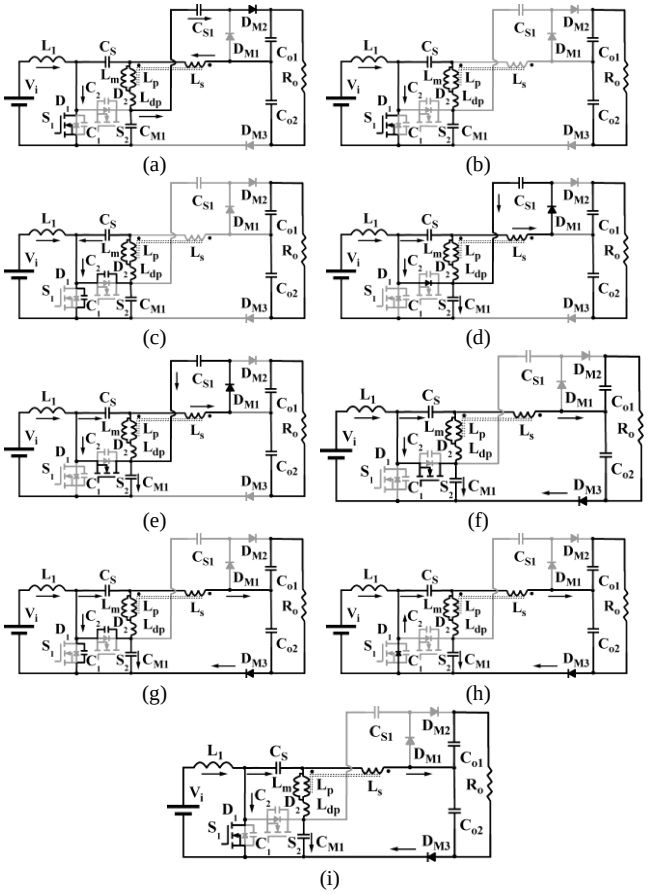

FIGURE 3. Modified SEPIC ZVRT converter coupled inductor and voltage multiplier cells operation stages. (a) First stage; (b) Second stage; (c) Third stage; (d) Fourth stage; (e) Fifth stage; (f) Sixth stage; (g) Seventh stage; (h) Eighth stage; (i) Ninth stage.

The primary winding (L_p) behaves as a simple inductor submitted to the voltage difference between C_{M1} and C_S, equal to the input voltage during this stage. The input inductor L_1 presents low current ripple as the conventional boost converter. The capacitor C_S keeps charging linearly with the charge released by C_{M1}.

$$i_{L1}(t) = I_i - \frac{V_i \cdot D}{f \cdot L_1} + \frac{V_i}{L_1} \cdot (t - t_0) \tag{8}$$

$$i_{Lp}(t) = I_o - \frac{V_i \cdot D}{f \cdot L_p} + \frac{V_i}{L_p} \cdot (t - t_0) + i_{Lp_{\omega o}(t)} \quad (9)$$

.

Third stage (t_2-t_3) – Figure 3.c: In this stage, the switch S_1 is turned off, the intrinsic switch S_1 capacitance (C_1) is charged, while the intrinsic switch S_2 capacitance (C_2) is discharged. When the voltage of capacitor C_1 achieves V_{CM1}, the voltage in C_2 is zero, finishing this operation stage.

$$V_{S1}(t_3) = V_{C1}(t_3) = V_{CM1} \quad (10)$$

$$V_{S2}(t_3) = V_{C2}(t_3) = 0\,. \quad (11)$$

Fourth stage (t_3-t_4) – Figure 3.d: After the voltage in switch S_2 becomes null, the intrinsic diode D_2 conducts, transferring energy to the capacitor C_M. The diode D_{M1} starts conducting, and the capacitor C_{S1} is charged with the current equal to $i_{Ls}(t)$. The capacitor C_{S1} voltage is equal to (12), taking into account the coupled inductor turn ratio (n). The command signal of the switch S_2 must be applied during the conduction of the switch's intrinsic diode for the ZVS operation. This stage ends when the current in the intrinsic diode (D_2) becomes null.

$$V_{CS1} = V_{CS} \cdot (1 + n)\,. \quad (12)$$

Fifth stage (t_4-t_5) – Figure 3.e: The current flowing across the diode D_2 becomes null at the instant t_4, and the current inverts its direction, conducted by the switch S_2. The current at the diode D_{M1} reduces until zero, blocking this diode at the instant t_5.

Sixth stage (t_5-t_6) – Figure 3.f: The diode D_{M3} starts conducting, charging the C_{o2} output capacitor with the voltage presented in (13). This stage is finished when the switch S_2 is turned off.

$$V_{Co2} = V_{CM1} + V_{CS} \cdot (1 + n)\,. \quad (13)$$

Seventh stage (t_6-t_7) – Figure 3.g: The switch S_2 is turned off, and the intrinsic switch S_1 capacitance (C_1) is discharged while the intrinsic switch S_2 capacitance (C_2) is charged. The energy to enable this process is provided by the leakage inductance (L_{dp}). When C_1 voltage becomes null, this stage ends.

$$V_{S1}(t_7) = V_{C1}(t_7) = 0 \quad (14)$$

$$V_{S2}(t_7) = V_{C2}(t_7) = V_{CM1}\,. \quad (15)$$

Eighth stage (t_7-t_8) – Figure 3.h: When the voltage of the intrinsic capacitance C_1 becomes null, the intrinsic diode D_1 conducts. The energy necessary to maintain the ZVS commutation in the switch S_1 turn-on of the proposed converter is supplied by leakage inductance of magnetic coupling. During the conduction of the intrinsic diode D_1, the command signal must be applied to ensure the ZVS commutation in switch S_1.

Ninth stage (t_7-t_8): In this stage, S_1 is turned on again, while the diode D_{M3} remains conductive until the beginning of the resonant period of that switch. The currents i_{Lp}, and i_{Ls} start to decrease when S_1 turns on and inverts its direction when the resonant period begins. After this stage, the operation returns to stage one.

B. *Theoretical Waveforms*

The main theoretical waveforms of the proposed converter are presented in Figure 4. The turn-on and turn-off commutations in both switches are ZVS. The leakage inductance allows the reduction of the reverse recovery current of the diodes and the ZVS/ZCS switching. The proposed converter operates on CCM in all load ranges due to the complementary operation of the switch S_2.

III. THEORETICAL ANALYSIS

Considering the operation stages and the theoretical waveforms, the main equations for the design of the proposed structure are presented.

A. *Capacitors Voltage and Converter Voltage Gain*

The voltage across the capacitors C_S and C_{M1} are presented in (16) and (17), respectively.

$$V_{CS} = \frac{V_i \cdot D}{(1 - D)} \quad (16)$$

$$V_{CM1} = \frac{V_i}{(1 - D)}\,. \quad (17)$$

The winding turn ratio between the primary and secondary of the series magnetic coupling formed by L_p/L_s is represented by the parameter (n). Considering (12), the voltage across the capacitor C_{S1} is calculated by (18).

$$V_{CS1} = \frac{D \cdot (1 + n)}{1 - D} \cdot V_i\,. \quad (18)$$

The output capacitor C_{o1} voltage is equal to the sum presented in (19):

$$V_{Co1} = V_i + n \cdot V_i + V_{CS1}\,. \quad (19)$$

Rearranging the (19), obtain (20):

$$V_{Co1} = \frac{1 + n}{1 - D} \cdot V_i \quad . \quad (20)$$

Considering (13), the voltage across the capacitor C_{o2} is given by (21).

$$V_{Co2} = \frac{1 + D \cdot (1 + n)}{1 - D} \cdot V_i\,. \quad (21)$$

The output voltage equals the sum of output capacitor voltages V_{Co1} and V_{Co2}, giving the voltage gain (M) of the proposed converter in (22):

$$M = \frac{V_o}{V_i} = \frac{2 + n + D \cdot (1 + n)}{1 - D}\,. \quad (22)$$

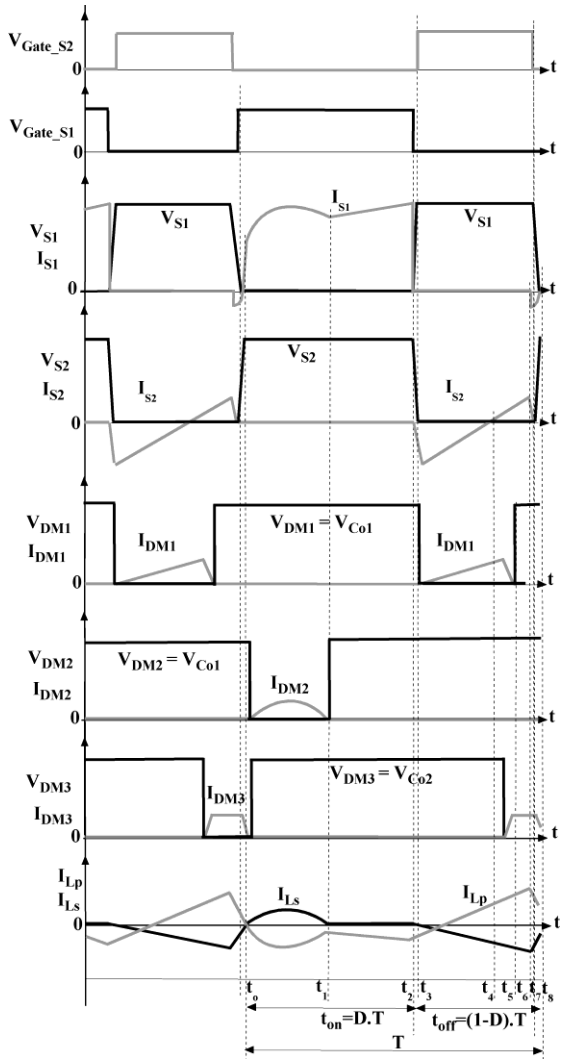

FIGURE 4. Theoretical waveforms.

Figure 5 presents the variation of the voltage gain with a coupled inductor turn ratio equal to 2. Some non-idealities at the converter's components, such as the intrinsic resistance of the converter's components (R_i) and the coupled inductor leakage inductance (L_{dp}), impact the converter voltage gain. They were accounted for through the parameters (α) and (β), respectively, as a function of the load resistance (R_o) and magnetizing inductance of the primary winding of the coupled inductors (L_m).

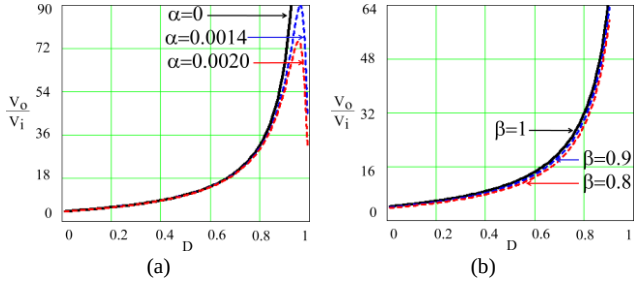

FIGURE 5. Converter voltage gain (n=2). (a) Ideal voltage gain (α=0) and intrinsic components resistance influence (α>0). (b) Ideal voltage gain (β=1) and coupled inductor leakage inductance influence (β<1).

$$\alpha = \frac{R_i}{R_o} \tag{23}$$

$$\beta = \frac{L_m}{L_m + L_{dp}} . \tag{24}$$

The main intrinsic resistances that influence the voltage gain come from the power switches and the inductors. However, as can be observed in Figure 5.a, this intrinsic resistance only influences the voltage gain in an extreme duty-cycle (D>0.9). Besides, the typical low voltage MOSFET used in this application presents very low conduction resistance (R_{DSon}<30 mΩ) and the current density usually considered in the inductor's design of high-efficiency converters results in operation close to ideal by working on duty-cycles lower than 0.8. The leakage inductance can be applied in the soft-switching process and a relatively low coupling coefficient can be considered in practice (β<0.9). The influence of the leakage inductance in the converter voltage gain is presented in Figure 5.b, showing that a small adjustment in the duty-cycle may be necessary considering reduced values of the coupling coefficient.

Some remarks are important to determine the coupled inductor turn ratio (n). The converter operation point can be chosen to avoid a high duty-cycle (D<0.8), increasing the coupled inductor turn ratio, but this would also increase current stress. The semiconductor's voltage stress, on the other hand, is reduced on higher converter duty-cycle. Therefore, a value of n=2 was chosen, operating with D=0.611 for the nominal converter specifications and a voltage gain equal to 15.

B. *Capacitors C_S, C_{S1} and C_{M1},*

The capacitor values can be calculated considering the charge variation and maximum voltage ripple specification. Low capacitance value is interesting to reduce volume and cost of these capacitors. Another relevant parameter is the resonant period $T_o=1/\omega_o$ given by (3), which occurs at the first operation stage (t_1-t_0). If half of the resonant period ($T_0/2$) is lower than the conduction period for switch S_1 (D.T), as shown in Figure 4, then zero current switching (ZCS) is possible for diode D_{M2}. If $T_o/2$ is close to switch D.T, then the resonant peak current calculated by (1) and the current stress are reduced.

The equivalent capacitance C_{eq} defined in (2) can be calculated by (25) considering a specified resonant period T_o and the leakage inductance L_{dp}.

$$C_{eq} = \left(\frac{T_o}{2 \cdot \pi}\right)^2 \cdot \frac{1}{L_{dp}} . \tag{25}$$

The capacitances C_S, C_{S1} and C_{M1} are considered equal and given by (26).

$$C_S = C_{S1} = C_{M1} = C_{eq} \cdot \left(2 + n^2\right). \tag{26}$$

C. *Input Inductor*

Considering an input current ripple Δ_{iL1}, the input inductance is given by (27). It is worth noting that the converter operates on low current ripple.

$$L_1 = \frac{V_i \cdot D}{\Delta_{iL1} \cdot f} . \tag{27}$$

D. *Semiconductor Current and Voltage Stress*

The maximum voltage of the power switches S_1 and S_2, and diodes are given by (28) and (29).

$$V_{S1} = V_{S2} = V_{CM1} = \frac{V_i}{1-D} = \frac{V_o}{2+n+D\cdot(1+n)} \quad (28)$$

$$V_{DM1} = V_{DM2} = V_{DM3} = \frac{V_i\cdot(1+n)}{1-D} = \frac{V_o\cdot(1+n)}{2+n+D\cdot(1+n)}. \quad (29)$$

The RMS current on switch S_1 can be approximated with equation (30), considering the output current (i_o), the converter voltage gain M, the resonant period T_o, switching period T and the constants k_1 and k_2 given by (31) and (32), respectively.

$$i_{S1rms} \approx i_o\sqrt{\frac{k_1^{\,2}}{2}\cdot\frac{T_o}{T} + 2\cdot k_1\cdot k_2\cdot\frac{T_o}{T} + k_2^{\,2}\cdot D} \quad (30)$$

$$k_1 = \frac{\pi\cdot(n+1)}{2}\cdot\frac{T_o}{T} \quad (31)$$

$$k_2 = M+1 \quad (32)$$

.

The RMS current on switch S_2 can be approximated by equations (33) and (34).

$$i_{S2rms} \approx \sqrt{\frac{i_{S2pk}^{\,2}\cdot(1-D)}{3}} \quad (33)$$

$$i_{S2pk} = i_o\cdot(M+1) + \frac{V_i\cdot D}{2\cdot f}\cdot\left(\frac{L_1+L_p}{L_1\cdot L_p}\right) \quad (34)$$

.

The average current on diodes D_{M1}, D_{M2}, and D_{M3} equals the output current i_o.

$$i_{DM1avg} = i_{DM2avg} = i_{DM3avg} = \frac{P_o}{V_o} = i_o \quad (35)$$

.

E. *Soft-switching Analysis and Coupled Inductor*

The zero-voltage resonant-transition (ZVRT) technique presented in [12], zero-voltage switching quasi-square wave (ZVS-QSW) in [13] or triangular current mode (TCM) in [11] and [14], was proposed for non-isolated dc-dc converters replacing the converter diode by an active switch with a complementary command. This operation requires reducing the converter inductance, which leads to increased inductor current ripple [10]. Figure 6.a presents the ZVRT configuration for the classical boost converter [13], and in Figure 6.b, the ZVRT configuration for the modified SEPIC converter presented in Figure 1.a [15]. Figure 6.c presents the condition for the soft-switching operation, where the instantaneous inductor current must be negative at the commutation instant to ensure the ZVS operation at the critical commutation switch (S_1 turn-on), as presented in [13] and [15]. This simple technique includes only an active switch, maintaining soft-switching from no-load operation until the nominal output power. The worst ZVS condition occurs at nominal output power because the average inductor current increases with the output power. The inductor value must be reduced to increase the current ripple, reaching the required current for the soft-switching operation. The average current at the converter inductor is reduced at light load operation, and a large negative instantaneous current is available to complete the charge and discharge of the intrinsic capacitance of the switches. Therefore, the main drawback of this technique is the increment in conduction losses needed to attain ZVS soft-switching. A typical efficiency curve for a ZVRT converter presents high efficiency at nominal output power, but the converter efficiency decreases significantly with output power reduction, due to the prevalence of conduction losses on light load.

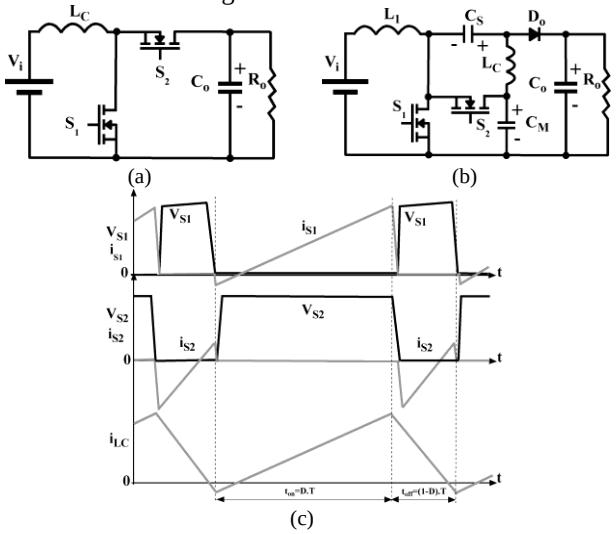

FIGURE 6. ZVRT technique. (a) classical ZVRT boost [13]; (b) ZVRT Modified SEPIC [15]; (c) Commutation waveforms.

This problem can be solved by increasing the switching frequency when operating with a light load, as proposed in [13] and [15], thus reducing the inductor´s current ripple and the conduction losses and ensuring high efficiency.

The same principle of the converter presented in Figure 6.b without a coupled inductor can be used for ZVS operation on the Figure 2 converter, reducing the magnetizing inductance of the coupled inductor L_p, ensuring the ZVS operation from nominal output power through to light load. However, this procedure increases conduction losses, which lowers efficiency mainly at light load operation. Considering a non-ideal coupling coefficient, the leakage inductance of the coupled inductors changes the original commutation process of the ZVRT technique, allowing ZVS without a significant increase in conduction losses. The energy stored from the leakage inductance makes it unnecessary to increase the inductor current ripple to maintain the ZVS operation, reducing the conduction losses and increasing the efficiency at light load operation without changing the switching frequency. As previously discussed, high-efficiency operation at light loads is relevant for photovoltaic applications where the weighted efficiency is a comparative parameter. Therefore, the use of the leakage inductance energy is considered in the commutation process analysis. The switch S_1 turn-off and switch S_2 turn-on ZVS commutation presented in the third operation stage, Figure 3.c, is maintained in all operation conditions because the instantaneous currents at the input inductor L_1 and the

coupled inductor L_p is used in the charge and discharge the switches' capacitances C_1-C_2. Considering a complementary command signal of the switches S_1-S_2 with a dead time higher than the interval for the intrinsic capacitors' voltage transition, the soft switching is maintained on all load conditions.

The switch S_2 turn-off and switch S_1 turn-on ZVS commutation presented in the seventh stage, Figure 3.g is a critical commutation that uses the energy of the leakage inductance to charge and discharge the switches' capacitors C_1-C_2. The worst operation condition occurs on light load, where the energy stored at the leakage inductance is lower than in nominal output power. Therefore, the light load operation condition is considered for soft-switching analysis, ensuring ZVS in all load ranges.

The ZVS operation is attainable at the critical commutation if the relation presented in (36) is respected. The energy stored at the leakage inductance L_{dp} must be higher than the energy stored at the commutation switch capacitors C_1-C_2, which is a function of the switch voltage at capacitor C_{M1}.

$$\frac{1}{2}\cdot\left(V_{CM1}\right)^2\cdot\left(C_1+C_2\right)\le\frac{1}{2}\cdot\left(i_{Lp\max}\right)^2\cdot L_{dp}. \qquad (36)$$

The energy stored at the leakage inductance is dependent on the current at the commutation instant (i_{LPmax}), given by (37) with light load operation.

$$i_{Lp\max}=\frac{V_i\cdot D}{2\cdot(L_p+L_{dp})\cdot f}. \qquad (37)$$

Therefore, the magnetizing inductance of the coupled inductor L_p and the leakage inductance L_{dp} can be adjusted by (35) and (36) to ensure ZVS operation in all load ranges.

The derivative of the voltage of switches S_1-S_2 at the turn-off instant can be controlled by adding an external capacitor connected in parallel to the switches, leading to soft-switching. The inclusion of an external capacitor can be necessary when using switches with low output capacitance. This capacitance can be calculated as a function of a maximum dv/dt to attain the ZVS commutation. However, the increment of this capacitance requires more energy from the leakage inductance to maintain the ZVS operation.

IV. PROPOSED CONVERTER COMPARISON

Table I compares the proposed converter considering recent soft-switching high-gain structures using coupled inductors and voltage multiplier cells. The voltage gain and normalized switches and diodes voltage stress are shown and compared in Figures 7.a, 7.b, and 7.c, respectively, considering a coupled inductor turn ratio n=2 and m=2 for the converter proposed in [27] using three coupled windings.

The proposed structure presents the second highest voltage gain, as shown in Figure 7.a, lower only than the converter presented in [28] which employs more components and is therefore more complex. The proposed converter performs with the lowest switch voltage stress operating with a duty-cycle higher than 0.4, as shown in Figure 7.b. The low input current ripple presented by [25], [27] and by the proposed converter is desirable for renewable power sources such as photovoltaic systems. All compared topologies present suitable efficiencies, higher than 94% at nominal output power, operating with high switching frequency. However, the proposed converter increases efficiency by reducing the output power due to the soft-switching operation in all load ranges without excessive current stress. Therefore, the proposed converter presents the highest weighted efficiency.

The proposed converter does not present the common ground connection between the input and output. However, the soft-switching technique developed can also be applied to the structures presented in Figures 1.b, 1.c, or 1.d with similar operation characteristics in applications where the common ground is required.

TABLE 1. Converter Comparison.

Converter	Voltage gain (V_o/V_i)	Normalized switch voltage (V_S/V_o)	Normalized diode voltage (V_D/V_o)	Number of components				Input current ripple	Nominal efficiency and Weighted efficiency	Common Ground
				S	D	C	MC			
[25]	$\frac{1+n}{1-D}$	$\frac{1}{1+n}$	$\frac{n}{1+n}$	2	2	5	2	Low	η=95.7% η_{EU}=94.7% η_{CEC}=95.3%	Yes
[26]	$\frac{1+2\cdot n}{1-D}$	$\frac{1}{1+2\cdot n}$	$\frac{n}{1+2\cdot n}$	2	4	5	1	High	η=94.5% η_{EU}=93.9% η_{CEC}=94.5%	Yes
[27]	$\frac{2+n}{1-D}+m$	$\frac{1}{2+n+m(1-D)}$	$\frac{(1+n+m)}{2+n+m(1-D)}$	2	2	4	2	Low	η=95.6% η_{EU}=95.6% η_{CEC}=96.1%	Yes
[28]	$\frac{n\cdot(2-D)}{(1-D)^2}+1$	$\frac{(1-D)}{n\cdot(2-D)+(1-D)^2}$	$\frac{n}{n\cdot(2-D)+(1-D)^2}$	4	4	5	2	High	η=94.8% η_{EU}=93.1% η_{CEC}=94.1%	Yes
Proposed	$\frac{2+n+D\cdot(1+n)}{1-D}$	$\frac{1}{2+n+D\cdot(1+n)}$	$\frac{1+n}{2+n+D\cdot(1+n)}$	2	3	5	2	Low	η=94.5% η_{EU}=96.3% η_{CEC}=96.5%	No

S: Switches; D: Diodes; C: Capacitors; MC: Magnetic Cores; n: Coupling inductor turn ratio; m: coupling inductor turn ratio for [27].

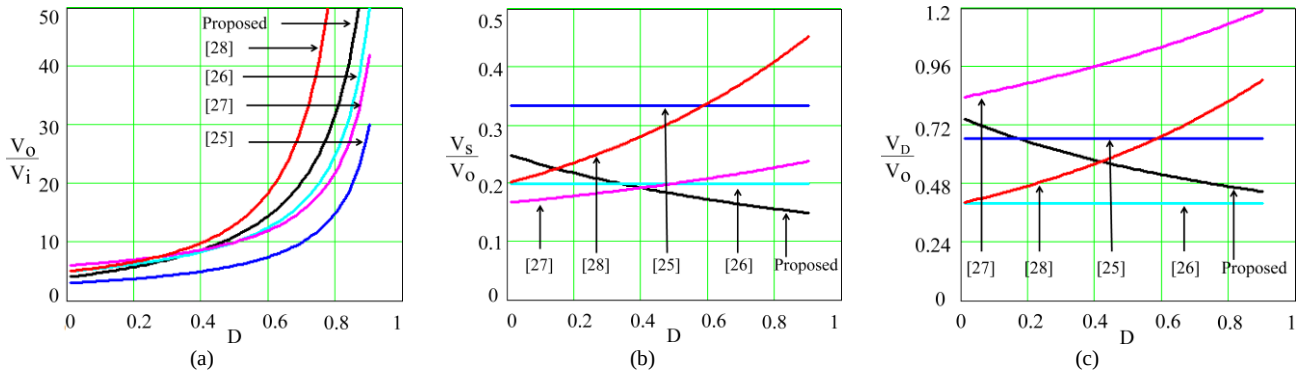

FIGURE 7. Proposed converter comparison (n=2). (a) Voltage gain; (b) Normalized switch voltage stress; (c) Normalized diode voltage stress.

V. EXPERIMENTAL RESULTS

The proposed converter presented in Figure 2 was tested with the implementation of the experimental prototype shown in Figure 8. Table II presents the converter parameters and specifications considered in the design procedure, following theoretical analysis and main equations discussed in section III. The prototype components' specifications are also included in Table II.

TABLE 2. Converter Specifications and Parameters.

Parameters	Specifications
Input voltage (V_i)	30 V
Output voltage (V_o)	450 V
Output power (P_o)	200 W
Switching frequency (f)	100 kHz
L_p-L_s turn ration (n)	2
Leakage inductance influence (β)	0.82
Input current ripple (Δ_{iL1})	30% of i_{L1}
S_1 - S_2	IRFP4768 (V_{DS}=250 V/R_{DSon}=14.5 mΩ)
D_{M1} - D_{M2} - D_{M3}	MBR40250 (V_{RRM}=250 V / I_F=40 A, V_F=0.71 V)
C_S - C_{S1} - C_{M1}	1 μF/400 V (Polypropylene)
L_1	95.41 μH (EE/42-15 Thornton) 20 turns
L_p- L_s	53.75 μH / 202.8 μH (EE/42-15 Thornton) 15 turns / 30 turns
C_{o1}-C_{o2}	100 μF/400 V (Electrolytic)

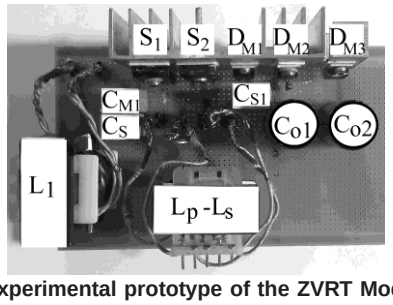

FIGURE 8. Experimental prototype of the ZVRT Modified SEPIC converter with coupling inductor and voltage multiplier cell.

Figure 9 shows the switch S_1 voltage and current operating with 100%, 50%, 25%, and 13% of the output power. The switch S_1 turn-on is the critical commutation depending on the coupling inductors' leakage inductance to attain ZVS operation. As can be observed in this figure, the switch S_1 capacitance is discharged, the intrinsic S_1 diode conducts, and then S_1 is turned on, maintaining the ZVS operation in all load ranges.

Figure 10 shows the switch S_2 voltage and current operating with 100%, 50%, 25%, and 13% of the output power.

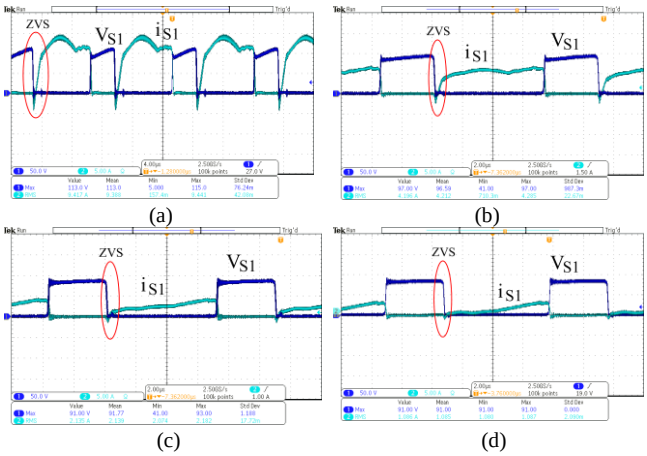

Figure 9. Switch S_1 voltage and current operating with different output power. (a) P_o=200 W; (b) P_o=100 W; (c) P_o=50 W; (d) P_o=26 W.

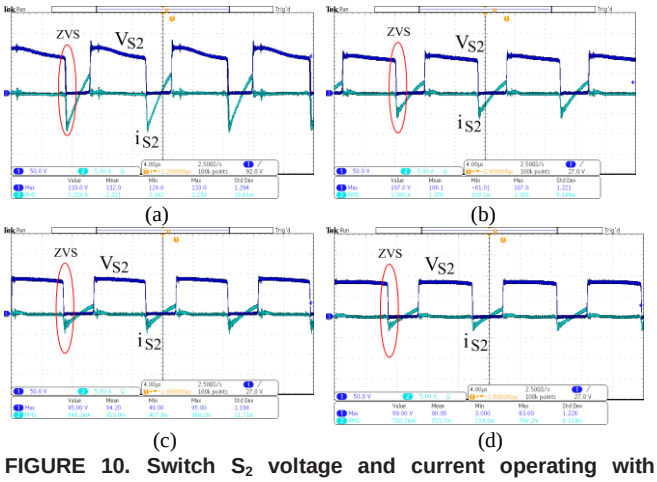

FIGURE 10. Switch S_2 voltage and current operating with different output power. (a) P_o=200 W; (b) P_o=100 W; (c) P_o=50 W; (d) P_o=26 W.

The switch S_2 turn-on is the non-critical commutation operating with input inductor L_1 and coupled inductor L_p current, maintaining the ZVS operation in all load ranges.

The gate-source (V_{gate_S1}-V_{gate_S2}) and drain-source (V_{S1}-V_{S2}) voltages of the switches S_1 and S_2 operating with 100%, 50%, 25%, and 13% of the output power are presented in

Figure 11. ZVS operation is verified in all load ranges without overlapping the switches' voltage signals.

Figure 12 presents some converter waveforms operating at nominal output power. Both the output voltage and the capacitor C_S, C_{M1} and C_{S1} voltage follow the equations presented in section III.

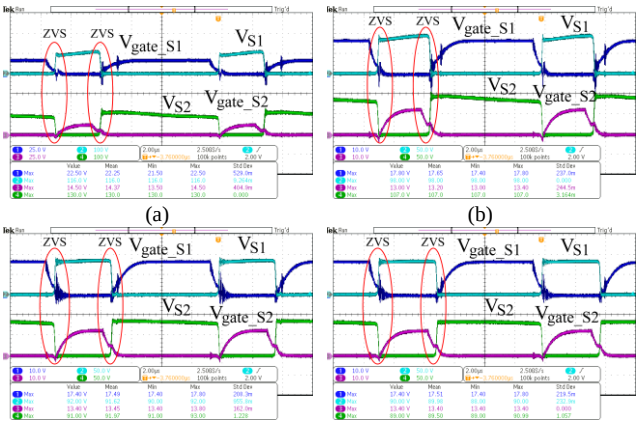

FIGURE 11. Switches S_1 and S_2 drain-source and gate-source voltage operating with different output power. (a) P_o=200 W; (b) P_o=100 W; (c) P_o=50 W; (d) P_o=26 W.

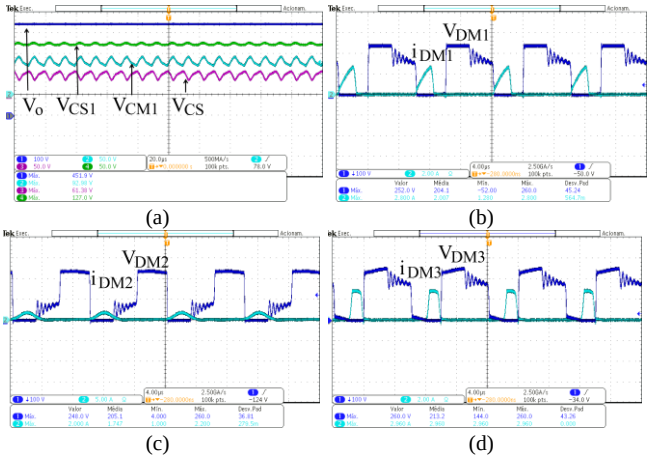

FIGURE 12. Converter waveforms operating at the nominal output power. (a) Output voltage Vo and capacitors C_{S1}, C_S and C_{M1} voltages. (b) Diode D_{M1} voltage and current; (c) Diode D_{M2} voltage and current; (c) Diode D_{M3} voltage and current.

The diodes are blocked with zero current switching (ZCS) due to the presence of the leakage inductance of the coupled inductor.

The experimental efficiency of the proposed converter is shown in Figure 13, being equal to 94.55% at nominal output power P_o=200 W and the maximum efficiency of 98% at P_o=70 W, operating with a switching frequency of 100 kHz. The soft-switching operation at light load with low current stress increases the efficiency with load reduction.

The European weighted efficiency is EU=96.3%, and the California Energy Commission weighted efficiency is CEC=96.5%, considering the results presented in Figure 13.

The main converter losses are shown in Figure 14, with the magnetic elements being responsible for most of them.

VI. CONCLUSIONS

A high-efficiency Modified SEPIC converter operating with soft-switching and high voltage gain is presented in this paper. The inclusion of the ZVRT soft-switching technique for Modified SEPIC converters using voltage multiplier cells and coupled inductors is proposed using the leakage inductance in the soft-switching process. Compared with the original ZVRT soft-switching technique, in which a high inductor current ripple is necessary for the ZVS operation, the proposed technique uses the leakage inductance of the coupled inductor in the commutation process, resulting in low current stress and reduced conduction losses. The soft-switching is maintained in all load range operating in CCM with reduced conduction losses. The simple implementation with the inclusion of only one active switch and high-efficiency operation at light load are also highlighted. The efficiency of the proposed converter is equal to 94.55 % at the nominal output power of 200 W with 100 kHz of switching frequency. The maximum efficiency was 98% when operating at 70 W.

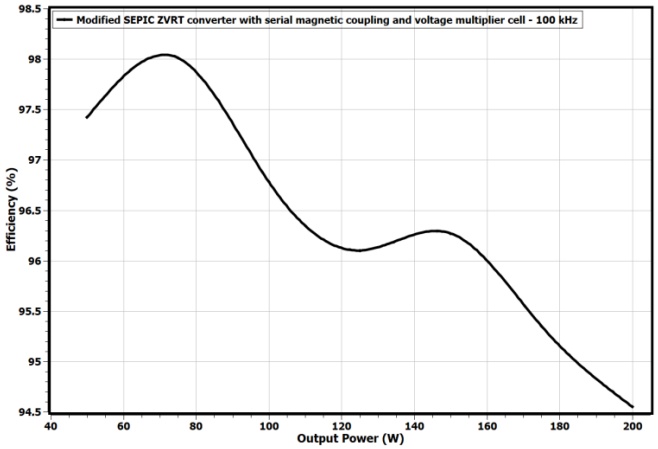

FIGURE 13. Experimental efficiency curve of the proposed converter.

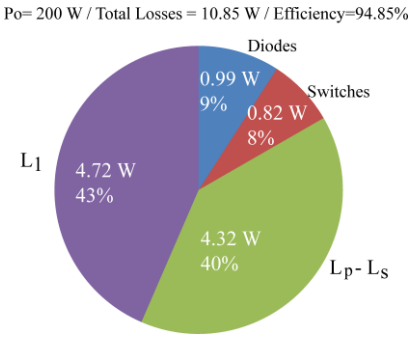

FIGURE 14. Main converter losses.

AUTHOR'S CONTRIBUTIONS

Conceptualization, Data Curation, Formal Analysis, Funding, Acquisition, Investigation, Methodology, Software, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing: KRAVETZ, F.I.; Conceptualization, Data Curation, Funding Acquisition, Methodology, Project Administration, Resources, Supervision, Writing – Review & Editing: GULES, R.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate—Similarity Check.

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